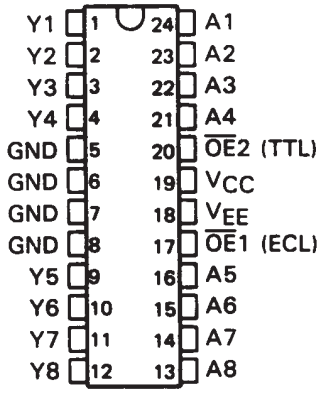
SDZS001A – D3136, AUGUST 1988 – REVISED DECEMBER 1988

- **10KH Compatible**
- **ECL and TTL Control Inputs**
- **P-N-P Inputs Reduce DC Loading**
- **Flow-Through Architectures Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE} and GND Configurations Minimize High-Speed Switching Noise**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These octal TTL-to-ECL translators are designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. The designer has a choice of inverting ('5542) or true ('5543) outputs. Two pins, $\overline{OE}1$ and $\overline{OE}2$, are provided for output enable control. These control inputs are negative ANDed together, with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment. The outputs, when disabled, go to a normal ECL logic low level.

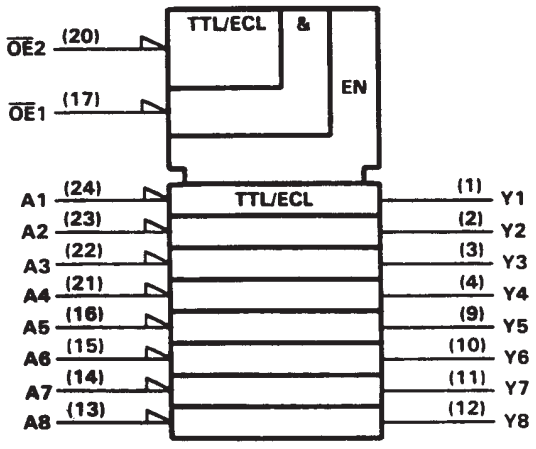
The SN10KHT5542 and SN10KHT5543 are characterized for operation from 0°C to 75°C.

FUNCTION TABLE

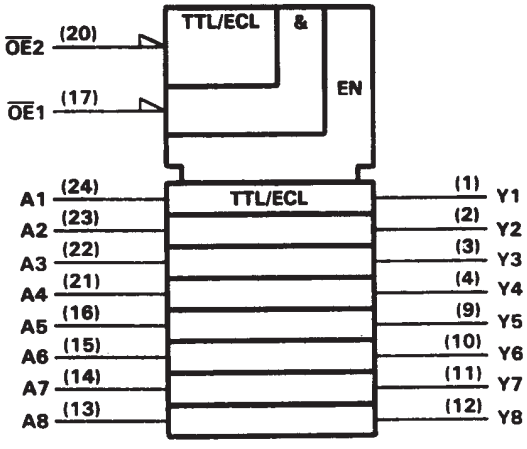
OUTPUT CONTROL		DATA INPUT	OUTPUT	
$\overline{OE}1$	$\overline{OE}2$	A	'5542	'5543
H	X	X	L	L
X	H	X	L	L
L	L	L	H	L
L	L	H	L	H

logic symbols†

SN10KHT5542



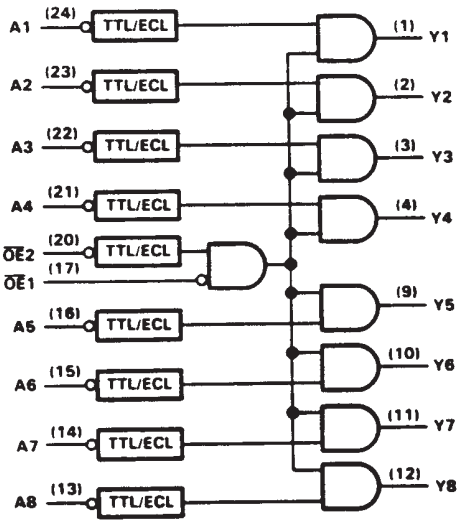
SN10KHT5543



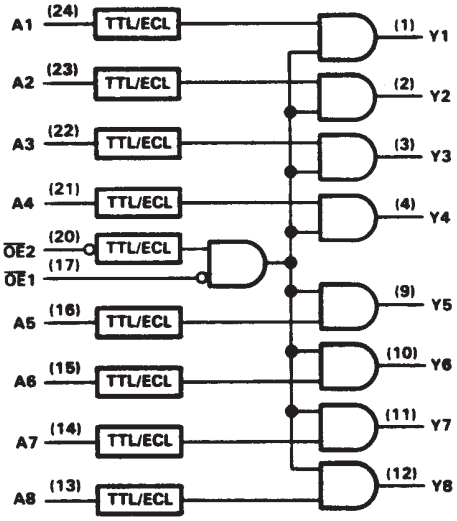
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN10KHT5542



SN10KHT5543



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . −8 V to 0 V
Input voltage range (TTL) (See Note 1) . . . . . −1.2 V to 7 V
Input voltage range (ECL) . . . . . V_{EE} to 0 V
Input current range (TTL) . . . . . −30 mA to 5 mA
Operating ambient temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5.0	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IH}	ECL high-level input voltage‡	0°C	−1170		−840	mV
		25°C	−1130		−810	
		75°C	−1070		−735	
V_{IL}	TTL low-level input voltage				0.8	V
V_{IL}	ECL low-level input voltage‡	0°C	−1950		−1480	mV
		25°C	−1950		−1480	
		75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	mA
T_A	Operating ambient temperature (see Note 3)		0		75	°C

‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. If unused, $\overline{OE}1$ should be tied directly to −2 V.

3: Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse air flow greater than 500 linear ft/min is maintained.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.94 V, I_I = −18 mA				−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 7 V				0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 2.7 V				20	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −840 mV	0°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −810 mV	25°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −735 mV	75°C			350	
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 0.5 V				−500	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −1950 mV	0°C	0.5			
			25°C	0.5			
			75°C	0.5			
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1020		−840	mV
			25°C	−980		−810	
			75°C	−920		−735	
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1950		−1630	mV
			25°C	−1950		−1630	
			75°C	−1950		−1600	
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			15	22	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			17	25	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			−78	−111	mA
C_i		V_{CC} = 5 V, V_{EE} = −5.2 V, f = 10 MHz			5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.7	3.7	ns
t_{PHL}			0.1	1.6	3.3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.8	2.8	5	ns
t_{PHL}			0.4	2.3	4.5	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.8	3	5.3	ns
t_{PHL}			0.6	2.5	4.7	
t_r		Y		1.5		ns
t_f				1.5		

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to −2 V.

4. Load circuit and switching waveforms are shown in Section 1.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.94 V, I_I = −18 mA				−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 7 V				0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 2.7 V				20	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −840 mV	0°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −810 mV	25°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −735 mV	75°C			350	
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 0.5 V				−500	μA
	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −1950 mV	0°C	0.5			
			25°C	0.5			
			75°C	0.5			
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1020		−840	mV
			25°C	−980		−810	
			75°C	−920		−735	
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −5.2 V, ±5%, See Note 3	0°C	−1950		−1630	mV
			25°C	−1950		−1630	
			75°C	−1950		−1600	
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			17	25	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			15	22	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			−77	−111	mA
C_i		V_{CC} = 5 V, V_{EE} = −5.2 V, f = 10 MHz			5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.5	3	ns
t_{PHL}			0.1	1.5	3.3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.6	2.2	4.3	ns
t_{PHL}			0.5	2.4	4.3	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.7	2.2	4.4	ns
t_{PHL}			0.5	2.6	4.7	
t_r		Y		1.5		ns
t_f				1.5		

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to −2 V.

4. Load circuit and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN10KHT5543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	10KHT5543	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

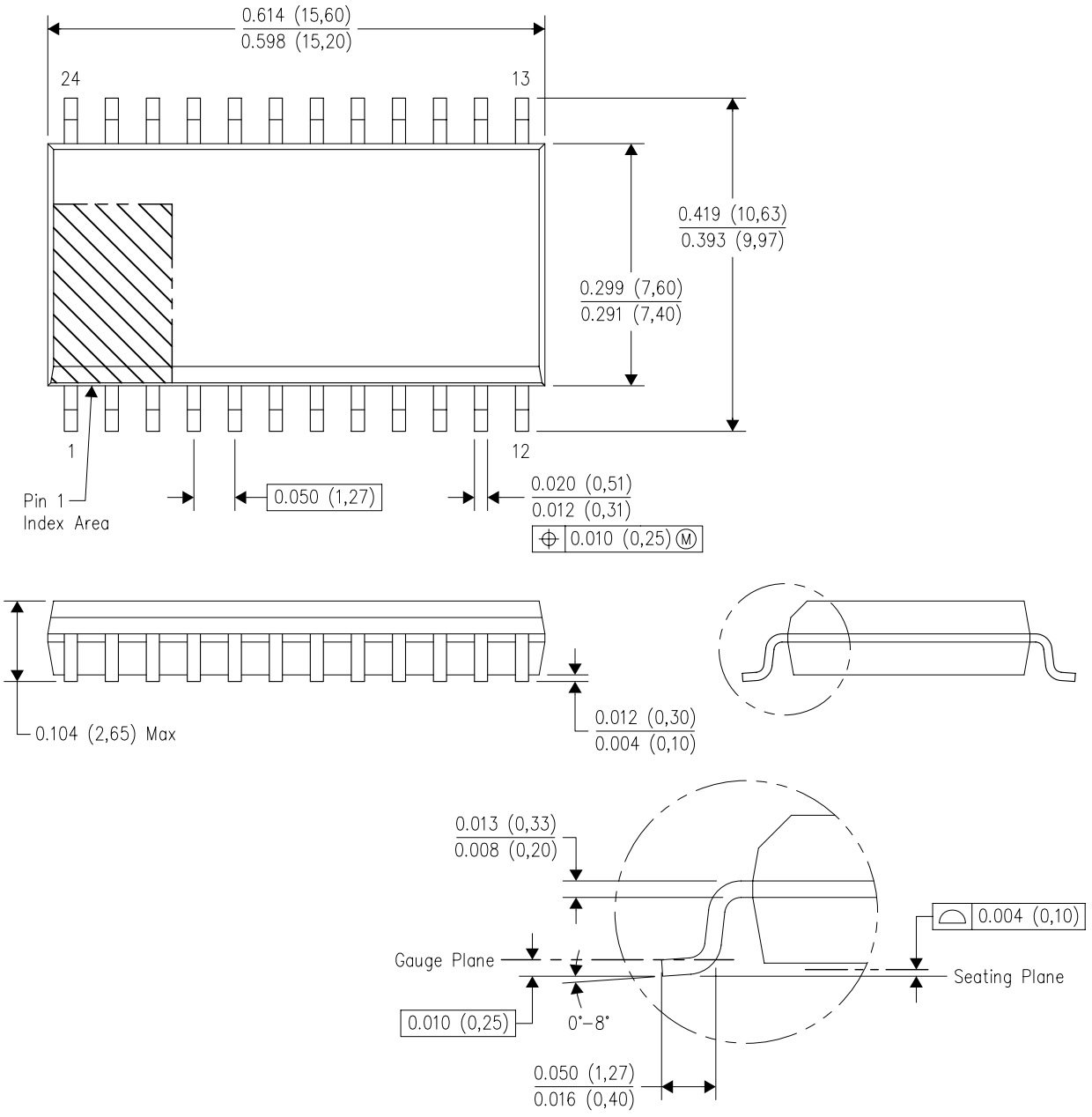
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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