

256Mb/512Mb/1Gb SEMPER™ Flash

Quad SPI, 1.8V/3.0V

Features

- CYPRESS™ 45-nm MIRRORBIT™ technology that stores two data bits in each memory array cell
- Sector architecture options
 - Uniform: Address space consists of all 256KB sectors
 - Hybrid Configuration 1: Address space consists of thirty-two 4KB sectors grouped either on the top or the bottom while the remaining sectors are all 256KB
 - Hybrid Configuration 2: Address space consists of thirty-two 4KB sectors equally split between top and bottom while the remaining sectors are all 256KB
- Page programming buffer of 256 or 512 bytes
- OTP secure silicon array of 1024 bytes (32 × 32 bytes)
- Quad SPI
 - Supports 1S-1S-4S, 1S-4S-4S, 1S-4D-4D, 4S-4S-4S, 4S-4D-4D protocols
 - SDR option runs up to 83-Mbps (166MHz clock speed)
 - DDR option runs up to 102-Mbps (102MHz clock speed)
- Dual SPI
 - Supports 1S-2S-2S protocol
 - SDR option runs up to 41.5-Mbps (166MHz clock speed)
- SPI
 - Supports 1S-1S-1S protocol
 - SDR option runs up to 21-Mbps (166MHz clock speed)
- Functional safety features
 - Functional safety with the industry's first ISO26262 ASIL B compliant and ASIL D ready NOR Flash
 - Infineon® Endurance Flex architecture provides high-endurance and long retention partitions
 - Data integrity CRC detects errors in memory array
 - SafeBoot reports device initialization failures, detects configuration corruption, and provides recovery options
 - Built-in error correcting code (ECC) corrects single-bit error and detects double-bit error (SECCDED) on memory array data
 - Sector erase status indicator for power loss during erase
- Protection features
 - Legacy block protection for memory array and device configuration
 - Advanced sector protection for individual memory array sector based protection
- AutoBoot enables immediate access to the memory array following power-on
- Hardware reset through CS# Signaling method (JEDEC) / individual RESET# pin / DQ3_RESET# pin
- Serial flash discoverable parameters (SFDP) describing device functions and features
- Device identification, manufacturer identification, and unique identification
- Data Integrity
 - 256Mb devices
 - Minimum 640,000 program-erase cycles for the main array
 - 512Mb devices
 - Minimum 1,280,000 program-erase cycles for the main array
 - 1Gb devices
 - Minimum 2,560,000 program-erase cycles for the main array
 - All devices
 - Minimum 300,000 program-erase cycles for the 4KB sectors
 - Minimum 25 Years data retention

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Performance summary

- Supply voltage
 - 1.7V to 2.0V (HS-T)
 - 2.7V to 3.6V (HL-T)
- Grade / temperature range
 - Industrial (–40°C to +85°C)
 - Industrial plus (–40°C to +105°C)
 - Automotive AEC-Q100 grade 3 (–40°C to +85°C)
 - Automotive AEC-Q100 grade 2 (–40°C to +105°C)
 - Automotive AEC-Q100 grade 1 (–40°C to +125°C)
- Packages
 - 256MB and 512MB
 - 16-lead SOIC (300mil) - SO3016
 - 24-ball BGA 6 × 8 mm
 - 16-lead SOIC (300mil)
 - 8-contact WSON 6 × 8 mm
 - 1GB
 - 16-lead SOIC (300mil) - SO3016
 - 24-ball BGA 8 × 8 mm
 - 16-lead SOIC (300mil)

Performance summary

Maximum read rates

| Transaction | Initial access latency (Cycles) | Clock rate (MHz) | Mbps |
|---------------|---------------------------------|------------------|-------|
| SPI Read | 0 | 50 | 6.25 |
| SPI Fast Read | 9 | 166 | 20.75 |
| Dual Read SDR | 7 | 166 | 41.5 |
| Quad Read SDR | 10 | 166 | 83 |
| Quad Read DDR | 7 | 102 | 102 |

Typical Program and Erase rates

| Operation | Kbps |
|---|-----------|
| 256B page programming (4KB sector / 256KB sector) | 595 / 533 |
| 512B page programming (4KB sector / 256KB sector) | 753 / 898 |
| 256KB sector erase | 331 |
| 4KB sector erase | 95 |

Typical current consumption

| Operation | Current (mA) |
|------------------------|--------------|
| SDR Read 50MHz | 10 |
| SDR Read 166MHz | 53 |
| DDR Read 102MHz | 50 |
| Program | 50 |
| Erase | 50 |
| Standby (HS-T) | 0.011 |
| Standby (HL-T) | 0.014 |
| Deep power down (HS-T) | 0.0013 |
| Deep power down (HL-T) | 0.0022 |

Data integrity

Program / Erase (PE) endurance - High endurance (256KB sectors)

| Sectors in partition | Minimum PE cycles | Minimum retention time | Unit |
|---------------------------------|-------------------|------------------------|-------|
| 512 (Default for 1GB devices) | 2,560,000 | 2 | Years |
| 508 | 2,540,000 | | |
| 504 | 2,520,000 | | |
| ... | ... | | |
| 256 (Default for 512MB devices) | 1,280,000 | | |
| 252 | 1,260,000 | | |
| 128 (Default for 256MB devices) | 640,000 | | |
| ... | ... | | |
| 28 | 140,000 | | |
| 24 | 120,000 | | |
| 20 | 100,000 | | |

Note Minimum cycles is for entire high endurance partition.

Program / Erase endurance - Long retention partition (256KB sectors)

| Minimum PE cycles | Minimum retention time | Unit |
|-------------------|------------------------|-------|
| 500 | 25 | Years |

Note Minimum cycles is for each sector.

Program / Erase endurance 4KB sector and nonvolatile register array

| Flash memory type | Minimum cycles | Unit | Minimum retention time | Unit |
|---|----------------|-----------|------------------------|-------|
| Program/Erase cycles per 4KB sector | 500 | PE cycles | 25 | Years |
| | 300,000 | | 2 | |
| Program/Erase cycles per persistent protection bits (PPB) array or nonvolatile register array | 500 | | 25 | |

Note It is required to restrict the power loss events to 300 times per sector during program or erase operation to achieve the mentioned endurance cycles.

Note Each write transaction to a nonvolatile register causes a PE cycle on the entire nonvolatile register array.

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1 Pinout and signal description

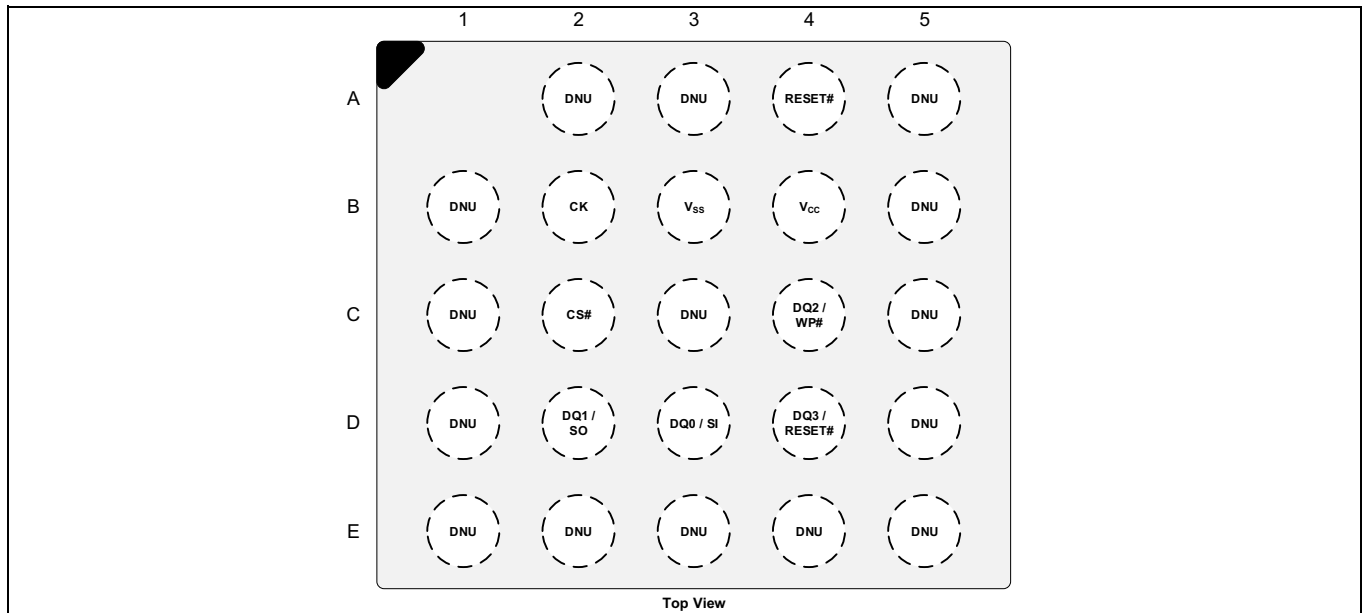


Figure 1 24-ball BGA pinout configuration^[1]

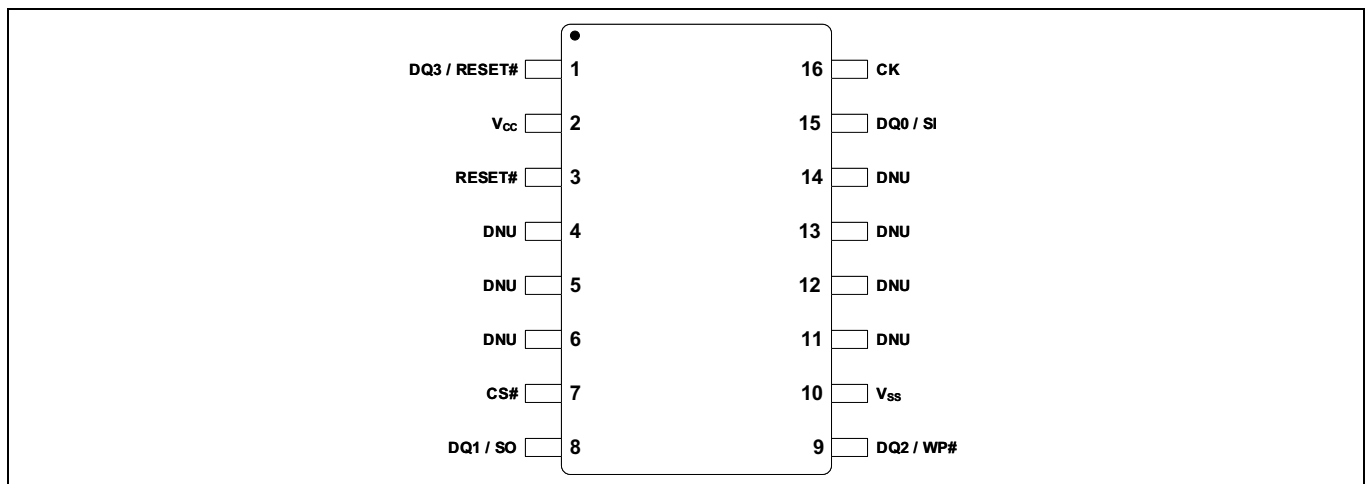


Figure 2 16-lead SOIC package (SO316), top view

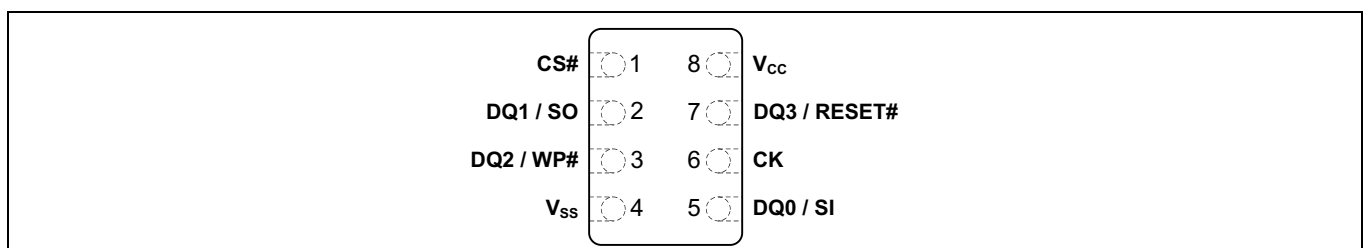


Figure 3 8-connector package (WSON 6 × 8), top view

Note

- Flash memory devices in BGA packages can be damaged if exposed to ultrasonic cleaning methods. The package, data integrity, or both may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Pinout and signal description

Table 1 Signal description

| Symbol | Type | Mandatory / optional | Description |
|-----------------|--------------------------------|----------------------|---|
| CS# | Input | Mandatory | Chip Select (CS#) . All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH. |
| CK | Input | Mandatory | Clock (CK) . Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock. |
| DQ0 / SI | Input/Output | Mandatory | Serial Input (SI) for single SPI protocol DQ0 Input/ Output for Dual or Quad SPI protocol |
| DQ1 / SO | Input/Output | Mandatory | Serial Output (SO) for single SPI protocol DQ1 Input/ Output for Dual or Quad SPI protocol |
| DQ2 / WP# | Input/Output (weak Pull-up) | Mandatory | Write Protect (WP#) for single and dual SPI protocol DQ2 Input/ Output for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad transactions or write protection. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register transactions. |
| DQ3 / RESET# | Input/Output (weak Pull-up) | Mandatory | RESET# for single and dual SPI protocol. This signal can be configured as RESET# when CS# is HIGH or Quad SPI protocol is disabled. DQ3 Input/ Output for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad SPI transactions or RESET# |
| RESET# | Input (weak Pull-up) | Optional | Hardware Reset (RESET#) . When LOW, the device will self initialize and return to the array read state. DQ[3:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own. |
| V _{CC} | Power Supply | Mandatory | Core Power Supply |
| V _{SS} | Ground Supply | Mandatory | Core Ground |
| DNU | - | - | Do Not Use. |

2 Interface overview

2.1 General description

The CYPRESS™ SEMPER™ Flash with Quad SPI family of products are high-speed CMOS, MIRRORBIT™ NOR Flash devices. SEMPER™ Flash is designed for Functional Safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

SEMPER™ Flash with Quad SPI devices support traditional SPI single bit serial input and output, optional two bit (Dual I/O or DIO) as well as four bit wide Quad I/O (QIO) and Quad Peripheral Interface (QPI) protocols. In addition, there are DDR read transactions for QIO and QPI that transfer address and read data on both edges of the clock.

Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4KBs or 256KBs).

SEMPER™ Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256KB sector array, or a hybrid configuration 1 where thirty-two 4KB sectors are either grouped at the top or at the bottom while the remaining sectors are all 256KB, or a hybrid configuration 2 where the thirty-two 4KB sectors are equally split between the top and the bottom while the remaining sectors are all 256KB.

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

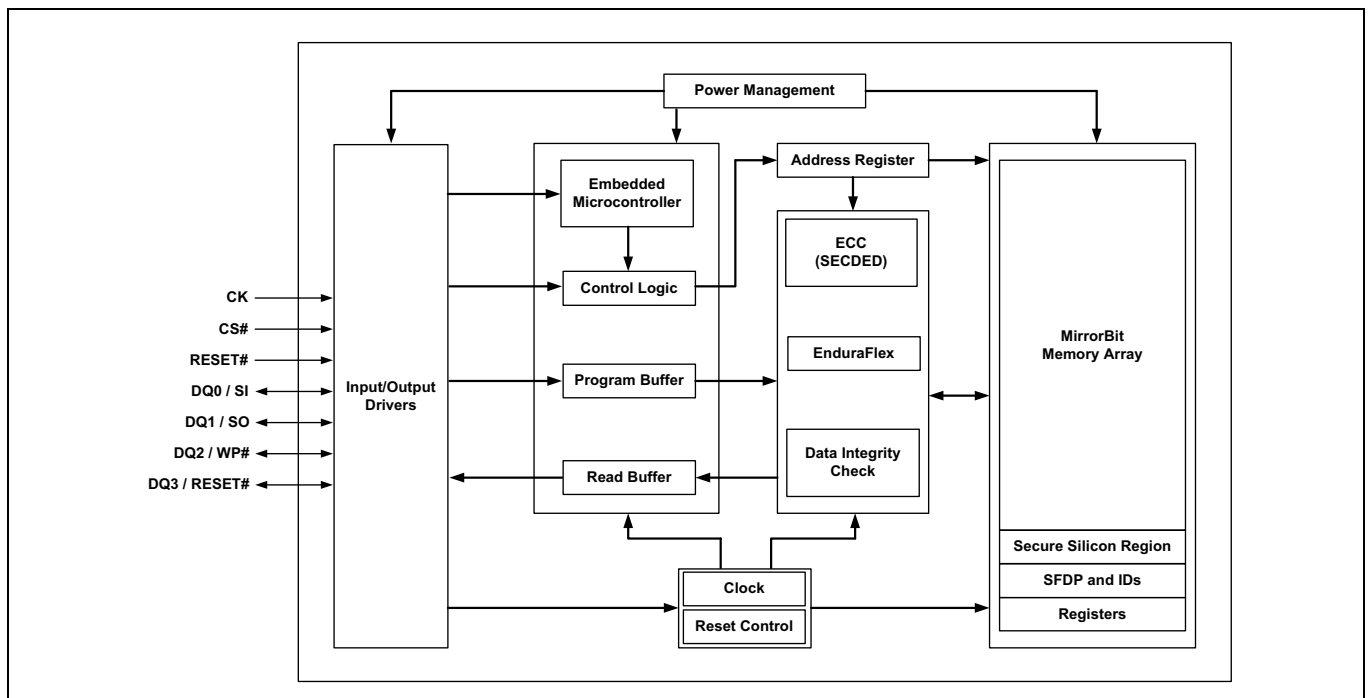


Figure 4 Logic block diagram

The SEMPER™ Flash with Quad SPI family consists of multiple densities with, 1.8V and 3.0V core and I/O voltage options.

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related Embedded Algorithms.

Changing the nonvolatile data in the memory array requires a sequence of operations that are part of Embedded Algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

Executing code directly from flash memory is often called Execute-In-Place (XIP). By using XIP with SEMPER™ Flash devices at the higher clock rates with Quad or DDR Quad SPI transactions, the data transfer rate can match or exceed traditional parallel or asynchronous NOR Flash memories while reducing signal count dramatically.

Infineon® Endurance Flex architecture provides system designers the ability to customize the NOR Flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

The SEMPER™ Flash with Quad SPI device supports error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.

The SEMPER™ Flash with Quad SPI device has built-in diagnostic features providing the host system with the device status.

- Program and Erase Operation: Reporting of program or erase success, failure and suspend status
- Error Detection and Correction: 1-bit and/or 2-bit error status with address trapping and error count
- Data Integrity Check: Error detection over memory array contents
- SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery
- Sector Erase Status: Reporting of erase success or failure status per sector
- Sector Erase Counter: Counts the number of erase cycles per sector

2.2 Signal protocols

2.2.1 SEMPER™ Flash with Quad SPI clock modes

The SEMPER™ Flash with Quad SPI device can be driven by an embedded microcontroller (bus master) in either of the following two clocking modes:

- **Mode 0** with Clock Polarity LOW at the fall of CS# and staying LOW until it goes HIGH at capture input.
- **Mode 3** with Clock Polarity HIGH at the fall of CS# then going LOW to HIGH at capture input.

For these two modes, data is latched into the device on the rising edge of the CK signal in SDR protocol and both edges of the CK signal in DDR protocol. The output data is available on the falling edge of the CK clock signal. For DDR protocol, Mode 3 is not supported.

The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

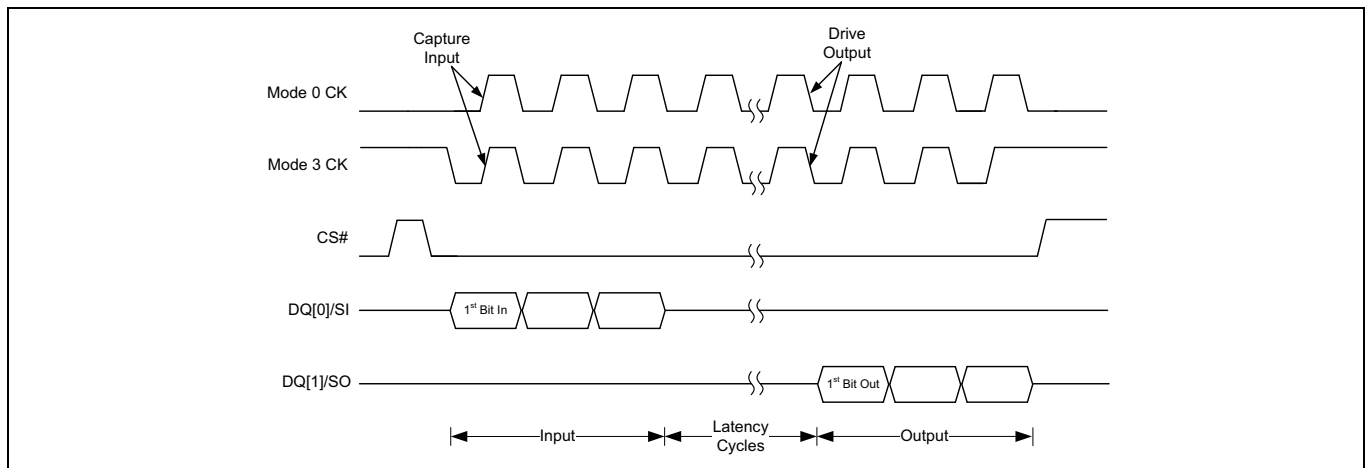


Figure 5 SPI SDR mode support

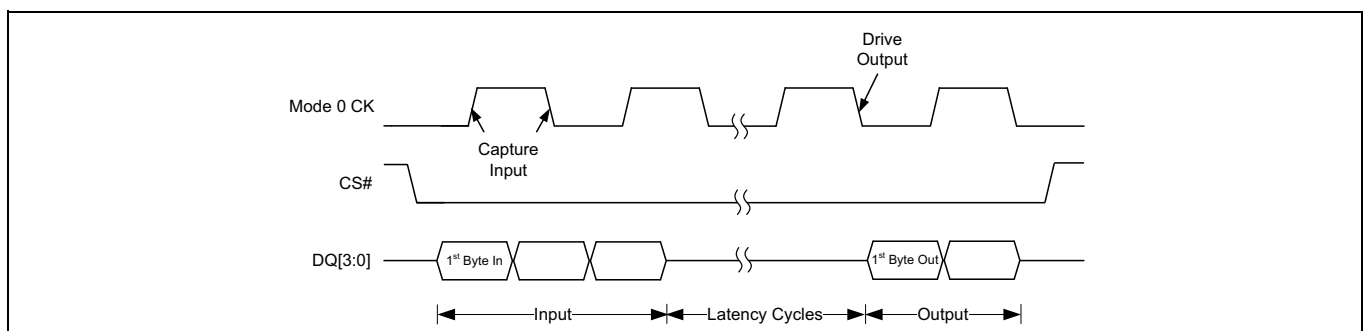


Figure 6 SPI DDR mode support

2.3 Transaction protocol

Transaction

- During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (DQ) signals followed by address and data from the host to the flash device. The clock continues to toggle during the transfer of read data from the flash device to the host or write data from the host to the flash device. When the host has transferred the desired amount of data, the host drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.
- While CS# is inactive, the CK is not required to toggle.
- The command transfer occurs at the beginning of every transaction. The address, latency cycles, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.

Transaction capture

- CK marks the transfer of each bit or group of bits between the host and memory. Command, address and write data bits transfer occurs on CK rising edge in SDR transactions, or on every CK edge, in DDR transactions.

NoteAll attempts to read the flash memory array during a program or erase (embedded operations) are ignored. The embedded operation will continue to execute without any effect. A very limited set of commands are accepted during an embedded operation. These are discussed in [Suspend and resume embedded operation on page 61](#).

Protocol terminology

- The number of DQ signals used during the transaction, depends on the current protocol mode or command transferred. The latency cycles do not use the DQ signals for information transfer. The protocol mode options are described by the data rate and the DQ width (number of DQ signals) used during the command, address, and data phases in the following format:
WR-WR-WR, where:
 - The first WR is the command bit width and rate.
 - The second WR is the address bit width and rate.
 - The third WR is the data bit width and rate.
- The bit width value may be 1, 2 or 4. R has a value of S for SDR or D for DDR. SDR has the same transfer value during the rising and falling edge of a clock cycle. DDR can have different transfer values during the rising and falling edges of each clock.
- Examples:
 - 1S-1S-1S means that the command is 1 bit wide SDR, the address is 1 bit wide SDR, and the data is one bit wide SDR.
 - 4S-4D-4D means that the command is 4 bits wide SDR, address, and data transfers are 4 bits wide DDR.

Protocols definition

- Protocol Modes defined for the SEMPER™ Flash with Quad SPI:
 1. 1S-1S-1S: One DQ signal used during command transfer, address transfer, and data transfer. All phases are SDR.
 2. 1S-2S-2S: One DQ signal used during command transfer, two DQ signals used during address transfer, and data transfer. All phases are SDR.
 3. 1S-1S-4S: One DQ signal used during command and address transfer, four DQ signals used during data transfer. All phases are SDR.
 4. 1S-4S-4S: One DQ signal used during command transfer, four DQ signals used during address transfer, and data transfer. All phases are SDR.
 5. 1S-4D-4D: One DQ signal used during command transfer at SDR, four DQ signals used during address and data transfer at DDR.
 6. 4S-4S-4S: Four DQ signals used during command transfer, address transfer, and data transfer. All phases are SDR.

7. 4S-4D-4D: Four DQ signals used during command transfer at SDR, four DQ signals used during address and data transfer at DDR.

- Each transaction begins with an 8-bit (1-byte) command. The command selects the type of information transfer or device operation to be performed.
- All protocols supports 3 or 4-byte addressing.

1S-1S-1S protocol (single input/output, SIO)

- The 1S-1S-1S mode is the preferred default protocol following Power-on-Reset (POR), but flash devices can be configured to reset into the Quad mode.
- This protocol uses DQ[0]/SI to transfer information from host to flash device and DQ[1]/SO to transfer information from flash device to host. On each DQ, information is placed on the DQ line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each byte. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.
- In 1S-1S-1S, DQ[3:2] are not used for data transfer period. DQ[2] can be used as a WP# and DQ[3] can be used as a RESET# input. Otherwise, the DQ[3:2] signals will be high impedance.

1S-2S-2S protocol (dual input/output, DIO)

- This protocol uses DQ[1:0] signals. The 8-bit command placed on the DQ[0] in MSb to LSb order. The LSb of address byte is placed on DQ[0] with next order bit on DQ[1] signal and so on. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order.
- In 1S-2S-2S, DQ[3:2] are not used for data transfer period. DQ[2] can be used as a WP# and DQ[3] can be used as a RESET# input. Otherwise, the DQ[3:2] signals will be high impedance.

1S-1S-4S protocol (quad output read, QOR)

- This protocol uses DQ[3:0] signals. The 8-bit command and address placed on the DQ[0] in MSb to LSb order. Sequential data bytes in SDR are transferred in lowest address to highest address order.

1S-4S-4S and 1S-4D-4D protocol (quad input/output, QIO)

- This protocol uses DQ[3:0] signals. The 8-bit command placed on the DQ[0] in MSb to LSb order. The LSb of address byte is placed on DQ[0] with each higher order bit on the successively higher numbered DQ signals. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. Sequential data bytes in DDR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order.

4S-4S-4S and 4S-4D-4D protocol (quad peripheral interface, QPI)

- This protocol uses DQ[3:0] signals. The LSb of each byte is placed on DQ[0] with each higher order bit on the successively higher numbered DQ signals. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. Sequential data bytes in DDR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order. [Serial peripheral interface \(SPI, 1S-1S-1S\) on page 13](#) through [Quad peripheral interface \(QPI, 4S-4S-4S and 4S-4D-4D\)](#) show all transaction formats by protocol mode.

2.3.1 Serial peripheral interface (SPI, 1S-1S-1S)

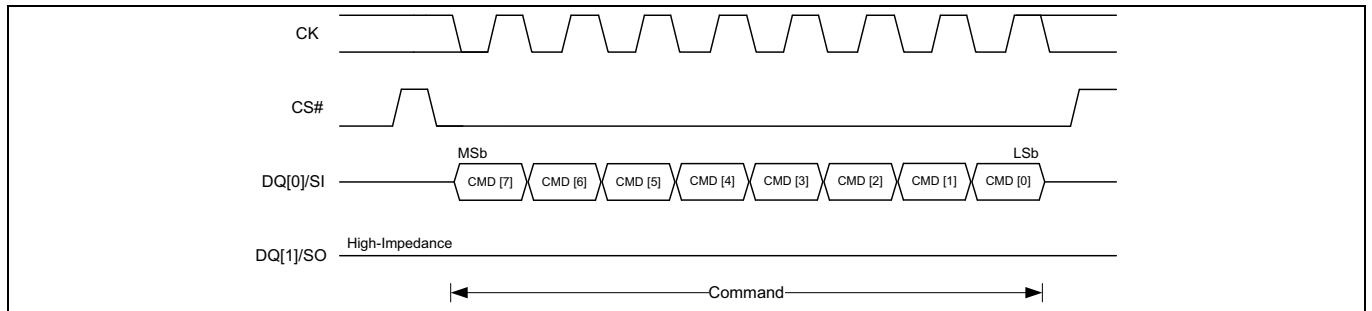


Figure 7 SPI transaction with command input

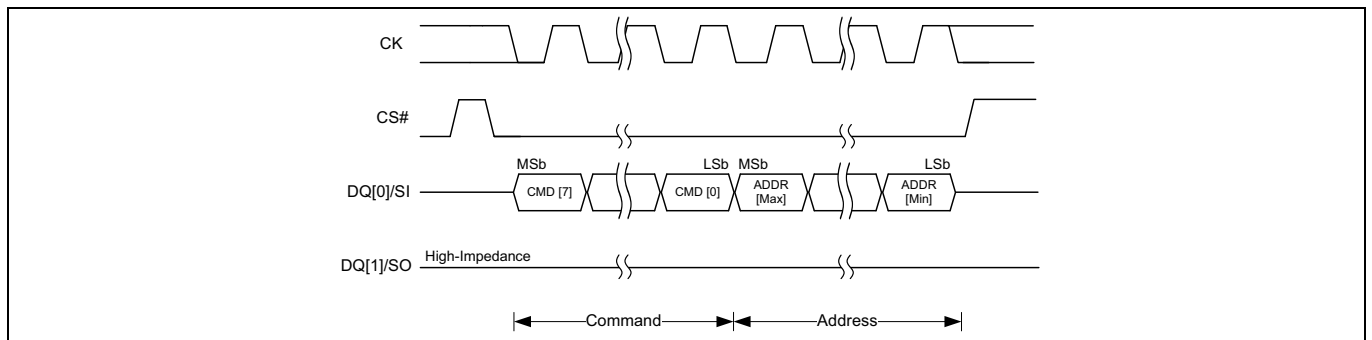


Figure 8 SPI transaction with command and address input

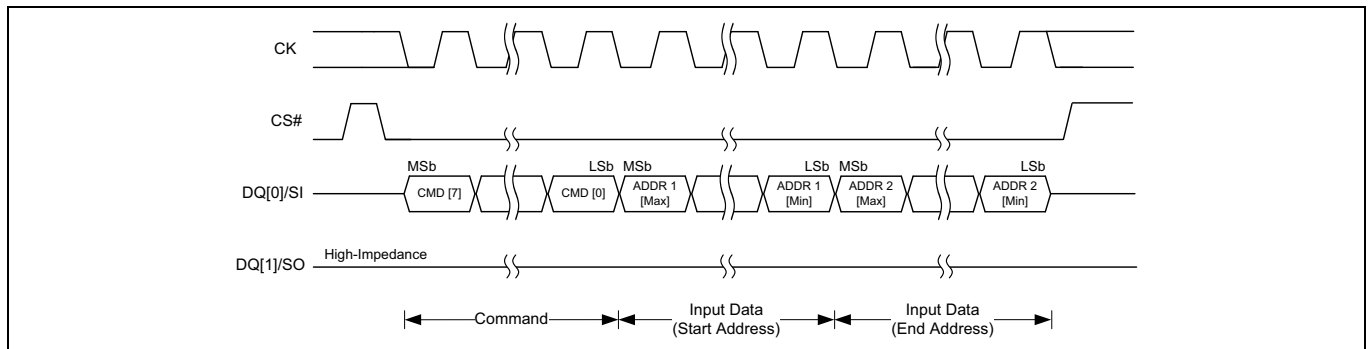


Figure 9 SPI transaction with command and two input addresses

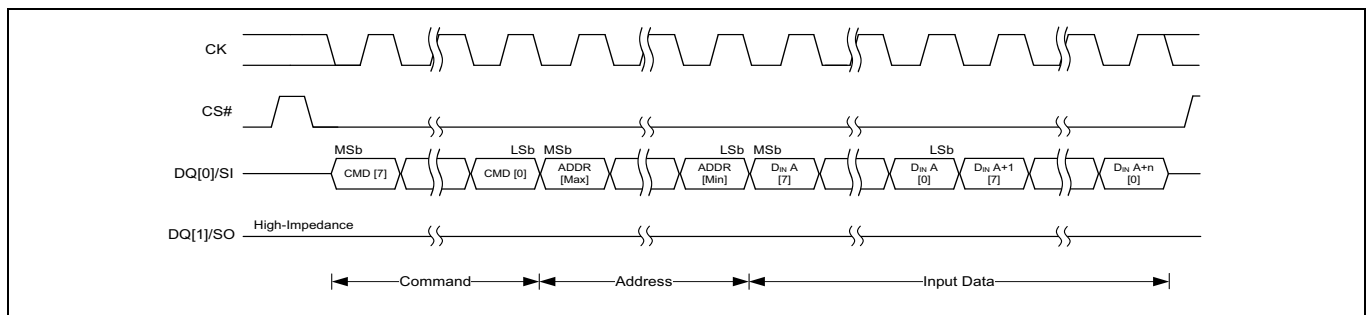


Figure 10 SPI program transaction with command, address, and data input

Interface overview

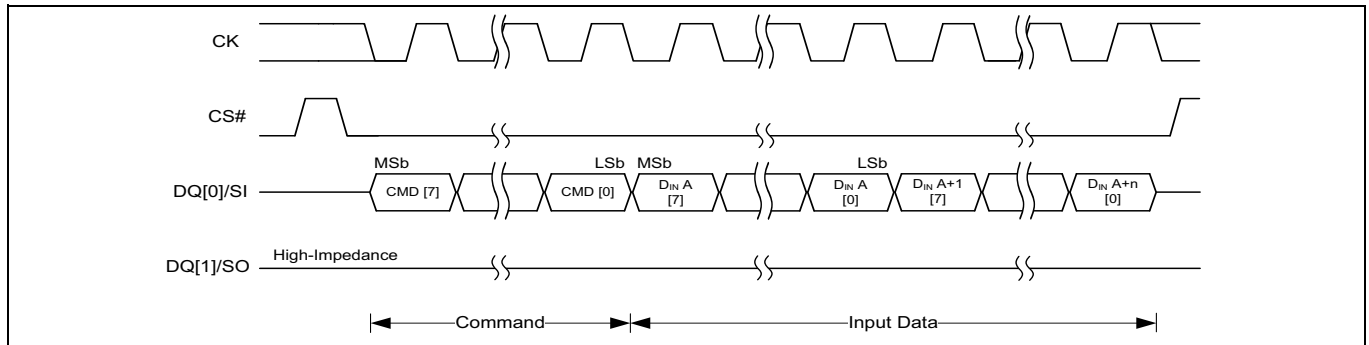


Figure 11 SPI program transaction with command and data input

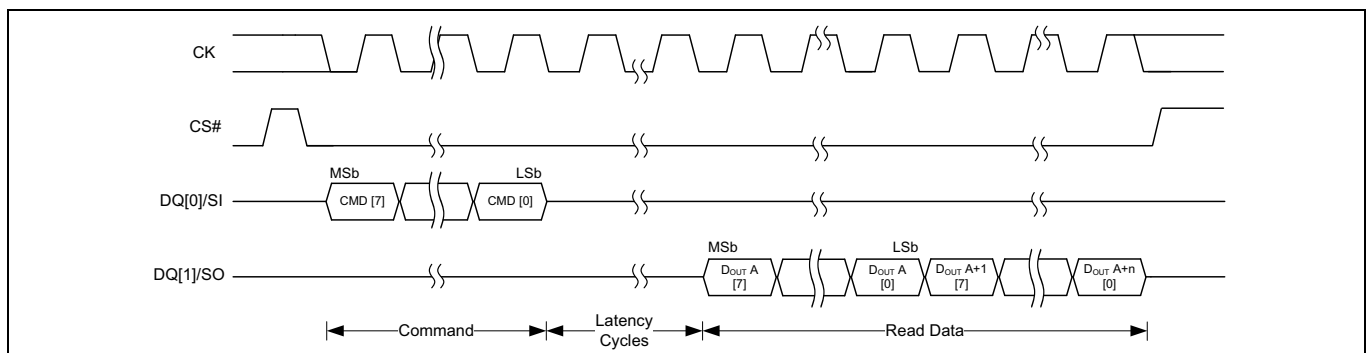


Figure 12 SPI read transaction with command input (output latency)^[2, 3]

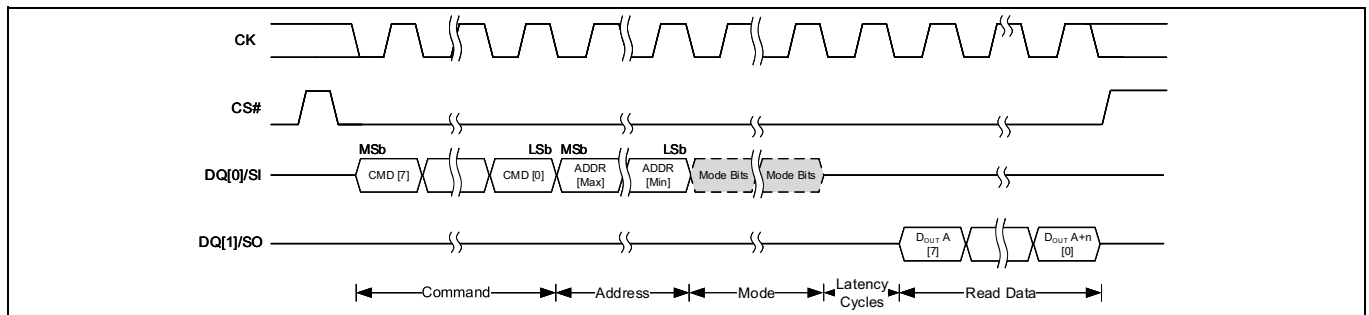


Figure 13 SPI read transaction with command and address input (output latency)^[4]

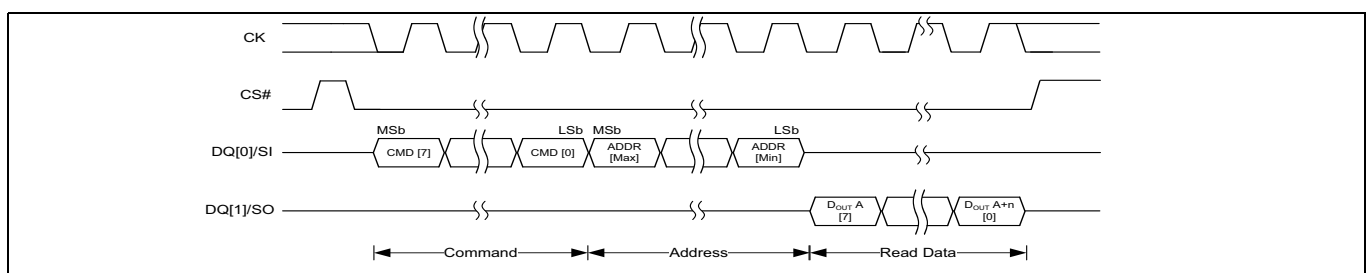


Figure 14 SPI read transaction with command and address input (no output latency)

Notes

2. In case of Status Register 1 and 2, Read Byte data out is the updated status.
3. In case of Data Learning Pattern Read, each byte outputs the DLP.
4. In case of RDAY2_4_0 transaction, the host must provide the mode bits.

Interface overview

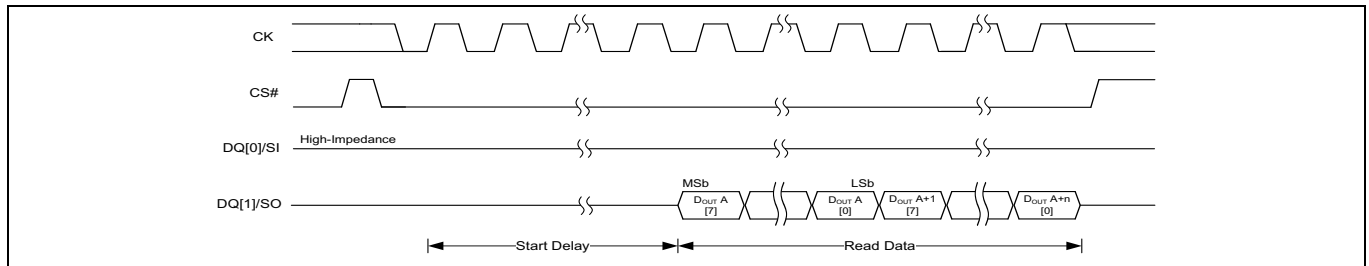


Figure 15 SPI transaction with output data sequence (AutoBoot)

2.3.2 Dual IO SPI (DIO, 1S-2S-2S)

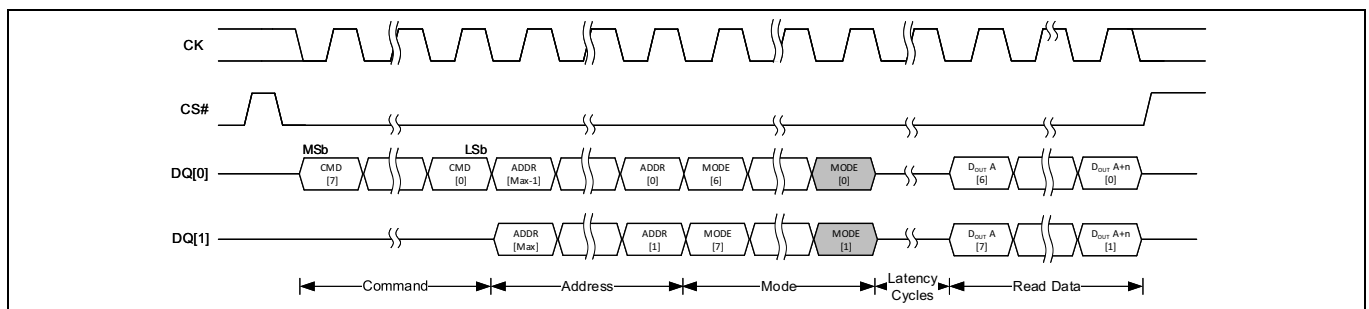


Figure 16 DIO read transaction with command, address, and mode input (output latency)

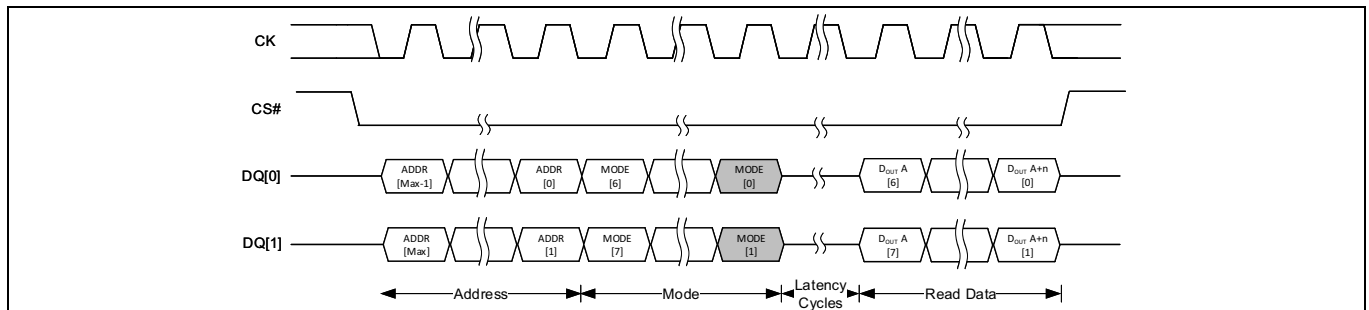


Figure 17 DIO continuous read transaction with address and mode input (output latency)

2.3.3 QUAD output read SPI (QOR, 1S-1S-4S)

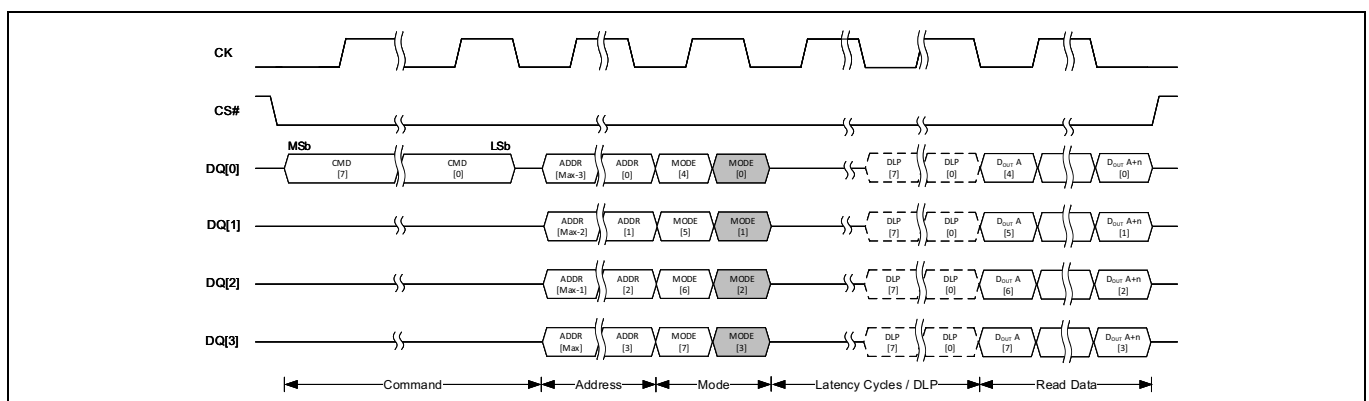


Figure 18 QOR SDR read transaction with command, address, and mode input (output latency)

2.3.4 QUAD IO SPI (QIO, 1S-4S-4S, 1S-4D-4D)

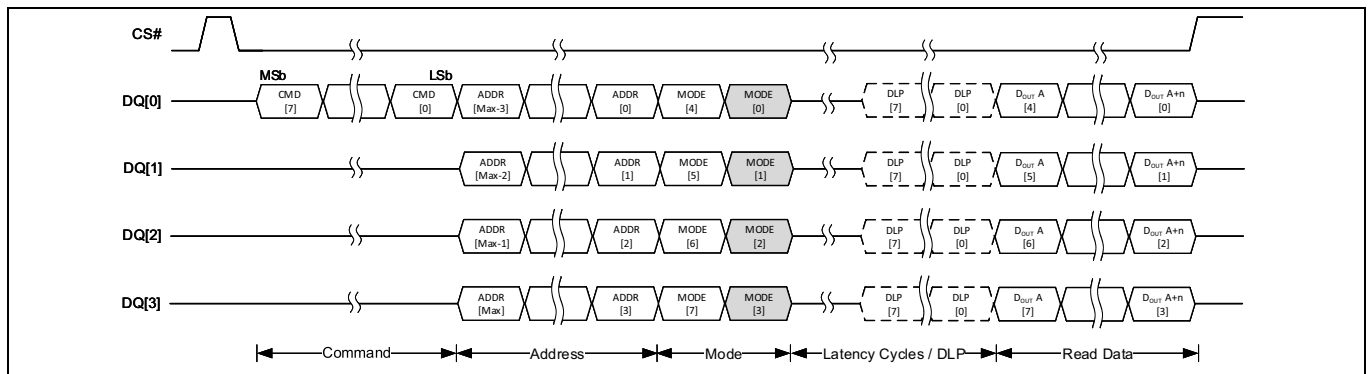


Figure 19 QIO SDR read transaction with command, address, and mode input (output latency)^[5]

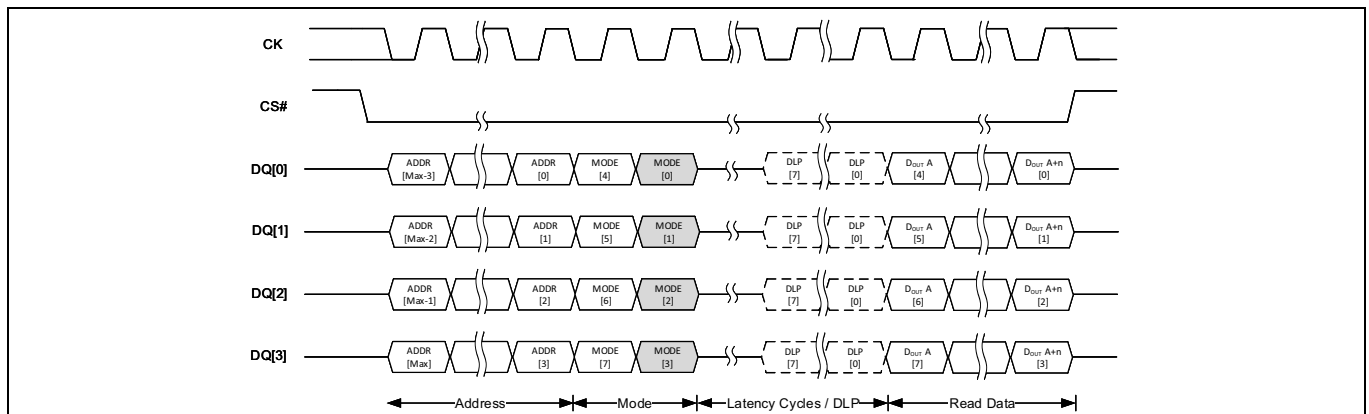


Figure 20 QIO SDR continuous read transaction with address and mode input (output latency)^[5]

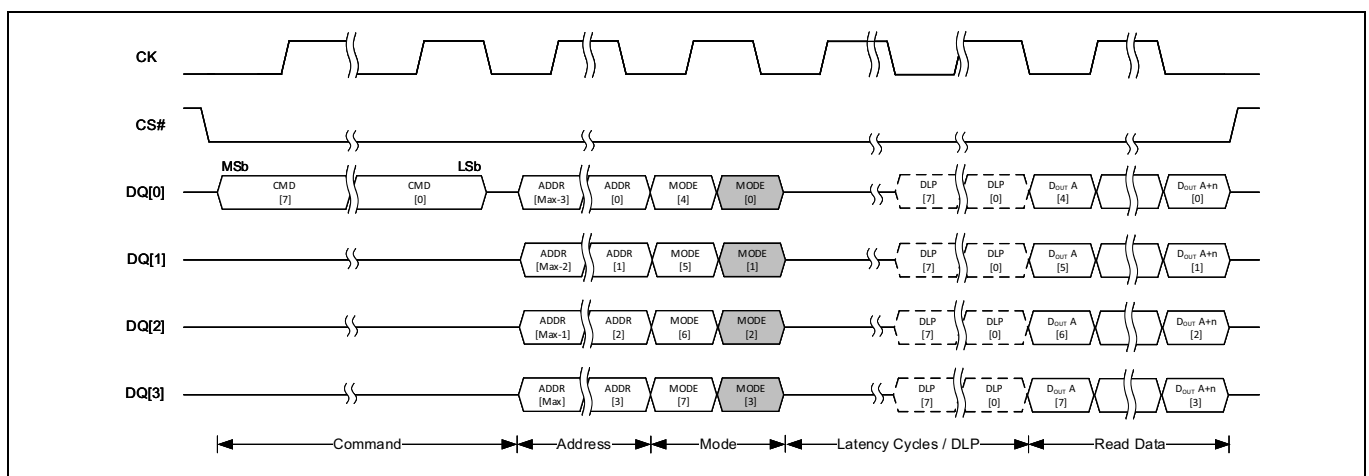


Figure 21 QIO DDR read transaction with command, address, and mode input (output latency)

Note

5. The gray bits data is don't care.

Interface overview

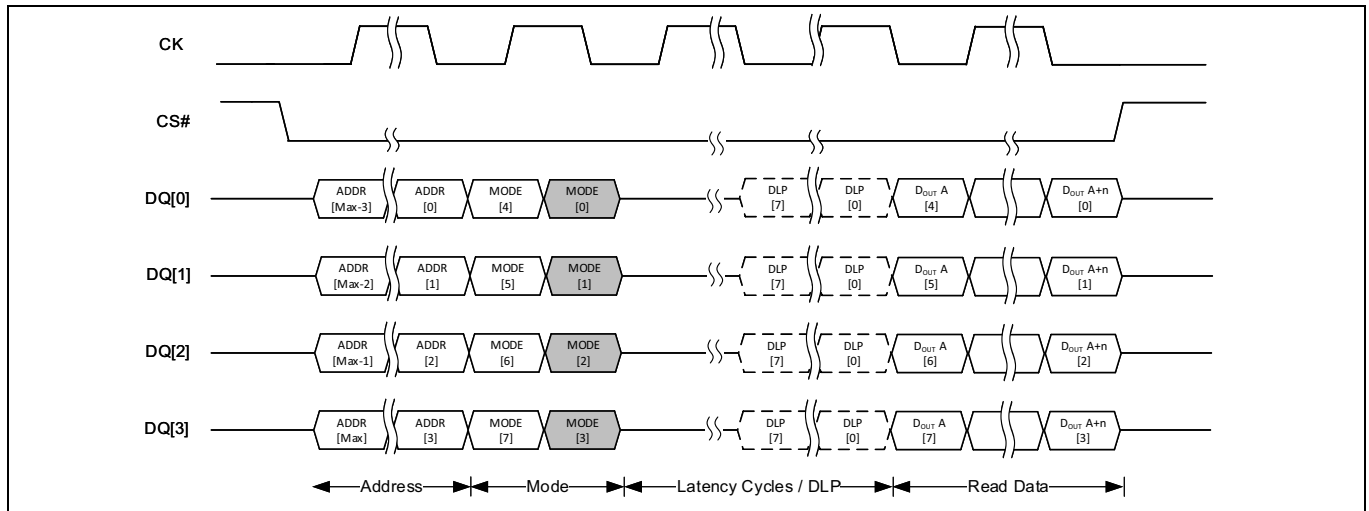


Figure 22 QIO DDR continuous read transaction with address and mode input (output latency)

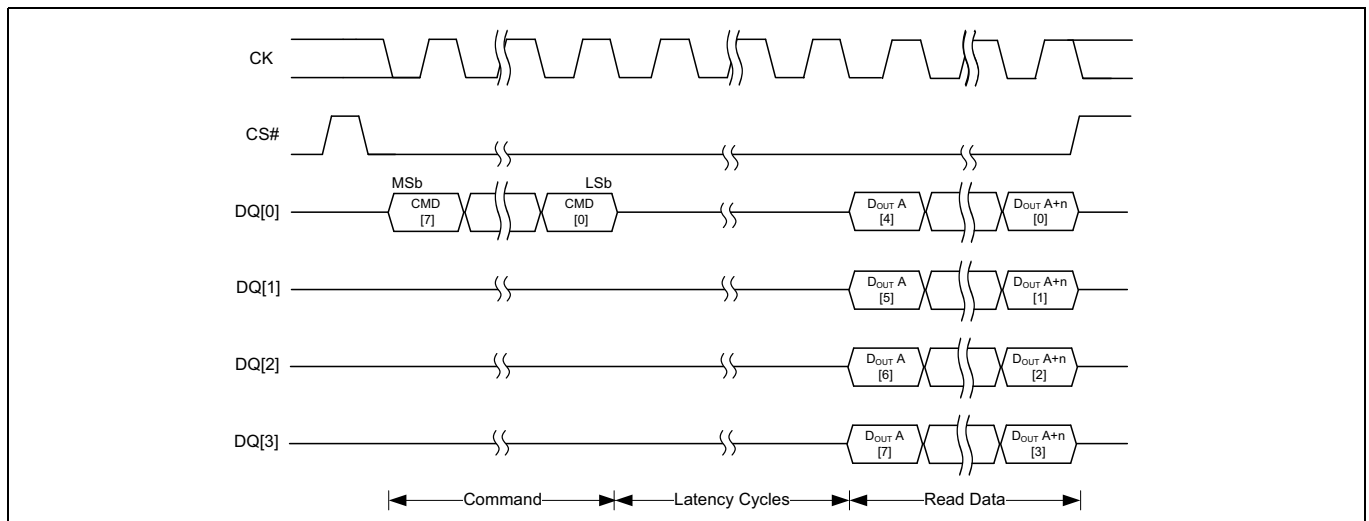


Figure 23 Quad ID read transaction with command input (output latency)

2.3.5 Quad peripheral interface (QPI, 4S-4S-4S and 4S-4D-4D)

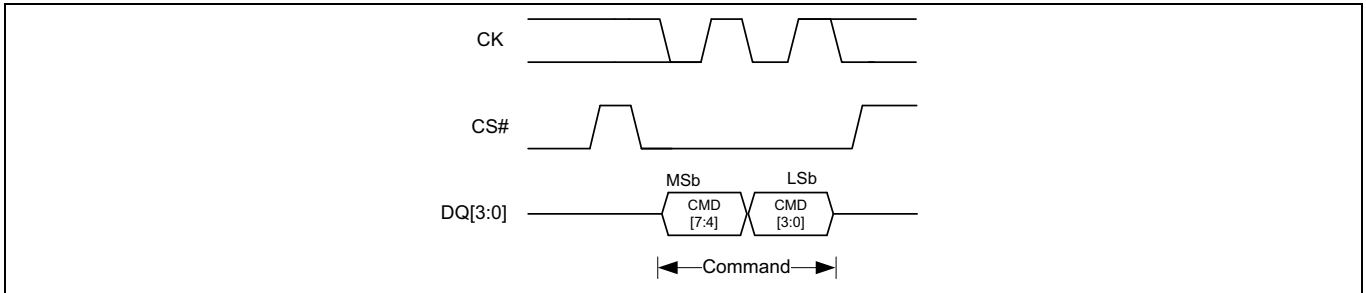


Figure 24 QPI SDR transaction with command input

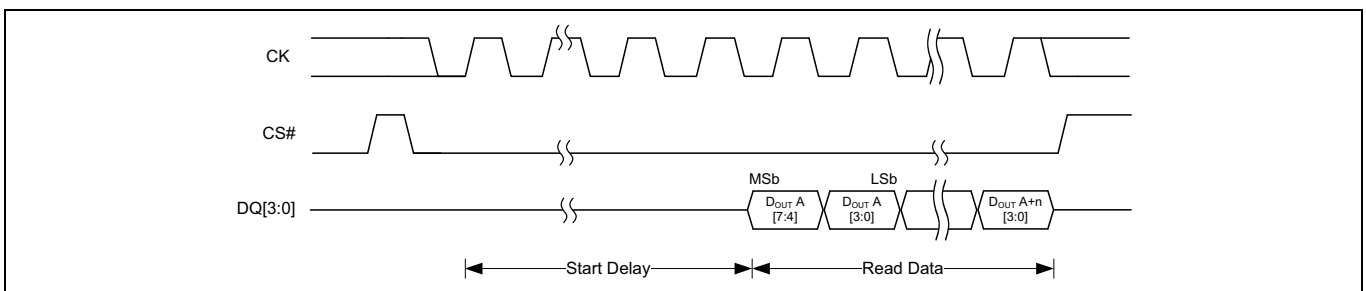


Figure 25 QPI transaction with output data sequence (AutoBoot)

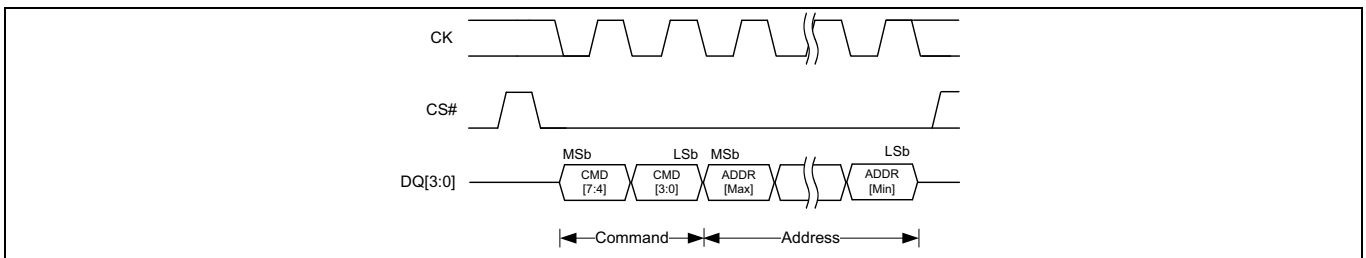


Figure 26 QPI SDR transaction with command and address input

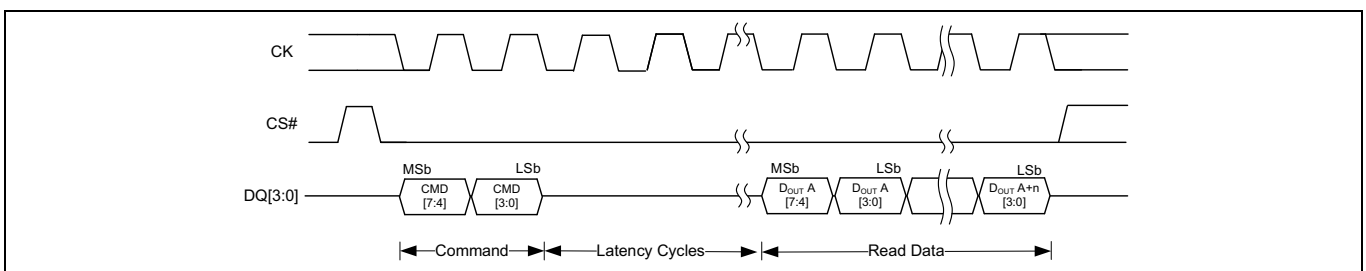


Figure 27 QPI SDR read transaction with command input (output latency)

Interface overview

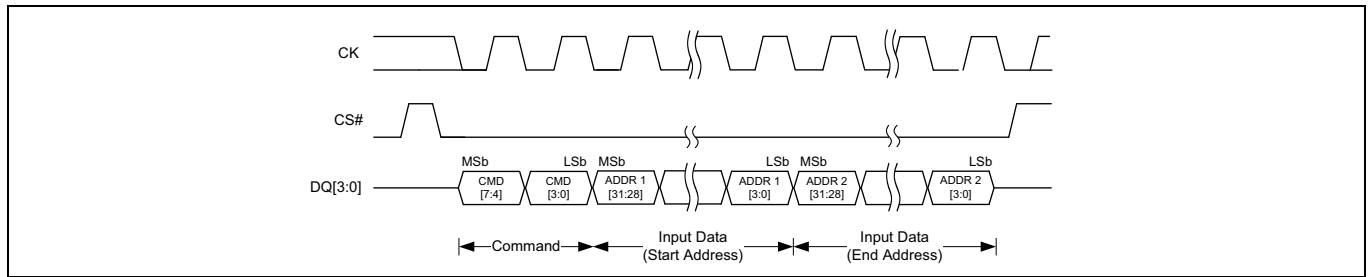


Figure 28 QPI SDR transaction with command and two addresses input

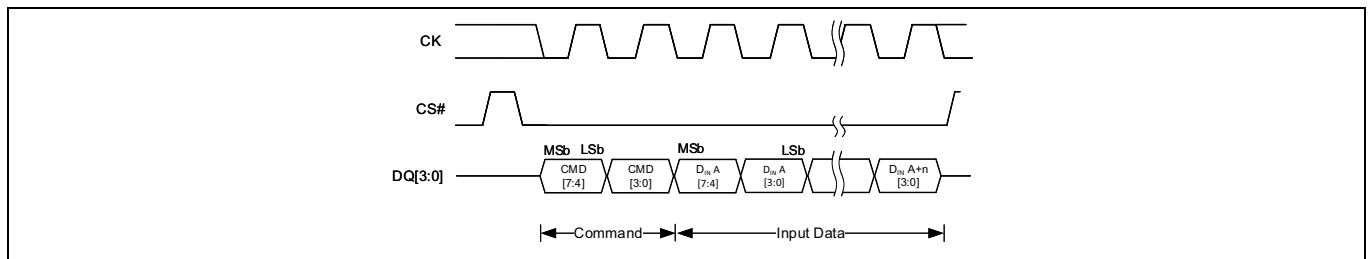


Figure 29 QPI SDR transaction with command and data input

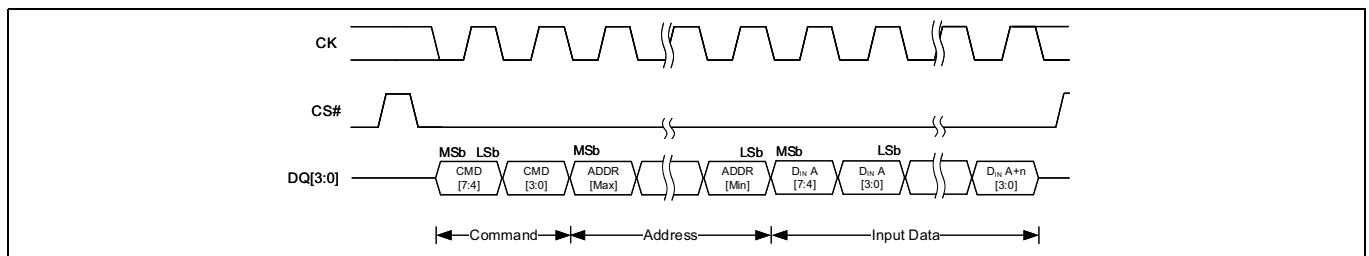


Figure 30 QPI SDR program transaction with command, address, and data input

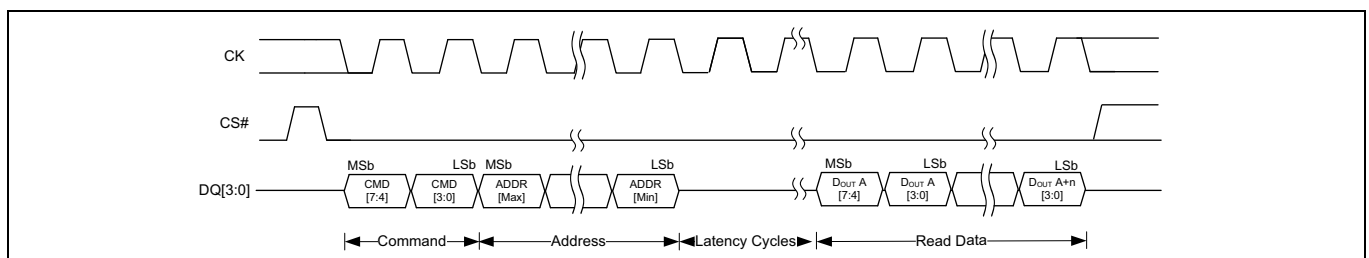


Figure 31 QPI SDR read transaction with command and address input (output latency)

Note

6. The gray bits data is don't care.

Interface overview

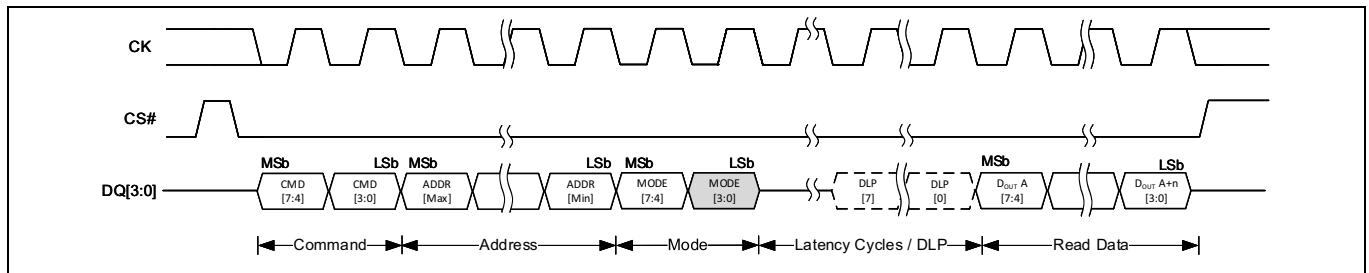


Figure 32 QPI SDR read transaction with command, address, and mode input (output latency)^[6]

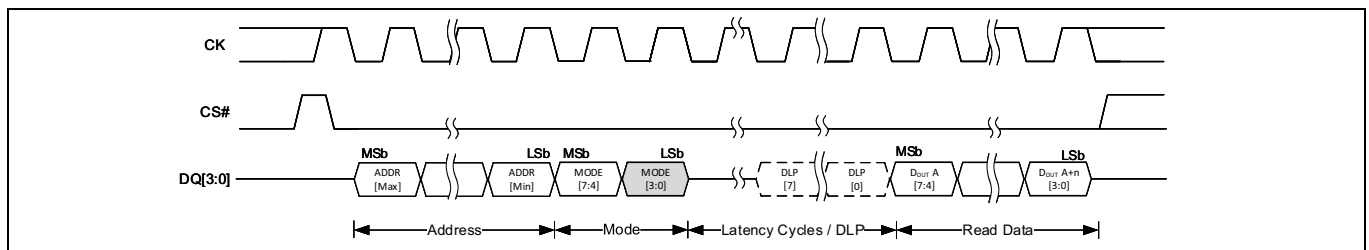


Figure 33 QPI SDR continuous read transaction with address and mode input (output latency)^[6]

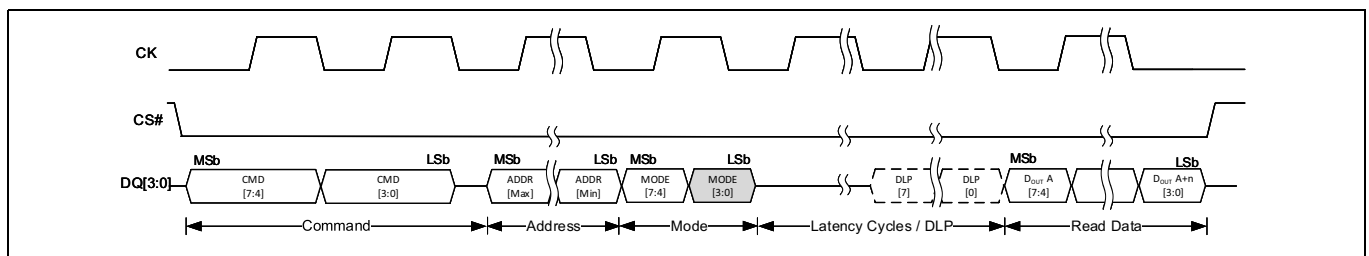


Figure 34 QPI DDR read transaction with command, address, and mode input (output latency)^[6]

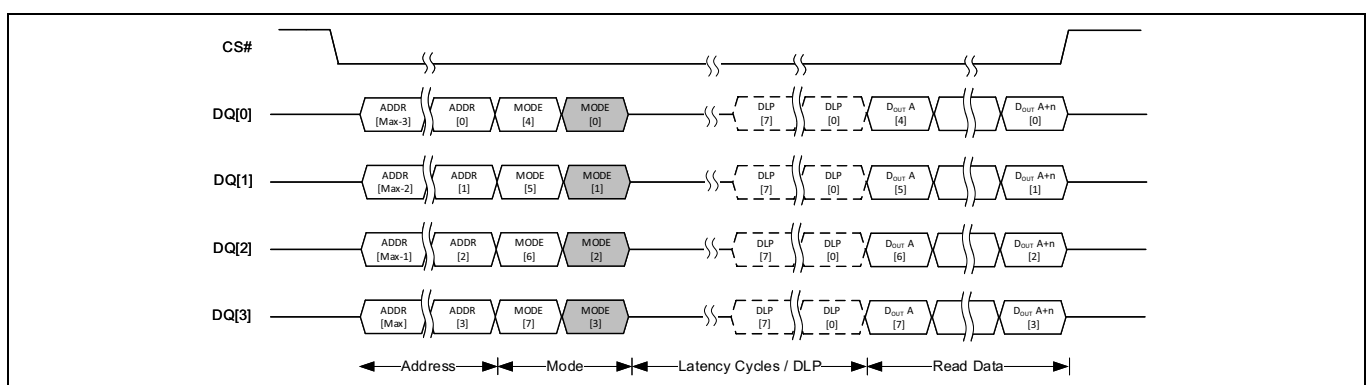


Figure 35 QPI DDR continuous read transaction with address and mode input (output latency)^[7]

Note

7. The gray bits data is don't care.

2.4 Register naming convention

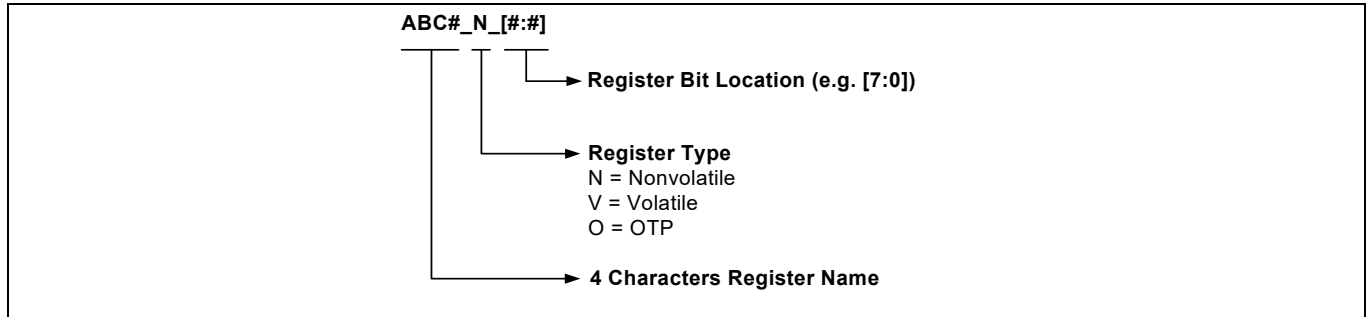


Figure 36 Register naming convention

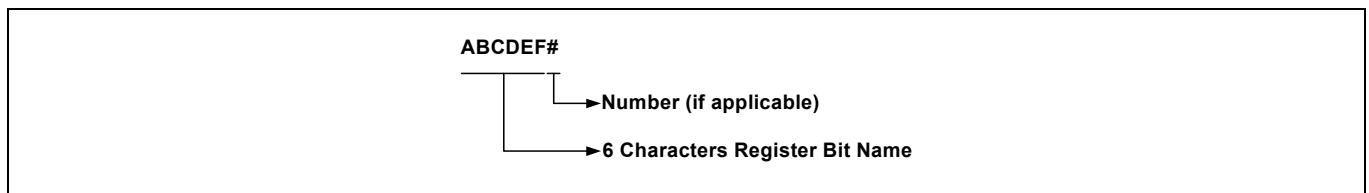


Figure 37 Register bit naming convention

2.5 Transaction naming convention

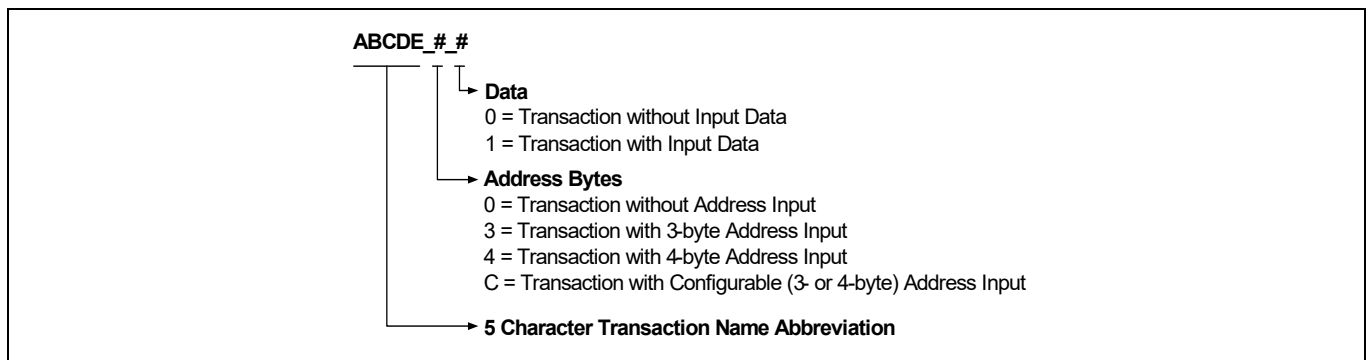


Figure 38 Transaction naming convention

3 Address space maps

The HL-T/HS-T family supports 24-bit as well as 32-bit (4-Byte) addresses, to enable 256Mb or 512Mb or 1Gb density devices. 4-Byte addresses allow direct addressing of up to 4GB (32Gb) address space. The address byte option can be changed by writing the respective configuration registers OR there are separate transactions also available to enter (EN4BA_0_0) and exit (EX4BA_0_0) the 4-byte address mode.

Besides flash memory array, HL-T/HS-T family includes separate address spaces for Manufacturer ID, Device ID, Unique ID, Serial Flash Discoverable Parameters (SFDP), Secure Silicon Region (SSR), and Registers.

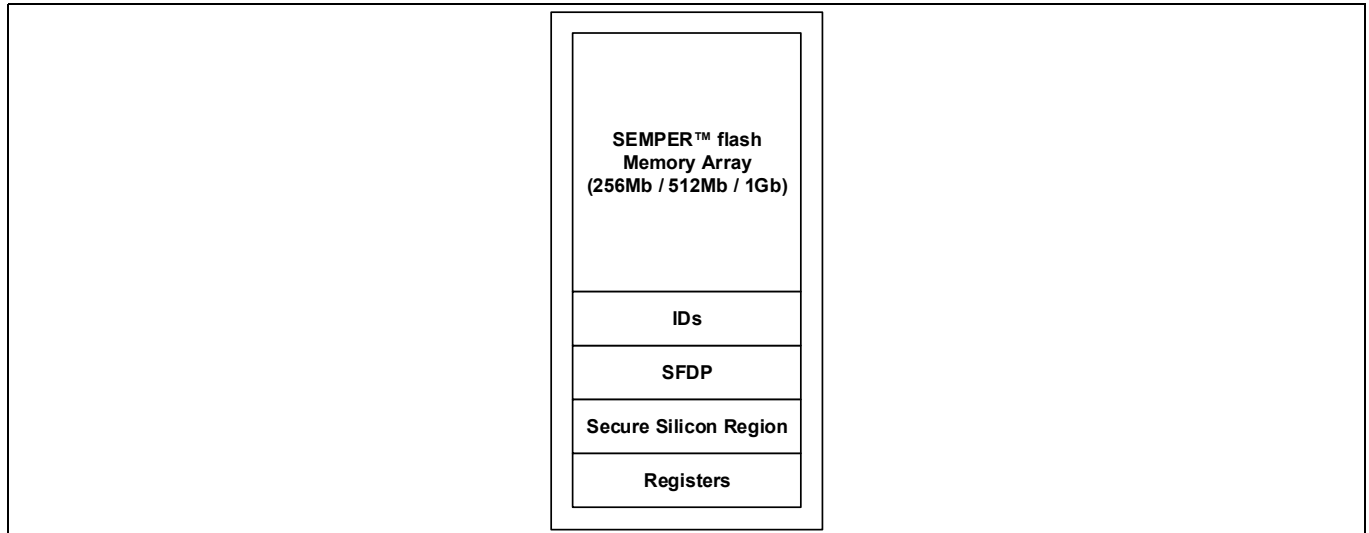


Figure 39 HL-T/HS-T address space map overview

3.1 SEMPER™ Flash memory array

The main flash array is divided into units called physical sectors.

The HL-T/HS-T family sector architecture supports the following options:

- 256Mb, 512Mb, 1Gb supports 256KB Uniform sector options
- 256Mb, 512Mb, 1Gb Hybrid sector options
 - Physical set of thirty-two 4KB sectors and one 128KB sector at the top or bottom of address space with all remaining sectors of 256KB
 - Physical set of sixteen 4KB sectors and one 192KB sector at both the top and bottom of the address space with all remaining sectors of 256KB

The combination of the sector architecture selection bits in Configuration Register-1 and Configuration Register-3 support the different sector architecture options of the HL-T/HS-T family. See [Registers on page 72](#) for more information.

Table 2 256KB uniform sector address map^[8]

| Sector size (KB) | S25HL01GT and S25HS01GT | | | S25HL512T and S25HS512T | | | S25HL256T and S25HS256T | | |
|------------------|-------------------------|--------------|--|-------------------------|--------------|--|-------------------------|--------------|--|
| | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - Sector ending address) |
| 256 | 512 | SA00 | 00000000h-0003FFFFh | 256 | SA00 | 00000000h-0003FFFFh | 128 | SA00 | 00000000h-0003FFFFh |
| | | : | : | | : | : | | | |
| | | SA511 | 07FC0000h-07FFFFFFh | | SA255 | 03FC0000h-03FFFFFFh | | SA127 | 01FC0000h-01FFFFFFh |

Note
 8. Configuration: CFR3N[3] = 1.

Address space maps

Table 3 Bottom hybrid configuration 1 thirty-two 4KB sectors and 256KB uniform sectors address map^[9]

| Sector size (KB) | S25HL01GT and S25HS01GT | | | S25HL512T and S25HS512T | | | S25HL256T and S25HS 256T | | |
|------------------|-------------------------|--------------|--|-------------------------|--------------|--|--------------------------|--------------|--|
| | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) |
| 4 | 32 | SA00 | 00000000h-00000FFFh | 32 | SA00 | 00000000h-00000FFFh | 32 | SA00 | 00000000h-00000FFFh |
| | | : | : | | : | : | | | |
| | | SA31 | 0001F000h-0001FFFFh | | SA31 | 0001F000h-0001FFFFh | | SA31 | 0001F000h-0001FFFFh |
| 128 | 1 | SA32 | 00020000h-0003FFFFh | 1 | SA32 | 00020000h-0003FFFFh | 1 | SA32 | 00020000h-0003FFFFh |
| 256 | 511 | SA33 | 00040000h-0007FFFFh | 255 | SA33 | 00040000h-0007FFFFh | 127 | SA33 | 00040000h-0007FFFFh |
| | | : | : | | : | : | | | |
| | | SA543 | 07FC0000h-07FFFFFFh | | SA287 | 03FC0000h-03FFFFFFh | | SA159 | 01FC0000h-01FFFFFFh |

Note

9. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 0.

Table 4 Top hybrid configuration 1 thirty-two 4KB sectors and 256KB uniform sectors address map^[10]

| Sector size (KB) | S25HL01GT and S25HS01GT | | | S25HL512T and S25HS512T | | | S25HL256T and S25HS256T | | |
|------------------|-------------------------|--------------|--|-------------------------|--------------|--|-------------------------|--------------|--|
| | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) |
| 256 | 511 | SA00 | 00000000h-0003FFFFh | 255 | SA00 | 00000000h-0003FFFFh | 127 | SA00 | 00000000h-0003FFFFh |
| | | : | : | | : | : | | | |
| | | SA510 | 07F80000h-07FBFFFFh | | SA254 | 03F80000h-03FBFFFFh | | SA126 | 01F80000h-01FBFFFFh |
| 128 | 1 | SA511 | 07FC0000h-07FDFFFFh | 1 | SA255 | 03FC0000h-03FDFFFFh | 1 | SA127 | 01FC0000h-01FDFFFFh |
| 4 | 32 | SA512 | 07FE0000h-07FE0FFFh | 32 | SA256 | 03FE0000h-03FE0FFFh | 32 | SA128 | 01FE0000h-01FE0FFFh |
| | | : | : | | : | : | | | |
| | | SA543 | 07FFF000h-07FFFFFFh | | SA287 | 03FFF000h-03FFFFFFh | | SA159 | 01FFF000h-01FFFFFFh |

Note

10. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 1.

Table 5 Hybrid configuration 2 bottom sixteen and top sixteen 4KB sectors address map^[11]

| Sector size (KB) | S25HL01GT and S25HS01GT | | | S25HL512T and S25HS512T | | | S25HL256T and S25HS256T | | |
|------------------|-------------------------|--------------|--|-------------------------|--------------|--|-------------------------|--------------|--|
| | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) | Sector count | Sector range | Byte address range (sector starting address - sector ending address) |
| 4 | 16 | SA00 | 00000000h-00000FFFh | 16 | SA00 | 00000000h-00000FFFh | 16 | SA00 | 00000000h-00000FFFh |
| | | : | : | | : | : | | | |
| | | SA15 | 0000F000h-0000FFFFh | | SA15 | 0000F000h-0000FFFFh | | SA15 | 0000F000h-0000FFFFh |
| 192 | 1 | SA16 | 00010000h-0003FFFFh | 1 | SA16 | 00010000h-0003FFFFh | 1 | SA16 | 00010000h-0003FFFFh |
| 256 | 510 | SA17 | 00040000h-0007FFFFh | 254 | SA17 | 00040000h-0007FFFFh | 126 | SA17 | 00040000h-0007FFFFh |
| | | : | : | | : | : | | | |
| | | SA526 | 07F80000h-07FBFFFFh | | SA270 | 03F80000h-03FBFFFFh | | SA142 | 01F80000h-01FBFFFFh |
| 192 | 1 | SA527 | 07FC0000h-07FEFFFFh | 1 | SA271 | 03FC0000h-03FEFFFFh | 1 | SA143 | 01FC0000h-01FEFFFFh |
| 4 | 16 | SA528 | 07FF0000h-07FF0FFFh | 16 | SA272 | 03FF0000h-03FF0FFFh | 16 | SA144 | 01FF0000h-01FF0FFFh |
| | | : | : | | : | : | | | |
| | | SA543 | 07FFF000h-07FFFFFFh | | SA287 | 03FFF000h-03FFFFFFh | | SA159 | 01FFF000h-01FFFFFFh |

Note

11. Configuration: CFR3N[3] = 0, CFR1N[6] = 1.

These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4KB sectors have the pattern xxxxx000h-xxxxxFFFh. All 256KB sectors have the pattern xxx00000h-xxx3FFFFh, xxx40000h-xxx7FFFFh, xx80000h-xxxCFFFFh, or xxD0000h-xxxFFFFFh.

3.2 ID address space

This particular region of the memory is assigned to manufacturer, device, and unique identification:

- The manufacturer identification is assigned by JEDEC (see [Table 89](#)).
- The device identification is assigned by CYPRESS™ (see [Table 89](#)).
- A 64-bit unique number is located in 8 bytes of the Unique Device ID address space. This Unique ID can be used as a software readable serial number that is unique for each device (see [Table 90](#)).

There is no address space defined for these IDs as they can be read by providing the respective transactions only. The transactions do not need the address to read these IDs. The data in this address space is read-only data.

3.3 JEDEC JESD216 serial flash discoverable parameters (SFDP) space

The SFDP standard provides a consistent method of describing the functional and feature capabilities of this serial flash device in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features. The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. The SFDP address space is programmed by CYPRESS™ and read-only for the host system (see [Table 85](#) through [Table 88](#)).

Table 6 SFDP overview address map

| Byte address | Description |
|--------------|--|
| 0000h | Location zero within JEDEC JESD216D SFDP space - start of SFDP header |
| ... | Remainder of SFDP header followed by undefined space |
| 0100h | Start of SFDP parameter tables The SFDP parameter table data starting at 0100h |
| ... | Remainder of SFDP parameter tables followed by either more parameters or undefined space |

3.4 SSR address space

Each HS/L-T family memory device has a 1024-byte Secure Silicon Region which is OTP address space. This address space is separate from the main flash array. The SSR area is divided into 32 individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The 16 lowest bytes contain a 128-bit random number. The random number cannot be written to, erased or programmed and any attempts will return an PRGERR flag.
- The next four bytes are used to provide one bit per secure region (32 bits in total) to permanently protect once set to “0” from writing, erasing or programming.
- All other bytes are reserved.

The remaining regions are erased when shipped from CYPRESS™, and are available for programming of additional permanent data.

Address space maps

Table 7 SSR address map

| Region | Byte address range | Contents | Initial delivery state |
|-----------|--------------------|---|-----------------------------------|
| Region 0 | 000h | LSB of CYPRESS™ Programmed Random Number | CYPRESS™ Programmed Random Number |
| | ... | ... | |
| | 00Fh | MSB of CYPRESS™ Programmed Random Number | |
| | 010h to 013h | Region Locking Bits Byte 10h [bit 0] locks region 0 from programming when = 0 ... Byte 13h [bit 7] locks region 31 from programming when = 0 | All Bytes = FFh |
| | 014h to 01Fh | Reserved for future use (RFU) | All Bytes = FFh |
| Region 1 | 020h to 03Fh | Available for User Programming | All Bytes = FFh |
| Region 2 | 040h to 05Fh | Available for User Programming | All Bytes = FFh |
| ... | ... | Available for User Programming | All Bytes = FFh |
| Region 31 | 3E0h to 3FFh | Available for User Programming | All Bytes = FFh |

3.5 Registers

Registers are small groups of memory cells used to configure how the HS/L-T family memory device operates, or to report the status of device operations. The registers are accessed by specific commands and addresses.

Table 8 shows the address map for every available register in this flash memory device.

Table 8 Register address map

| Function | Register type | Register name | Volatile component address (hex) | Nonvolatile component address (hex) |
|---------------------------------------|---|------------------------|----------------------------------|-------------------------------------|
| Device Status | Status Register 1 | STR1N[7:0], STR1V[7:0] | 0x00800000 | 0x00000000 |
| | Status Register 2 | STR2V[7:0] | 0x00800001 | N/A |
| Device Configuration | Configuration Register 1 | CFR1N[7:0], CFR1V[7:0] | 0x00800002 | 0x00000002 |
| | Configuration Register 2 | CFR2N[7:0], CFR2V[7:0] | 0x00800003 | 0x00000003 |
| | Configuration Register 3 | CFR3N[7:0], CFR3V[7:0] | 0x00800004 | 0x00000004 |
| | Configuration Register 4 | CFR4N[7:0], CFR4V[7:0] | 0x00800005 | 0x00000005 |
| Infineon® Endurance Flex architecture | Infineon® Endurance Flex architecture Selection Register 0 [1:0] | EFX00[1:0] | N/A | 0x00000050 |
| | Infineon® Endurance Flex architecture Selection Register 1 [7:0] | EFX10[7:0] | | 0x00000052 |
| | Infineon® Endurance Flex architecture Selection Register 1 [10:8] | EFX10[10:8] | | 0x00000053 |
| | Infineon® Endurance Flex architecture Selection Register 2 [7:0] | EFX20[7:0] | | 0x00000054 |
| | Infineon® Endurance Flex architecture Selection Register 2 [10:8] | EFX20[10:8] | | 0x00000055 |
| | Infineon® Endurance Flex architecture Selection Register 3 [7:0] | EFX30[7:0] | | 0x00000056 |
| | Infineon® Endurance Flex architecture Selection Register 3 [10:8] | EFX30[10:8] | | 0x00000057 |
| | Infineon® Endurance Flex architecture Selection Register 4 [7:0] | EFX40[7:0] | | 0x00000058 |
| | Infineon® Endurance Flex architecture Selection Register 4 [10:8] | EFX40[10:8] | 0x00000059 | |
| Error Correction | ECC Status Register | ESCV[7:0] | 0x00800089 | N/A |
| | ECC Error Detection Count Register [7:0] | ECTV[7:0] | 0x0080008A | |
| | ECC Error Detection Count Register [15:8] | ECTV[15:8] | 0x0080008B | |
| | ECC Address Trap Register [7:0] | EATV[7:0] | 0x0080008E | |
| | ECC Address Trap Register [15:8] | EATV[15:8] | 0x0080008F | |
| | ECC Address Trap Register [23:16] | EATV[23:16] | 0x00800040 | |
| | ECC Address Trap Register [31:24] | EATV[31:24] | 0x00800041 | |

Address space maps

Table 8 Register address map (continued)

| Function | Register type | Register name | Volatile component address (hex) | Nonvolatile component address (hex) |
|-------------------------------|---|---------------------|----------------------------------|-------------------------------------|
| AutoBoot | AutoBoot Register [7:0] | ATBN[7:0] | N/A | 0x00000042 |
| | AutoBoot Register [15:8] | ATBN[15:8] | | 0x00000043 |
| | AutoBoot Register [23:16] | ATBN[23:16] | | 0x00000044 |
| | AutoBoot Register [31:24] | ATBN[31:24] | | 0x00000045 |
| Data Learning | Data Learning Register [7:0] | DLPN[7:0],DLPV[7:0] | 0x00800010 | 0x00000010 |
| Erase Count | Sector Erase Count Register [7:0] | SECV[7:0] | 0x00800091 | N/A |
| | Sector Erase Count Register [15:8] | SECV[15:8] | 0x00800092 | |
| | Sector Erase Count Register [23:16] | SECV[23:16] | 0x00800093 | |
| Data Integrity Check | Data Integrity Check CRC Register [7:0] | DCRV[7:0] | 0x00800095 | |
| | Data Integrity Check CRC Register [15:8] | DCRV[15:8] | 0x00800096 | |
| | Data Integrity Check CRC Register [23:16] | DCRV[23:16] | 0x00800097 | |
| | Data Integrity Check CRC Register [31:24] | DCRV[31:24] | 0x00800098 | |
| Protection and Security | Advanced Sector Protection Register [7:0] | ASPO[7:0] | N/A | 0x00000030 |
| | Advanced Sector Protection Register [15:8] | ASPO[15:8] | | 0x00000031 |
| | ASP PPB Lock Register (Persistent Protection Block) | PPLV[7:0] | 0x0080009B | N/A |
| | ASP Password Register [7:0] | PWDO[7:0] | N/A | 0x00000020 |
| | ASP Password Register [15:8] | PWDO[15:8] | | 0x00000021 |
| | ASP Password Register [23:16] | PWDO[23:16] | | 0x00000022 |
| | ASP Password Register [31:24] | PWDO[31:24] | | 0x00000023 |
| | ASP Password Register [39:32] | PWDO[39:32] | | 0x00000024 |
| | ASP Password Register [47:40] | PWDO[47:40] | | 0x00000025 |
| | ASP Password Register [55:48] | PWDO[55:48] | | 0x00000026 |
| ASP Password Register [63:56] | PWDO[63:56] | 0x00000027 | | |

4 Features

4.1 Error detection and correction

HL-T/HS-T family devices support error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for error detection and correction during read operations. The ECC is based on a 16-byte data unit. When the 16-byte data unit is loaded into the Program Buffer and is transferred to the 128-bits flash memory array Line for programming (after an erase), an 8-bit ECC for each data unit is also programmed into a portion of the memory array that is not visible to the host system software. This ECC information is then checked during each flash array read operation. Any 1-bit error within the data unit will be corrected by the ECC logic. The 16-byte data unit is the smallest program granularity on which ECC is enabled.

When any amount of data is first programmed within a 16-byte data unit, the ECC value is set for the entire data unit. If additional data is subsequently programmed into the same data unit, without an erase, then the ECC for that data unit is disabled and the 1-bit ECC disable bit is set. A sector erase is needed to again enable ECC on that data unit.

These are automatic operations transparent to the user. The transparency of the ECC feature enhances data reliability for typical programming operations which write data once to each data unit while also facilitating software compatibility with previous generations of products by still allowing for single-byte programming and bit-walking (in this case, ECC will be disabled) in which the same data unit is programmed more than once.

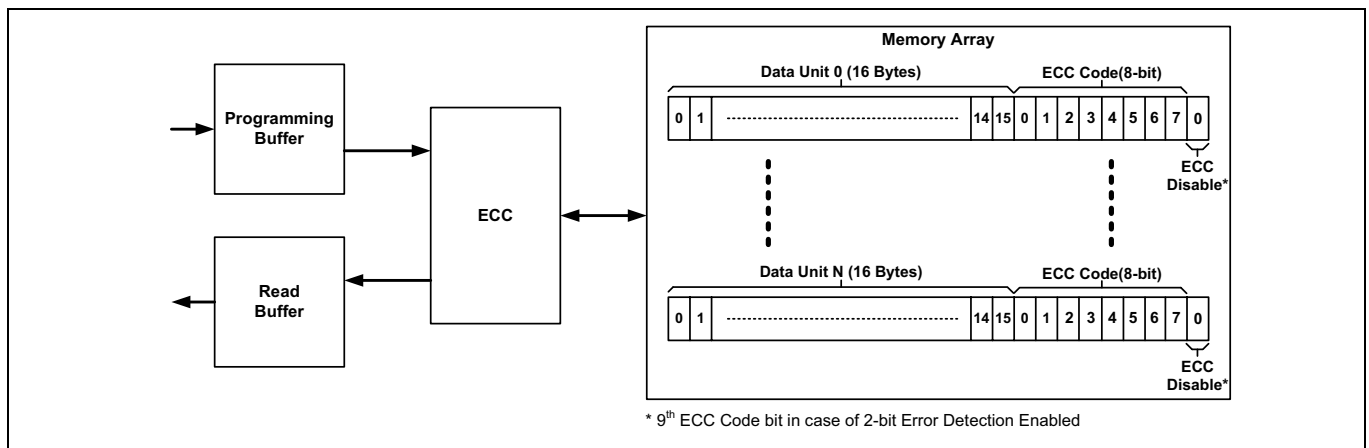


Figure 40 16-byte ECC data unit example

SEMPER™ NOR Flash supports 2-bit error detection as the default ECC configuration. In this configuration, any 1-bit error in a data unit is corrected and any 2-bit error is detected and reported. The 16-byte unit data requires a 9-bit Error Correction Code for 2-bit error detection. When 2-bit error detection is enabled, byte-programming, bit-walking, or multiple program operations to the same data unit (without an erase) are not allowed and will result in a Program Error. Changing the ECC mode from 1-bit error detection to 2-bit error detection, or from 2-bit error detection to 1-bit error detection will invalidate all data in the memory array. When changing the ECC mode, the host must first erase all sectors in the device. If the ECC mode is changed without erasing programmed data, subsequent read operations will result in undefined behavior.

Features

4.1.1 ECC error reporting

There are four methods for reporting to the host system when ECC errors are detected.

- ECC Data Unit Status provides the status of 1-bit or 2-bit errors in data units.
- ECC Status Register provides the status of 1-bit or 2-bit errors since the last ECC clear or reset.
- The Address Trap Register captures the address location of the first ECC error encountered after POR or reset during memory array read.
- An ECC Error Detection counter keeps a tally of the number of 1-bit or 2-bit errors that have occurred in data units during reads.

4.1.1.1 ECC data unit status (EDUS)

- The status of ECC in each data unit is provided by the 8-bit ECC Data Unit Status.
- The ECC status transaction outputs the ECC status of the addressed data unit. The contents of the ECC Data Unit status then indicate, for the selected data unit, whether there is a 1-bit error corrected, 2-bit error detected, or the ECC is disabled for that data unit.

Table 9 ECC data unit status

| Bits | Fieldname | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|-----------|-----------|---|---|-----------------------------|--|
| EDUS[7:4] | RESRVD | Reserved For future use | V => R | 0000 | These bits are Reserved for future use. |
| EDUS[3] | ECC2BD | ECC Error 2-bit Error Detection Flag | V => R | 0 | This bit indicates whether a two bit error is detected in the data unit, if two bit ECC error detection is enabled CFR4V[3] = 1. When CFR4V[3] = 0 and 2-bit error detection is disabled, ECC2BD bit will always be '0'. Note If 2 bit error detection is enabled (CFR4V[3] = 1), the ECCOFF bit will not be set to 1b while performing single byte programming or bit walking in a data unit that was already partially programmed. An attempt to do such byte programming or bit walking will result in a Program Error. Selection Options: 1 = Two Bit Error detected 0 = No error |
| EDUS[2] | RESRVD | Reserved For future use | V => R | 0 | This bit is Reserved for future use. |
| EDUS[1] | ECC1BC | ECC Error 1-bit Error Detection and Correction Flag | V => R | 0 | This bit indicates whether an error was corrected in the data unit. Selection Options: 1 = Single Bit Error corrected in the addressed data unit 0 = No single bit error was corrected in the addressed data unit |
| EDUS[0] | ECCOFF | Data Unit ECC OFF/ON Flag | V => R | 0 | This bit indicates whether the ECC syndrome is OFF in the data unit. Selection Options: 1 = ECC is OFF in the selected data unit 0 = ECC is ON in the selected data unit Dependency: CFR4x[3] |

4.1.1.2 ECC status register (ECSV)

- An 8-bit ECC Status Register provides the status of 1-bit or 2-bit errors during normal reads since last ECC clear or reset. ECC Status Register does not have user programmable nonvolatile bits, all defined bits are volatile read only bits. The default state of these bits are set by hardware.
- ECC Status Register can be accessed through the Read Any Register transaction. The correct sequence for Read Any Register based ECSV is read as follows:
 - Read data from memory array using any of the Read transaction
 - ECSV is updated by the device
 - Read Any Register transaction of ECSV provides the status of any ECC event since the last clear or reset.
- ECSV is cleared by POR, CS# Signaling Reset, Hardware/Software reset, or a Clear ECC Status Register transaction.

4.1.1.3 ECC error address trap (EATV)

- A 32-bit register is provided to capture the ECC data unit address where an ECC error is first encountered during a read of the flash array. Only the address of the first enabled error type (“2-bit only” or “1-bit or 2-bit” as selected in CFR4N[3]) encountered after POR, hardware reset, or the ECC Clear transaction is captured. The EATV Register is only updated during Read transactions.

The EATV Register contains the address that was accessed when the error was detected. The failing bits may not be located at the exact address indicated in the register, but will be located within the aligned 16-byte ECC data unit where the error was detected. If errors are found in multiple ECC data units during a single read operation, only the address of the first failing ECC unit address is captured in the EATV Register.

When 2-bit error detection is not enabled and the same ECC unit is programmed more than once, ECC error detection for that ECC unit is disabled, therefore no error can be recognized to trap the address.

The Address Trap Register has a valid address when the ECC Status Register (ECSV) bit 3 or 4 = 1.

- The Address Trap Register can be read using the Read Any Register transaction.
- Clear ECC Status Register transaction, POR, or CS# Signaling/Hardware/Software reset clears the Address Trap Register.

4.1.1.4 ECC error detection counter (ECTV)

- A 16-bit register is provided to count the number of 1-bit or 2-bit errors that occur as data is read from the flash memory array. Only errors recognized in the main array will cause the Error Detection Counter to increment. ECTV Register is only updated during Read transaction. Read ECC Status transaction does not affect the ECTV Register.

The 16-bit Error Detection Counter will not increment beyond FFFFh. However, the ECC continues to work.

Note that during continuous read operations, when a 1-bit or a 2-bit error is detected, the clock may continue toggling and the memory device will continue incrementing the data address and placing new data on the DQ signals; any additional data units with errors that are encountered will be counted until CS# is brought back HIGH.

During a read transaction only one error is counted for each data unit found with an error. Each read transaction will cause a new read of the target data unit. If multiple read transactions access the same data unit containing an error, the error counter will increment each time that data unit is read.

When 2-bit error detection is not enabled and the same data unit is programmed more than once, ECC error detection for that data unit is disabled so, no error can be recognized or counted.

- The ECC Error Detection Counter Register can be read using the Read Any Register transaction.
- ECTV Register is set to 0 on POR, CS# Signaling/Hardware/Software Reset or with Clear ECC Status Register transaction.

Features

4.1.2 ECC related registers and transactions

Table 10 ECC related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|---|--|
| Configuration Register - 4 (CFR4N, CFR4V) (see Table 52 on page 81) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| ECC Status Register (ECSV) (see Table 55 on page 83) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| ECC Address Trap Register (EATV) (see Table 56 on page 83) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |
| ECC Error Detection Counter Register (ECTV) (see Table 57 on page 84) | Read ECC Status (RDECC_4_0, RDECC_C_0) | Read ECC Status (RDECC_4_0, RDECC_C_0) |
| | Clear ECC Status Register (CLECC_0_0) | Clear ECC Status Register (CLECC_0_0) |

4.2 Infineon® Endurance Flex architecture (wear leveling)

Infineon® Endurance Flex architecture allows partitioning of the main memory array into regions which can be configured as either high endurance or long retention. Infineon® Endurance Flex architecture implements wear leveling in high endurance regions where program/erase cycles are spread evenly across all the sectors which are part of the wear leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, Infineon® Endurance Flex architecture's wear leveling algorithm is based on a mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of program/erase cycles over all physical sectors. The logical to physical mapping information is stored in a dedicated flash array which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

Infineon® Endurance Flex architecture's high endurance region requires a minimum set of 20 sectors. To provide flexibility between configuring long retention, high endurance, or both regions, a four pointer architecture is provided. The factory default setting designates all sectors as high endurance as part of the wear leveling pool with all pointers disabled. The four pointers can be used to form a maximum of five regions which can each be configured as long retention or high endurance.

Figure 41 provides an overview of the Infineon® Endurance Flex architecture. It shows the five possible regions based on different sector architecture.

Note

12.4KB sectors are not part of the Infineon® Endurance Flex architecture.

Features

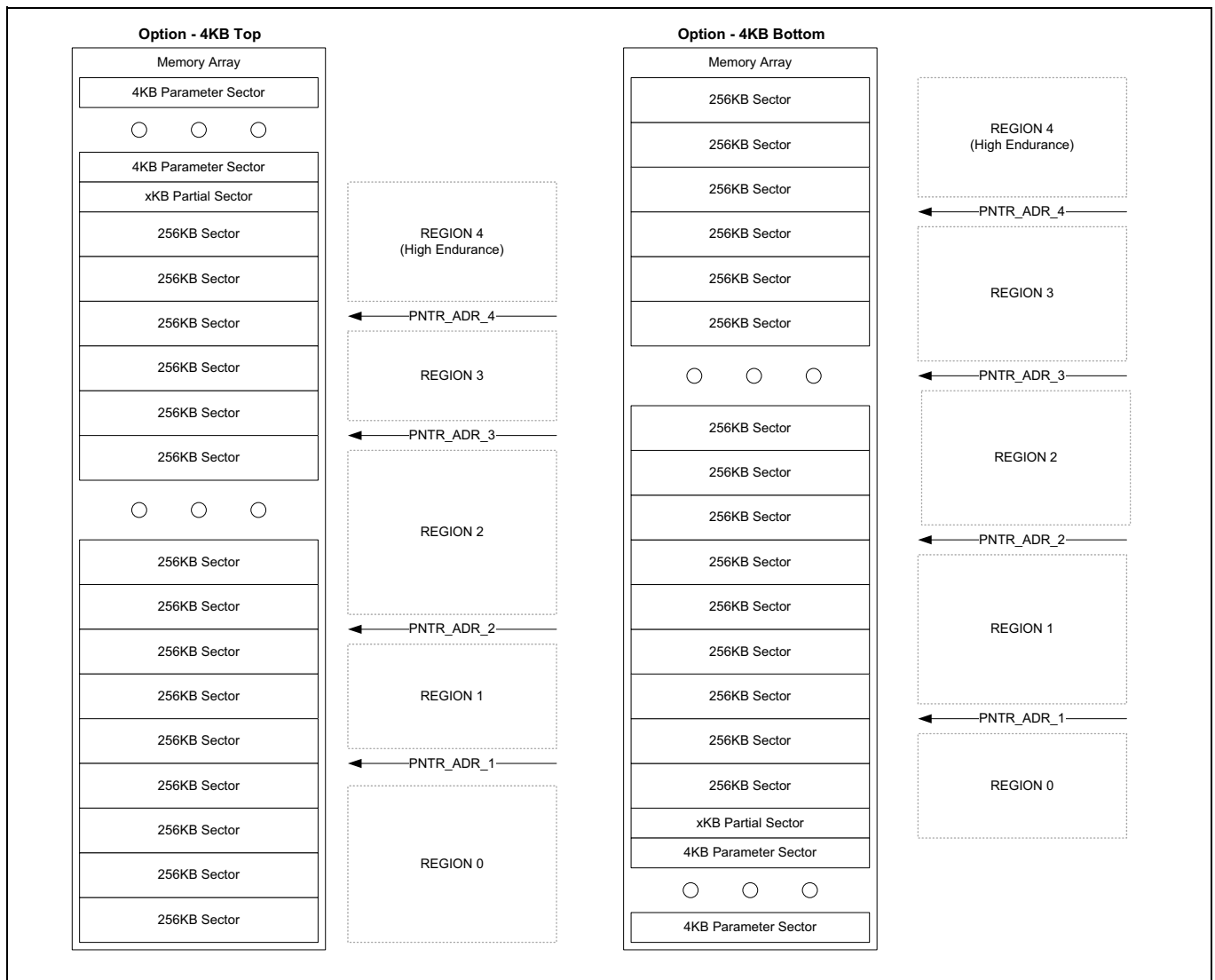


Figure 41 Infineon® Endurance Flex architecture overview

Features

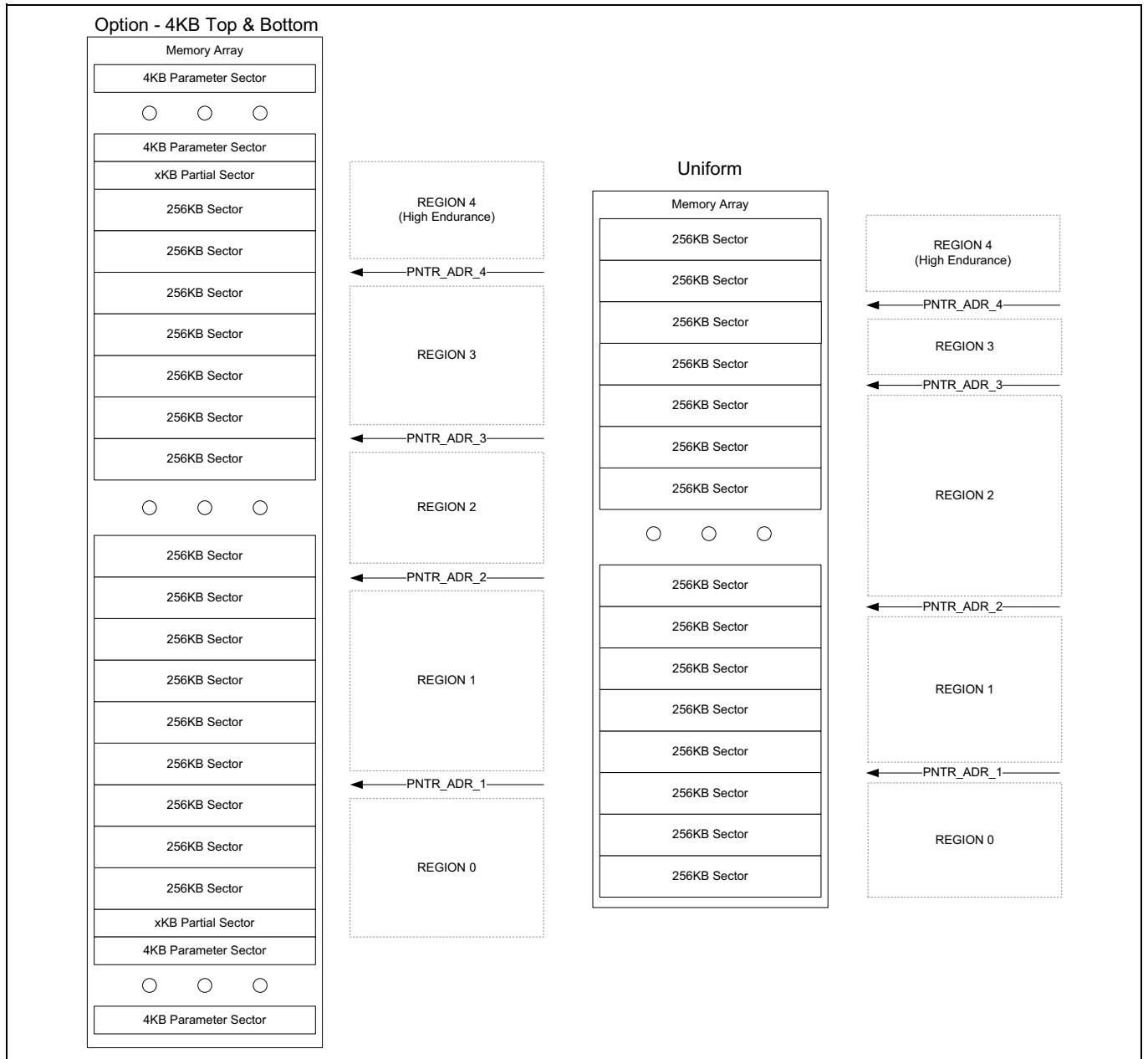


Figure 42 Infineon® Endurance Flex architecture overview (Continued)

Features

Table 11 Region definitions^[13, 14, 15, 16]

| Region | Lower limit | Upper limit |
|--------|-------------------|-------------------|
| 0 | Sector 0 | Address Pointer 1 |
| 1 | Address Pointer 1 | Address Pointer 2 |
| 2 | Address Pointer 2 | Address Pointer 3 |
| 3 | Address Pointer 3 | Address Pointer 4 |
| 4 | Address Pointer 4 | Highest Sector |

Notes

- 13. The pointer addresses must obey the following rules:
 Pointer#4 address > Pointer#3 address
 Pointer#3 address > Pointer#2 address
 Pointer#2 address > Pointer#1 address
- 14. 4KB sectors are excluded.
- 15. It is required that the high data endurance and long data retention regions are configured at the time the device is first powered-up by the customer. Once configured, they can never be changed again.
- 16. The minimum size of any high endurance region is 20 sectors.

4.2.1 Configuration 1: Maximum endurance - Single high endurance region

Maximum endurance is achieved when all 256KB sectors are designated as high endurance. All sectors must be designated as high endurance using the Infineon® Endurance Flex architecture pointer. Maximum endurance pointer configuration is shown in [Table 12](#).

Table 12 Infineon® Endurance Flex architecture pointer values for maximum endurance configuration^[17]

| Pointer # | Pointer address EPTADn[8:0] | Region type ERGNTn | Pointer enable# EPTEBn | Global region selection GBLSEL | Wear leveling enable WRLVEN |
|-----------|-----------------------------|--------------------|------------------------|--------------------------------|-----------------------------|
| 0 | N/A | N/A | N/A | 1'b1 | 1'b1 |
| 1 | 9'b111111111 | 1'b1 | 1'b1 | N/A | N/A |
| 2 | 9'b111111111 | | | | |
| 3 | 9'b111111111 | | | | |
| 4 | 9'b111111111 | | | | |

Note

- 17. This is also the default configuration of the device.

4.2.2 Configuration 2: Two region selection - One long retention region and one high endurance region

Sectors for long retention or high endurance must be delineated using the Infineon® Endurance Flex architecture pointer. Region 0 is defined as long retention and consists of 16 sectors. Region 1 is defined as high endurance and has 240 sectors. The pointer setup for two region configuration is shown in [Table 13](#). The number of pointers defined is based on the number of regions configured.

Table 13 Infineon® Endurance Flex architecture pointer values for two region configuration

| Pointer # | Pointer address EPTADn[8:0] | Region type ERGNTn | Pointer enable# EPTEBn | Global region selection GBLSEL | Wear leveling enable WRLVEN |
|-----------|-----------------------------|--------------------|------------------------|--------------------------------|-----------------------------|
| 0 | N/A | N/A | N/A | 1'b0 | 1'b1 |
| 1 | 9'b000010000 | 1'b1 | 1'b0 | N/A | N/A |
| 2 | 9'b111111111 | 1'b1 | 1'b1 | | |
| 3 | | | | | |
| 4 | | | | | |

Features

4.2.3 Infineon® Endurance Flex architecture related registers and transaction

Table 14 Infineon® Endurance Flex architecture related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|---|--|
| Infineon® Endurance Flex architecture Selection Registers (EFX40, EFX30, EFX20, EFX10, EFX00) (see Infineon® Endurance Flex architecture selection register (EFXx) on page 88) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |

4.3 Data integrity CRC

HL-T/HS-T family devices have a group of transactions to perform a hardware accelerated Cyclic Redundancy Check (CRC) calculation over a user defined address range in the memory array. The calculation is another type of embedded operation similar to programming or erase, in which the device is busy while the calculation is in progress. The CRC operation uses the following CRC32 polynomial to determine the CRC check-value.

$$\text{CRC32 Polynomial: } X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$$

The check-value generation sequence is started by entering the DICHK_4_1 transaction. The transaction includes loading the beginning address into the CRC Start Address Register identifying the beginning of the address range that will be covered by the CRC calculation. The transaction also includes loading the ending address into the CRC End Address Register. Bringing CS# HIGH starts the CRC calculation. The CRC process calculates the check-value on the data contained at the starting address through the ending address.

During the calculation period the device goes into the Busy state (STR1V[0] - RDYBSY = 1). Once the check-value calculation has completed the device returns to the Ready state (STR1V[0] - RDYBSY = 0) and the calculated check-value is available to be read. The check-value is stored in the Data Integrity CRC Register (DCRV[31:0]) and can be read using Read Any Register (RDARG_C_0) transaction.

The check-value calculation can only be initiated when the device is in Standby State; and once started it can be suspended with the CRC Suspend transaction (SPEPD_0_0) to read data from the memory array. During the Suspended state the CRC Suspend Status Bit in the Status Register 2 will be set (STR2V[4] - DICRCS = 1). Once suspended, the host can read the Status Register, read data from the array and can resume the CRC calculation by using the CRC Resume transaction (RSEPD_0_0).

The Ending Address (ENDADD) must be at least two addresses higher than the Starting Address (STRADD). If $\text{ENDADD} < \text{STRADD} + 3$ the check-value calculation will abort and the device will return to the Ready state (STR1V[0] - RDYBSY = 0). Data Integrity CRC abort status bit will be set (STR2V[3] - DICRCA = 1) to indicate the aborted condition. The DICRCA bit can be cleared, once set, by Software reset or a valid subsequent CRC command execution. If $\text{ENDADD} < \text{STRADD} + 3$, the check-value will hold indeterminate data.

Note Any invalid transaction during CRC check-value calculation can corrupt the check-value data.

4.3.1 Data integrity check related registers and transactions

Table 15 Data integrity CRC related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|--|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Data Integrity Check (DICHK_4_1) | Data Integrity Check (DICHK_4_1) |
| Status Register 2 (STR2V) (see Table 44 on page 75) | Suspend Erase/Program/Data Integrity Check (SPEPD_0_0) | Suspend Erase/Program/Data Integrity Check (SPEPD_0_0) |
| Data Integrity CRC Check-Value Register (DCRV) (see Table 54 on page 82) | Resume Erase/Program/ Data Integrity Check (RSEPD_0_0) | Resume Erase/Program/ Data Integrity Check (RSEPD_0_0) |

4.4 Data protection schemes

Data protection is required to safeguard against unintended changes to stored data and device configuration. This includes inadvertent erasing or programming the memory array as well as writing to the configuration registers which can alter the functionality of the device. Three types of protection schemes are discussed which range from protecting either a single or a group of sectors to either a portion or the complete memory array. **Figure 43** shows an overview of different protection schemes along with applicable data regions.

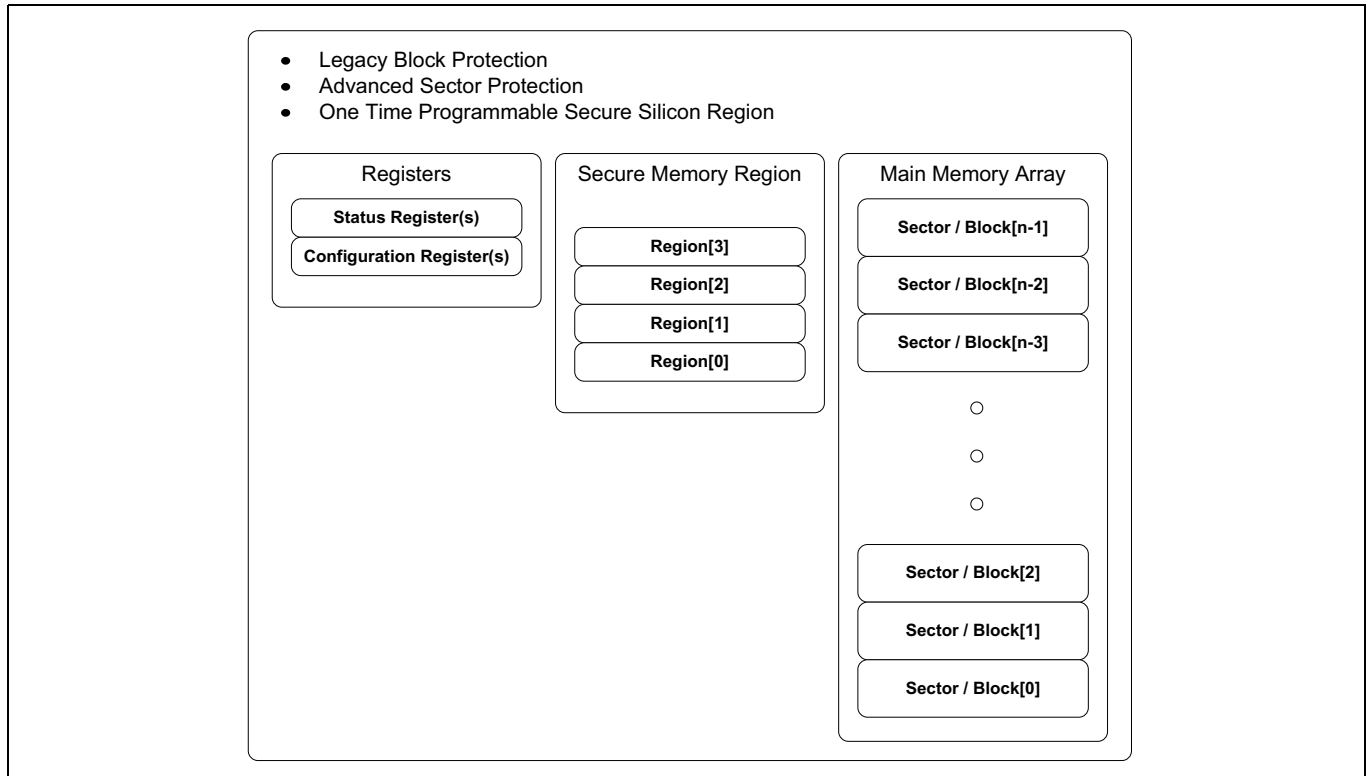


Figure 43 Data protection and security (write/program/erase) schemes

4.4.1 Legacy block protection (LBP)

The Legacy Block Protection (LBP) is a block-based data protection scheme. LBP supports compatibility with legacy serial NOR Flash devices. LBP provides protection for data in the memory array and device configuration by protecting Status and Configuration registers.

4.4.1.1 Memory array protection

The protection for the memory array is with block size selection, which is achieved through a combination of bits present in the Status Register 1 (STR1N[4:2]/STR1V[4:2] - LBPROT[2:0]) and Configuration Register 1 (CFR1N[5]/CFR1V[5] - TBPROT).

Features

Table 16 provides the LBP memory array block selection summary.

Table 16 Legacy block memory array protection selection

| CFR1N[5]/CFR1V[5] TBPROT | STR1N[4]/STR1V[4] LBPROT[2] | STR1N[3]/STR1V[3] LBPROT[1] | STR1N[2]/STR1V[2] LBPROT[0] | Memory array block size | 256Mb (KBs) | 512Mb (KBs) | 1Gb (KBs) |
|-----------------------------|--------------------------------|--------------------------------|--------------------------------|----------------------------|----------------|----------------|-----------|
| 0 | 0 | 0 | 0 | None | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | Upper 64th | 512 | 1024 | 2048 |
| 0 | 0 | 1 | 0 | Upper 32nd | 1024 | 2048 | 4096 |
| 0 | 0 | 1 | 1 | Upper 16th | 2048 | 4096 | 8192 |
| 0 | 1 | 0 | 0 | Upper 8th | 4096 | 8192 | 16384 |
| 0 | 1 | 0 | 1 | Upper 4th | 8192 | 16384 | 32768 |
| 0 | 1 | 1 | 0 | Upper Half | 16384 | 32768 | 65536 |
| 0 | 1 | 1 | 1 | All sectors | 32768 | 65536 | 131072 |
| 1 | 0 | 0 | 0 | None | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | Lower 64th | 512 | 1024 | 2048 |
| 1 | 0 | 1 | 0 | Lower 32nd | 1024 | 2048 | 4096 |
| 1 | 0 | 1 | 1 | Lower 16th | 2048 | 4096 | 8192 |
| 1 | 1 | 0 | 0 | Lower 8th | 4096 | 8192 | 16384 |
| 1 | 1 | 0 | 1 | Lower 4th | 8192 | 16384 | 32768 |
| 1 | 1 | 1 | 0 | Lower Half | 16384 | 32768 | 65536 |
| 1 | 1 | 1 | 1 | All sectors | 32768 | 65536 | 131072 |

4.4.1.2 Configuration protection

LBP has selection bits in Configuration Register 1 (CFR1N[4,0]/CFR1V[4,0] - PLPROT, TLPROT) which either permanently or temporarily protect Status and Configuration registers, thereby again protecting the device's configuration. The temporary protection remains in effect until the next power down or hardware reset or CS# signaling reset.

Table 17 Option 2 - Legacy block configuration protection selection^[18]

| CFR1N[4]/CFR1V[4] PLPROT | CFR1N[0]/CFR1V[0] TLPROT | Register protection status |
|-----------------------------|-----------------------------|---|
| 0 | 0 | Status and Configuration registers are unprotected |
| 1 | X | Status and Configuration registers are permanently protected (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS) |
| 0 | 1 | Status and Configuration registers are Protected till next Power down (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS) |

Note

18. Protecting the configuration also protects the memory array blocks which have been selected for protection.

4.4.1.3 Write protect signal

The Write Protect (DQ2_WP#) input in combination with the Status Register Write Disable bit (STR1x[7]) provide hardware input signal controlled protection. When WP# is LOW and STR1x[7] is set to “1” Status Register 1 (STR1N and STR1V) and Configuration register-1 (CFR1N and CFR1V) are protected from alteration. This prevents disabling or changing the protection defined by the Block Protect bits.

4.4.1.4 Legacy block protection flowchart

The LBP protection scheme flowchart is shown in [Figure 44](#).

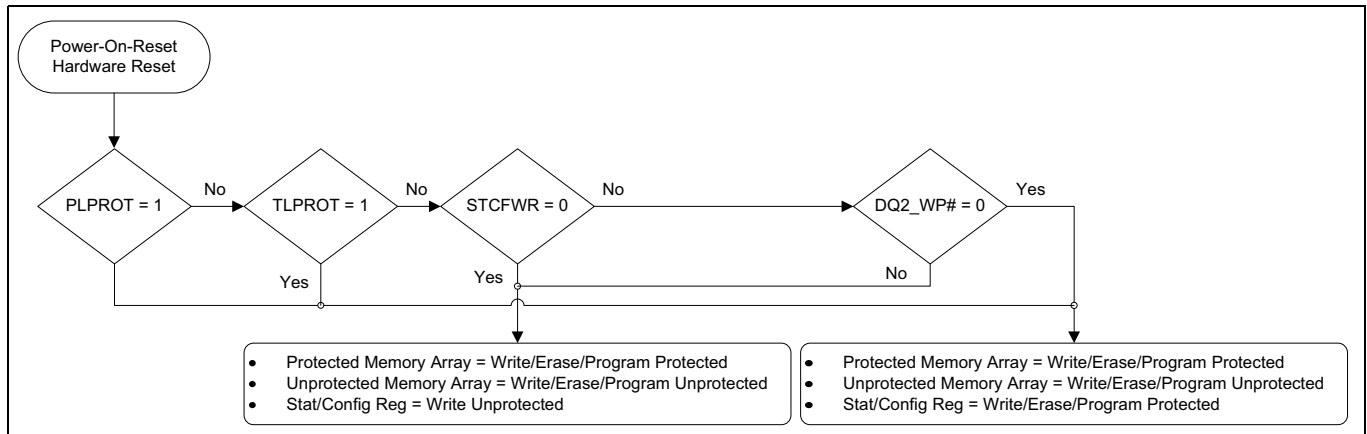


Figure 44 Legacy block protection flowchart

4.4.1.5 LBP related registers and transactions

Table 18 LBP related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|---|--|---|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| Configuration Register 1 (CFR1N, CFR1V) (see Table 45 on page 76) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |
| | Read Status Register 1 (RDSR1_0_0) | Read Status Register 1 (RDSR1_0_0) |
| | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |

4.4.2 Advanced sector protection (ASP)

The Advanced Sector Protection (ASP) scheme allows each memory array sector to be independently controlled for protection against erasing or programming, either by volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well as password-protected.

The main memory array sectors are protected against erase and program by volatile (DYB) and nonvolatile (PPB) protection bit pairs. Each DYB/PPB bit pair can be individually set to '0' protecting the related sector or cleared to '1' un-protecting the related sector. DYB protection bits can be set and cleared as often as needed whereas PPB bits being nonvolatile must adhere to their respective technology based endurance requirements. [Figure 45](#) shows an overview of ASP.

Features

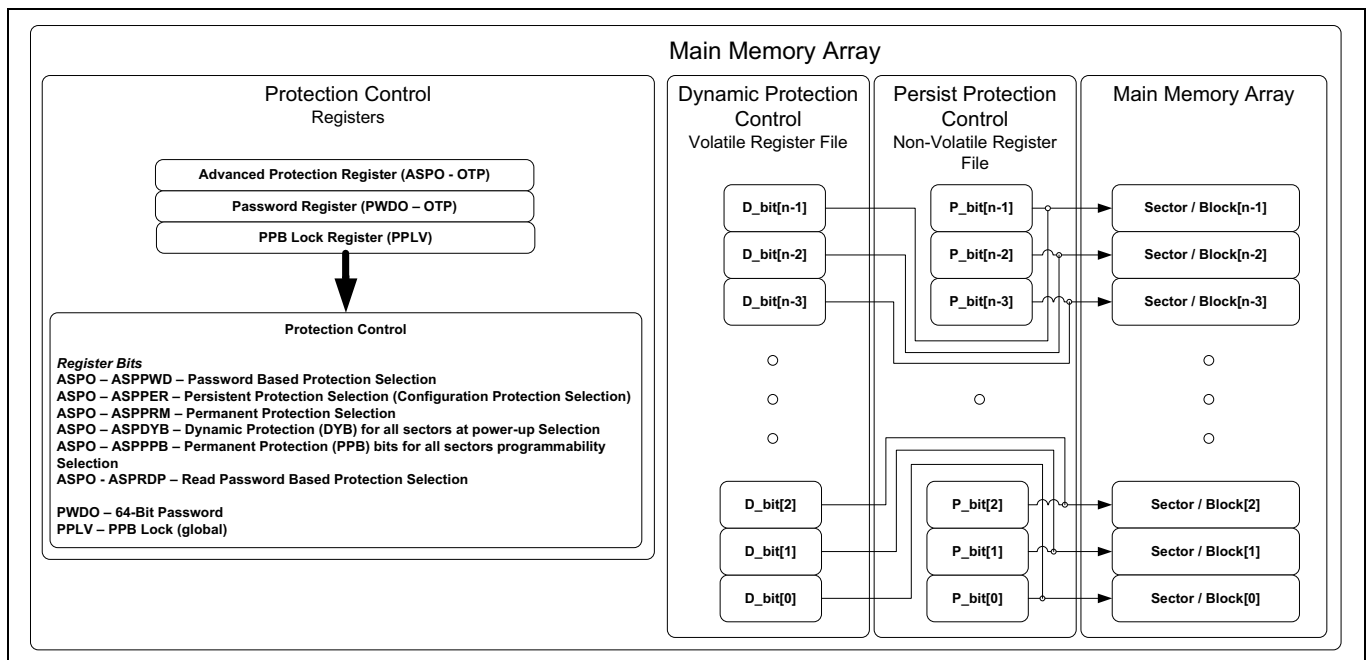


Figure 45 Advanced sector protection (Nonvolatile)

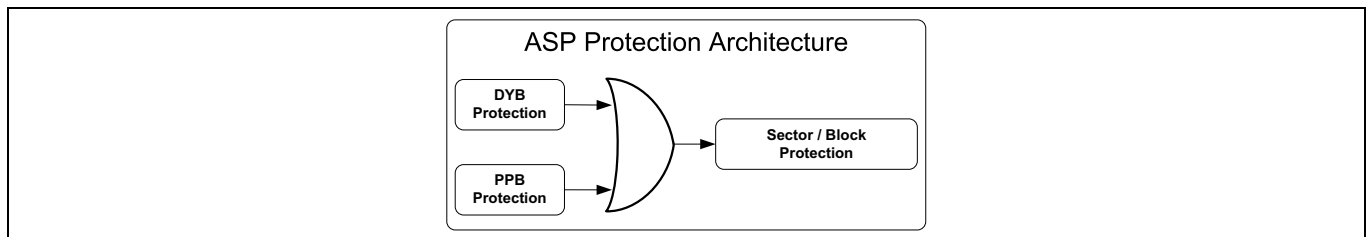


Figure 46 DYB and PPB protection control

ASP provides a rich set of configuration options producing multiple data protection schemes which can be employed based on design or system needs. These configuration options are discussed in [Configuration protection on page 39](#) through [ASP related registers and transactions on page 44](#).

4.4.2.1 Configuration protection

ASP provides provisions to protect device's configuration through Persistent Protection scheme. Selecting bit 1 in Advanced Sector Protection Register (ASPO[1] - ASPPER) selects the Persistent Protection scheme and protects the following registers or register bits from write or program:

- CFR1V[6,5,4,2]/CFR1N[6,5,4,2] - SP4KBS, TBPROT, PLPROT, TB4KBS
- CFR3N[3]/CFR3V[3] - UNHYSA
- ASPO[15:0]
- PWDO[63:0]

The persistent protection scheme flowchart is shown in [Figure 47](#).

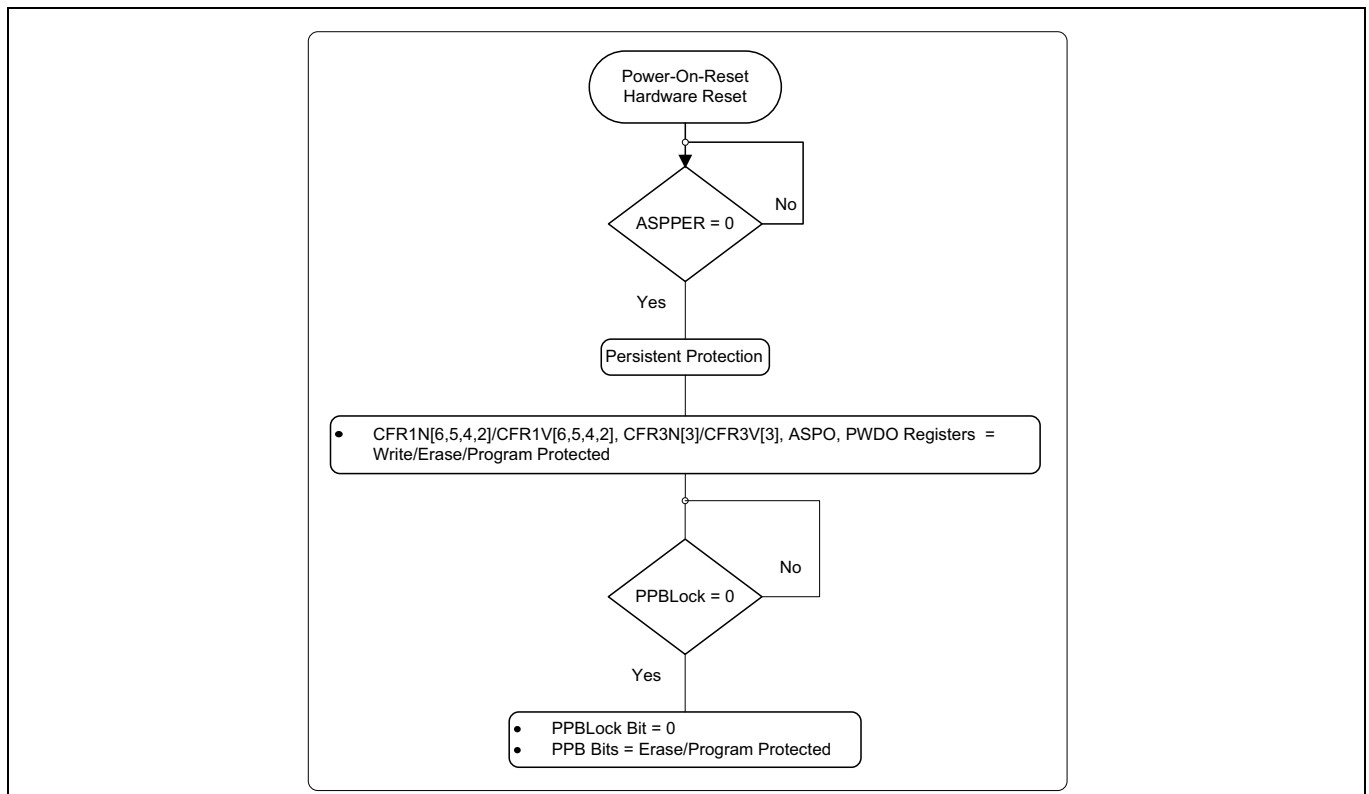


Figure 47 Persistent protection scheme flowchart

4.4.2.2 Dynamic DYB (volatile) sector protection

Dynamic Protection Bits (DYB) are volatile and unique for each sector and can be individually modified. DYBs only control protection for sectors that have their PPBs cleared. By issuing the DYB Write transaction, the DYB are set to 0 or cleared to 1, thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The DYB can be set to 0 or cleared to 1 as often as needed

In Dynamic Sector Protection scheme, an option is provided to reset all DYB volatile protection bits to '0' upon power up (protected), essentially protecting all sectors from erase or program. Selecting bit 4 in the Advanced Sector Protection Register (ASPO[4] - ASPDYB) selects the Dynamic Protection (DYB) for all sectors at power-up protection scheme. These DYB bits can be individually set to '1', if desired. The Dynamic Sector Protection scheme flowchart showing power up protection is shown in [Figure 48](#).

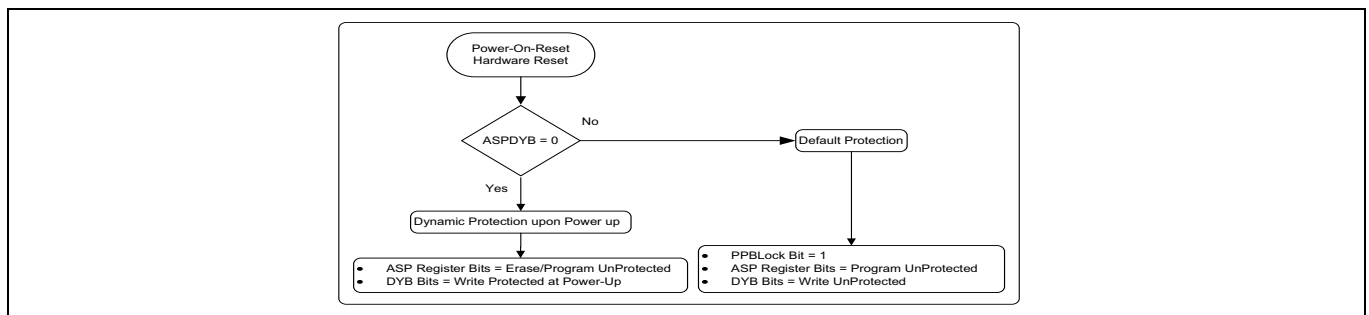


Figure 48 Dynamic sector protection scheme flowchart

4.4.2.3 Permanent/Temporary PPB (nonvolatile) sector protection

Each nonvolatile bit (PPB) provides nonvolatile protection for an individual memory sector, which remains locked (protection enabled) until its corresponding bit is cleared to 1. There are two options to control the PPB based nonvolatile selection in ASP, namely Permanent and Temporary.

4.4.2.4 Permanent PPB protection scheme

The PPB are located in a separate nonvolatile flash array. One of the PPB bits is assigned to each sector. When a PPB is programmed to 0 its related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire PPB sector must be erased at the same time. Programming a PPB bit requires the typical word programming time. During a PPB bit programming operation or PPB bit erasing, the Status Register can be accessed to determine when the operation has completed. Erasing all the PPBs requires typical sector erase time.

Permanent PPB based protection scheme, as the name applies, is permanent and can never be altered. Once the PPB architecture is decided, selecting bit 0 in Advanced Sector Protection Register (ASPO[0]) enables the Permanent Protection for all PPB bits essentially disabling all PPB erase and program operations. ASPO is also protected from write or program.

The Permanent PPB Protection scheme flowchart is shown in [Figure 49](#).

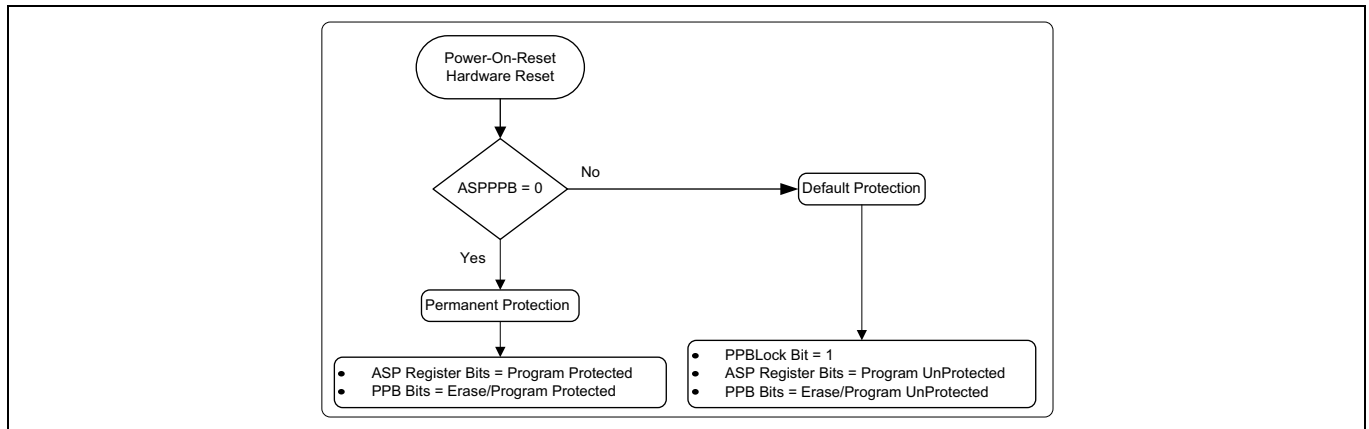


Figure 49 Permanent PPB sector protection flowchart

4.4.2.5 Temporary PPB protection scheme

PPB based nonvolatile protection architecture can be temporarily locked where erasing and programming of the individual PPB bits is inhibited. The Persistent Protection Lock Bit (PPB Lock) is a volatile bit for protecting all PPB bits. When cleared to 0, it locks all PPBs and when set to 1, it allows the PPBs to be changed. There is only one PPB Lock Bit per device. The PPB Lock transaction (WRPLB_0_0) is used to clear the bit to 0. The PPB Lock Bit must be cleared to 0 only after all the PPBs are configured to the desired settings. The PPB Lock Bit is set to 1 during POR or a Hardware Reset. When cleared with the PPB Lock transaction, no software command sequence can set PPB Lock, only another Hardware Reset or Power-Up can set PPB Lock.

Note Temporary PPB Protection does not require any ASP configuration.

4.4.2.6 Password protection scheme

Password Protection scheme allows an even higher level of security, by requiring a 64-bit password for setting PPB Lock. In addition to this password requirement, after Power-Up or Hardware Reset, the PPB Lock Bit is cleared to 0 to ensure protection at Power-Up. Successful execution of the Password Unlock transaction by entering the entire password sets the PPB Lock Bit to 1, allowing for sector PPB modifications. Selecting bit 2 in Advanced Sector Protection Register (ASPO[2] - ASPPWD) selects the Password Protection scheme. Password Protection scheme also protects ASPO from write or program.

Note A password must be programmed before selecting the password protection scheme. The password unlock SPI transaction (PWDUL_0_1) is used to provide a password for comparison.

The Password Protection scheme flowchart is shown in [Figure 50](#).

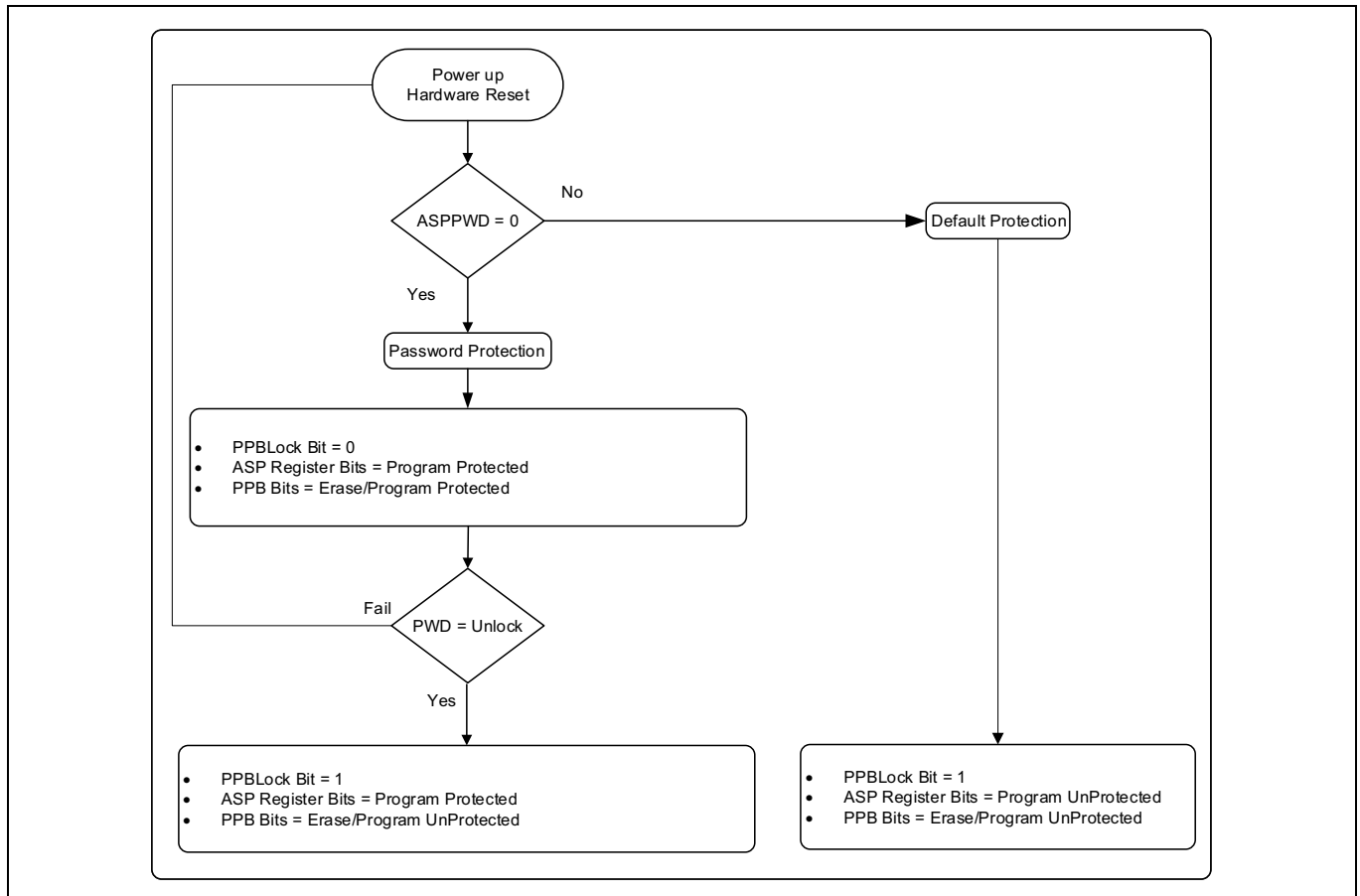


Figure 50 Password protection scheme flowchart

4.4.2.7 Read password protection scheme

The Read Password Protection scheme replaces the Password Protection scheme and provides the most data protection. The Read Password Protection scheme enables protecting the flash Memory Array from read, program, and erase. Only the lowest or highest (256KB) sector address range, selected by bit 5 of Configuration Register 1 (CFR1x[5] - TBPROT), remains readable until a successful Password Unlock transaction is complete. A '0' selects from the top most sector and a '1' selects from the bottom most sector irrespective of the sector address supplied in the read transaction. Note that reads from the read-protected portion of the array will alias back to the readable sector.

Clear Program and Erase Failure Flags transaction, all memory array Read transactions, Password Unlock transaction, Read manufacturer and device ID transaction, Read SFDP transaction, Read Status Register -1 transaction, Read Status Register-2 transaction, Read ECC Status transaction, Clear ECC Status Register transaction, and Enter DPD Mode transaction are allowed during Password Read Mode before the Password is supplied.

Note A password must be programmed before selecting the Read Password Protection Scheme. The password unlock SPI transaction

(PWDUL_0_1) is used to provide a password for comparison.

The Read Password Protection scheme flowchart is shown in [Figure 51](#).

Features

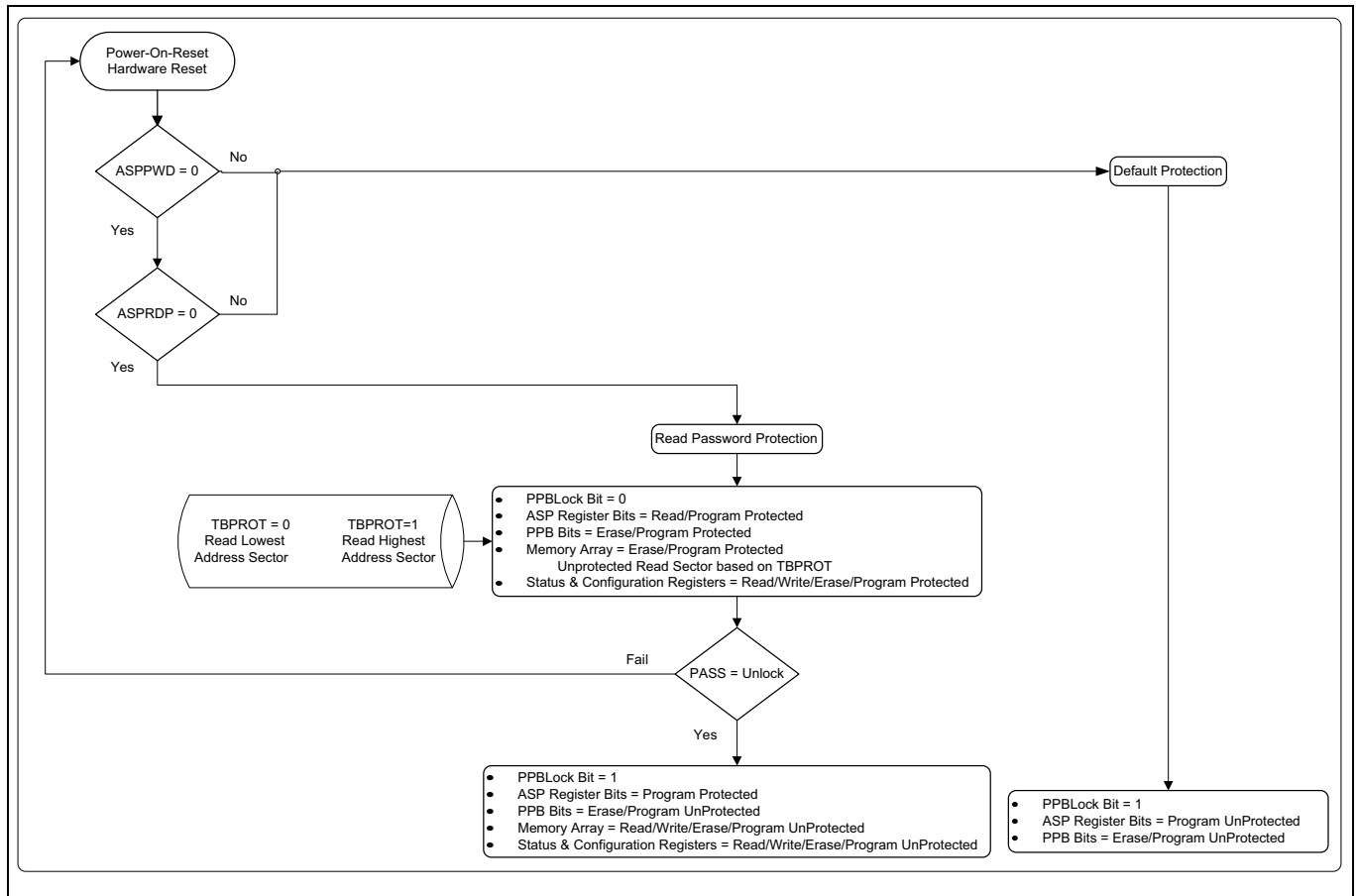


Figure 51 Read password protection scheme flowchart

4.4.2.8 PPB Bits - OTP selection

ASP provides a configuration option to permanently disable the PPB erase transaction (ERPPB_0_0). This makes all PPB bits OTP. With this option, once the PPB protection is selected, it can never be changed. Selecting bit 3 in Advanced Sector Protection Register (ASPO[3] - ASPPPB) makes PPB bits OTP.

4.4.2.9 General ASP guidelines

- Persistent protection (ASPPER) and Password protection (ASPPWD) are mutually exclusive - only one option can be programmed.
- Read Password protection (ASPRDP) if desired, must be programmed at the same time as Password protection (ASPPWD).
- Once the password is programmed and verified, the Password Protection scheme (ASPPWD) must be programmed (to 0) to prevent reading the password.
- When the Read Password scheme and Password Protection scheme are enabled (i.e. ASPO[5] - ASPRDP, ASPO[2] - ASPPWD are programmed to 0), then all addresses are redirected to the Boot Sector until the password unlocking sequence is properly entered with the correct password. At which time, the Read Password Mode is disabled and all addressing will select the proper location.
- Programming memory spaces or writing registers is not allowed when Read Password Protection Mode is active.

Features

4.4.2.10 ASP related registers and transactions

Table 19 ASP related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|---|--|--|
| Advanced Sector Protection Register (ASPO) (see Table 58 on page 84) | Read Dynamic Protection Bit (RDDYB_4_0, RDDYB_C_0) | Read Dynamic Protection Bit (RDDYB_4_0, RDDYB_C_0) |
| Configuration Register 1 (CFR1N, CFR1V) (see Table 45 on page 76) | Write Dynamic Protection Bit (WRDYB_4_1, WRDYB_C_1) | Write Dynamic Protection Bit (WRDYB_4_1, WRDYB_C_1) |
| | Read Persistent Protection Bit (RDPPB_4_0, RDPPB_C_0) | Read Persistent Protection Bit (RDPPB_4_0, RDPPB_C_0) |
| | Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0) | Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0) |
| | Erase Persistent Protection Bit (ERPPB_0_0) | Erase Persistent Protection Bit (ERPPB_0_0) |
| | Write PPB Protection Lock Bit (WRPLB_0_0) | Write PPB Protection Lock Bit (WRPLB_0_0) |
| | Read Password Protection Mode Lock Bit (RDPLB_0_0) | Read Password Protection Mode Lock Bit (RDPLB_0_0) |
| | Password Unlock (PWDUL_0_1) | Password Unlock (PWDUL_4_1) |
| | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |

4.4.3 Secure silicon region (SSR)

Secure Silicon Region (SSR) is a 1024 byte memory region (separate from the main memory array). The 1024 bytes are divided into 32, individually lockable 32-byte regions. Figure 52 provides an overview of SSR.

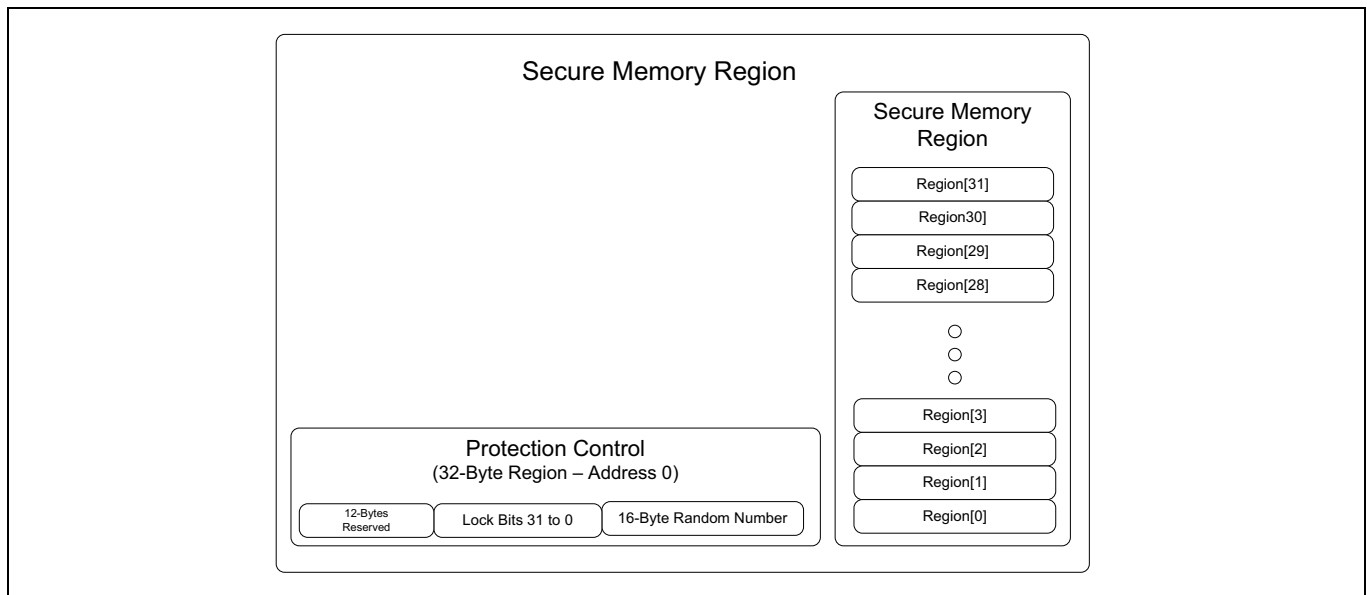


Figure 52 OTP protection (nonvolatile)

The first 32-byte region (starting at address 0) provides the protection mechanism for the other 32-byte regions. The sixteen lowest bytes of this region contain a 128-bit random number. The random number cannot be written to, erased or programmed. The next four bytes (32 bits in total) of this region provide protection from programming if set to '0' for the remaining 32-byte regions - one bit per 32-byte region. All other bytes are reserved.

Note Attempting to Erase or Program the 128-bit random number will result in ERSERR or PRGERR, respectively. A hardware Reset is required to bring the device back to Standby mode.

Features

4.4.3.1 SSR related registers and transactions

Table 20 SSR related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|-------------------|---|--|
| N/A | Program Secure Silicon Region (PRSSR_C_1) | Program Secure Silicon Region (PRSSR_C_1) |
| | Read Secure Silicon Region (RDSSR_C_0) | Read Secure Silicon Region (RDSSR_C_0) |

4.5 SafeBoot

SEMPER™ Flash memory devices contain an embedded microcontroller which is used to initialize the device, manage embedded operations, and perform other advanced functionality. An initialization failure of this embedded microcontroller or corruption of the nonvolatile configuration registers can render the flash device unusable. Barring a catastrophic event, such as permanent corruption of the embedded microcontroller firmware, it is possible to recover the device.

The SafeBoot feature allows Status Register polling to detect an embedded microcontroller initialization failure or configuration register corruption through error signatures.

4.5.1 Microcontroller initialization failure detection

If the microcontroller embedded in the flash device fails to initialize, a hardware reset can recover the device, unless it is a catastrophic failure. This hardware reset must be initiated by the Host controller. Upon detecting a failed microcontroller initialization, the flash device automatically reverts to its Default Boot mode (1S-1S-1S) and provides a failure signature in its Status Register.

Table 21 shows the device's Status Register bits upon detecting an initialization failure.

Table 21 Status register 1 power-on detection signature

| Bit | Field name | Function | Detection signature |
|----------|-------------|---|---------------------|
| STR1V[7] | STCFWR | Status Register and Configuration Registers Protection Selection against write (erase/program) | 0 |
| STR1V[6] | PRGERR | Programming Error Status Flag | 1 |
| STR1V[5] | ERSERR | Erasing Error Status Flag | 1 |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection | 0 |
| STR1V[3] | | Note: LBPROT[2:0] can be anything from 000 to 111 based on Block Protection configuration. | 0 |
| STR1V[2] | | | 0 |
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | 0 |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | 1 |

Table 22 Interface configuration upon detecting power-on failure^[19]

| Interface | Transactions supported | Register type | Address (# of bytes) | Frequency of operation | Register read latency (# of clock cycles) | Output impedance |
|----------------|---|---------------------------------|----------------------|--|---|------------------|
| SPI (1S-1S-1S) | Read Status Register 1 (RDSR1_0_0) Read Any Register (RDARG_C_0) | Status Register (Volatile Only) | 4 | Maximum (allowed for RDSR1_0_0, RDARG_C_0) | 2 | 45Ω |

Note

19. For reading the Status Register, providing the NonVolatile Status Register address to RDARG_C_0 will produce indeterminate results.

4.5.1.1 Host polling behavior

The host will need to go through a Status Register polling sequence to determine if an initialization failure has occurred in the device. The flowchart for the sequence is shown in **Figure 53**.

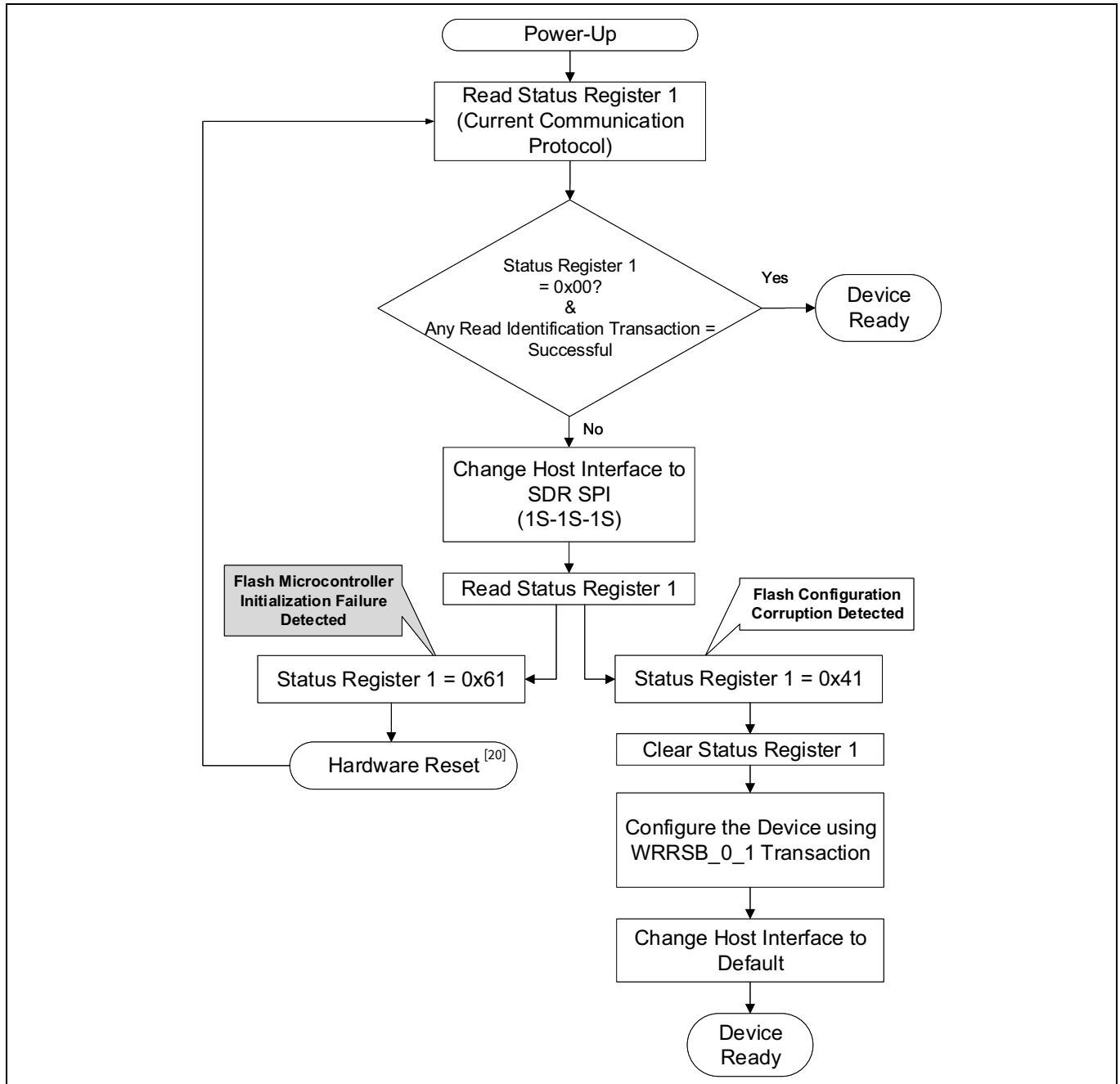


Figure 53 Host polling sequence for microcontroller initialization failure detection

Note The polling sequence must start from the higher I/O interface configuration to lower I/O interface configuration only. For example, 4S-4D-4D to 1S-1S-1S.

Note

²⁰. If you have Vcc within specifications and a hardware reset does not resolve the issue, replace the flash device.

Features

4.5.1.2 Microcontroller initialization failure detection related registers and transactions

Table 23 Microcontroller initialization failure related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|---|--|--|
| Status Register 1 Volatile (STR1V) (see Table 41 on page 73) | Read Any Register (RDARG_C_0) Read Status Register -1 (RDSR1_0_0) | N/A |

4.5.2 Configuration corruption detection

If during device's configuration update, such as writing to a nonvolatile register, a power loss occurs or a hardware reset is initiated, the write register transaction will get interrupted. The device will return to Standby mode, but the nonvolatile register data is most likely corrupted since the embedded write operation was prematurely terminated. During the next power-up, the configuration corruption is detected and the device reverts to its Default Boot mode (1S-1S-1S) and allows rewriting the configuration again. The device will maintain the configured protection scheme.

Table 24 shows the device's Status Register bits upon detecting a configuration corruption.

Table 24 Status Register 1 configuration corruption detection signature

| Bit | Field name | Function | Detection signature |
|----------|-------------|---|---------------------|
| STR1V[7] | STCFWR | Status Register and Configuration Registers Protection Selection against write (erase/program) | 0 |
| STR1V[6] | PRGERR | Programming Error Status Flag | 1 |
| STR1V[5] | ERSERR | Erasing Error Status Flag | 0 |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection Note LBPROT[2:0] can be anything from 000 to 111 based on Block Protection configuration. | 0 |
| STR1V[3] | | | 0 |
| STR1V[2] | | | 0 |
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | 0 |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | 1 |

Table 25 Interface configuration upon detecting configuration corruption

| Interface | Transactions supported | Address (# of bytes) | Frequency of operation | Register read latency (# of clock cycles) | Output impedance |
|----------------|---------------------------------|----------------------|------------------------|---|------------------|
| SPI (1S-1S-1S) | All SPI (1S-1S-1S) Transactions | 4 | Maximum | 2 | 45Ω |

4.5.2.1 Host polling behavior

The host will need to go through a Status Register polling sequence to determine if a Configuration corruption has occurred in the device. The flowchart for the sequence is shown in [Figure 54](#).

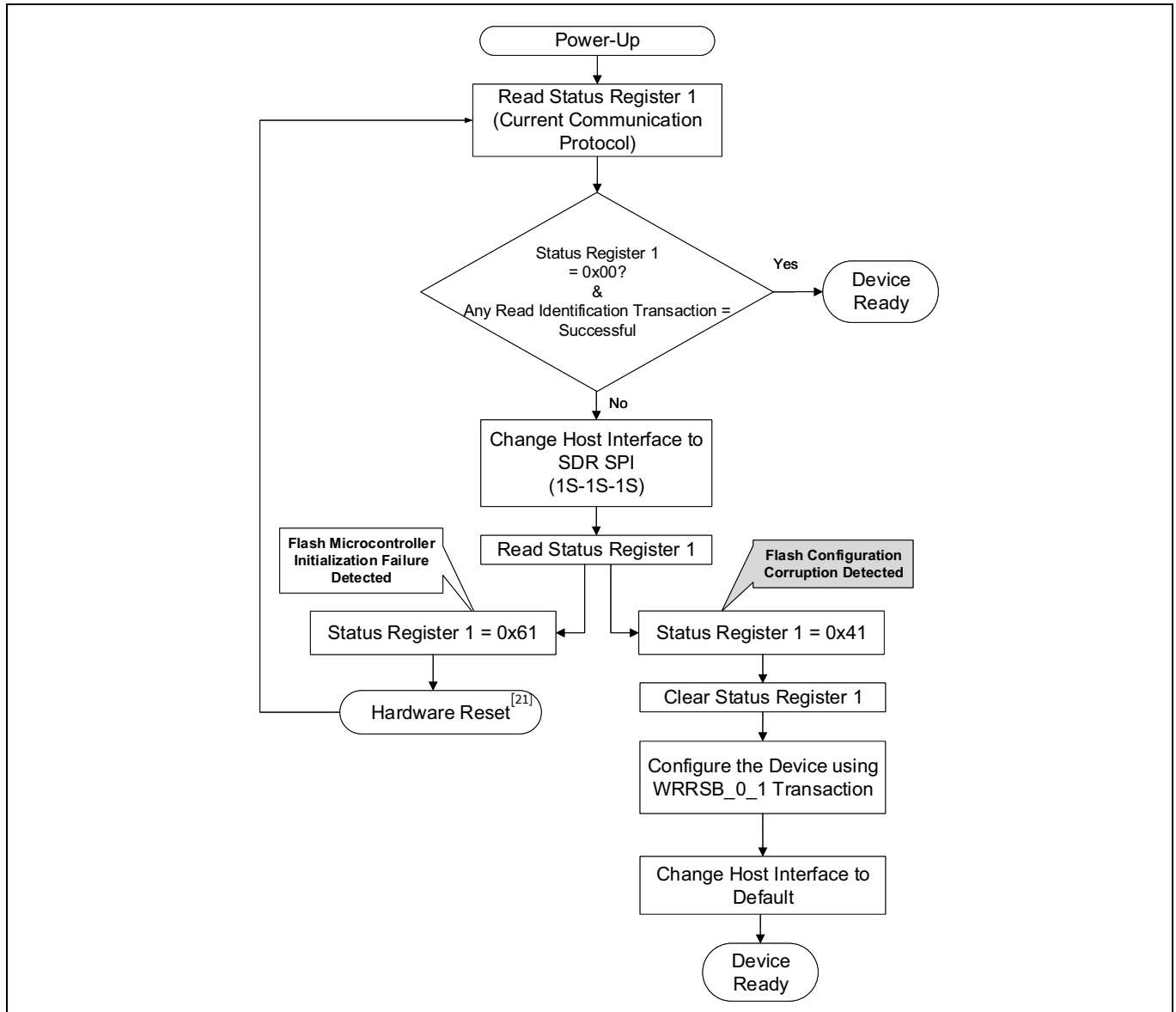


Figure 54 Host polling sequence for configuration corruption detection

Note The polling sequence must start from a higher I/O interface configuration to a lower I/O interface configuration. As an example, 4S-4D-4D to 1S-1S-1S. Not the other way around.

Note

21. If you have Vcc within specifications and a hardware reset does not resolve the issue, replace the flash device.

Features

4.5.2.2 Configuration corruption detection related registers

Table 26 Configuration corruption detection related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|---|
| Status Register 1 Volatile (STR1V) (see Table 41 on page 73) | All 1S-1S-1S Transactions | N/A |

4.6 AutoBoot

AutoBoot allows the host to read data from HL-T/HS-T family of devices after power up or after a hardware reset without having to send any read transactions (including the address). Based on the device configuration, data is output on the interface I/Os once CS# is brought LOW and CK is toggled.

The starting address for the read data is specified in the AutoBoot Register (ATBN[31:9] - STADR[22:0]). This starting address can be at any page boundary location in the memory (512 byte page boundary). Also identified in the AutoBoot Register is a starting delay which is represented as the number of clock cycles (ATBN[8:1] - STDLY[7:0]). This delay is instituted before the data is read out. The delay can be programmed to meet the host's requirements but a minimum amount is required to meet the memory access times based on the frequency for operation. It is highly recommended to check the Status Register 1 value after successful or unsuccessful AutoBoot execution to verify the configuration corruption (SafeBoot).

Note Wrap function must be disabled for AutoBoot.

Note AutoBoot is disabled when the Read Password feature is enabled, as part of the Advanced Sector Protection. It is recommended to disable AutoBoot (ATBN[0] - ATBTEN) when Read Password feature is enabled.

Note It is highly recommended to assign first AutoBoot address in the Long Retention region.

4.6.1 AutoBoot related registers and transactions

Table 27 AutoBoot related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|---|
| AutoBoot Register (ATBN) (see Table 66 on page 87) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |
| | AutoBoot Transaction (see Figure 15 on page 15) | AutoBoot QPI Transaction (see Figure 26 on page 18) |

4.7 Read

HL-T/HS-T supports different read transactions to access different memory maps, namely: Read Memory array, Read Device Identification, Read Register, Read Secure Silicon, Read Protection DYB and PPB bits.

These read transactions can use any protocol mentioned in the Transaction Protocols section and potentially can use the following features:

- The read transactions require latency cycles following the address to allow time to access the memory array (except RDAY1_4_0 and RDAY1_C_0 of 1S-1S-1S protocol) (see [Table 49](#)).
- The read transactions can use the Data Learning Pattern (DLP) driven by the memory, on all data outputs, in the latency cycles immediately before the start of data (see [Data learning pattern \(DLP\) on page 54](#)).
- The read transaction has the option of wrapped read length and alignment groups of 8-, 16-, 32-, or 64-bytes (see [Table 52](#) and [Table 53](#)).

4.7.1 Read identification transactions

There are three unique identification transactions, each support Single and Quad SPI Protocols (see [Transaction table on page 91](#)).

4.7.1.1 Read device identification transaction

The Read Device Identification (RDIDN_0_0) transaction provides read access to manufacturer identification and device identification. The transaction uses latency cycles set by (CFR3V[7:6]) to enable maximum clock frequency of 166MHz.

4.7.1.2 Read quad identification

The Read Quad Identification (RDQID_0) transaction provides read access to manufacturer identification, device identification information. This transaction is an alternate way of reading the same information provided by the RDIDN_0_0 transaction while in QPI mode. In all other respects the transaction behaves the same as the RDIDN_0_0 transaction.

The transaction is recognized only when the device is in Quad mode (CFR1V[1] = 1). The instruction is shifted in on DQ0-DQ3. After the last bit of the instruction is shifted into the device, then dummy cycles then, one byte of manufacturer identification and two bytes of device identification will be shifted sequentially out on DQ0-DQ3. Continued shifting of output beyond the end of the defined ID address space will provide undefined data. The maximum clock frequency for the transaction is 166MHz.

4.7.1.3 Read SFDP transaction

The Read Serial Flash Discoverable Parameters (RSFDP_3_0) transaction provides access to the JEDEC Serial Flash Discovery Parameters (SFDP) (see [Transaction table on page 91](#)). The transaction uses a 3-byte address scheme. If a non-zero address is set, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. Continuous (sequential) read is supported with the RSFDP_3_0 transaction. Eight latency cycles are required. Read SFDP Transaction is not supported in Read Password mode before the password is provided. The maximum clock frequency for the Read SFDP transaction is 50MHz.

4.7.1.4 Read unique identification transaction

Read Unique Identification (RDUID_0_0) transaction is similar to Read Device Identification transaction, but accesses a different 64-bit number which is unique to each device. It is factory programmed.

4.7.1.5 Read identification related register and transaction

Table 28 Read identification related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|---|--|---|
| Configuration Register 3 (CFR3N, CFR3V) (see Table 50 on page 80) | Read Identification (RDIDN_0_0) | Read Identification (RDIDN_0_0) |
| | Read Serial Flash Discoverable (RSFDP_3_0) | Read Serial Flash Discoverable (RSFDP_3_0) |
| | Read Unique Identification (RDUID_0_0) | Read Unique Identification (RDUID_0_0) |
| | | Read Quad Manufacturer and Device Identification (RDQID_0_0) |

4.7.2 Read memory array transactions

Memory array data can be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

4.7.2.1 SPI read and read fast transactions

The SPI Read SDR and Read Fast SDR transactions (1S-1S-1S) are supported for Host systems that require backward compatibility to legacy SPI. Read Fast SDR transaction is available with 3- or 4-byte address options. This protocol does not support the DLP for capture of data. The option of wrapped read length is available. The Read transaction is for maximum clock frequency of 50MHz and requires no latency cycles. The Fast Read Transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum clock frequency of 166MHz (see [Transaction table on page 91](#)).

The Read Fast 4-Byte transaction has continuous read mode bits that follow the address so, a series of Read Fast 4-Byte transactions can eliminate the eight-bit command after the first Read Fast 4-Byte command sends a mode bit pattern of Axh that indicates the following transaction will also be a Read Fast 4-Byte command. The first Read Fast 4-Byte command in a series starts with the 8-bit command, followed by address, followed by eight cycles of mode bits, followed by an optional latency period. If the mode bit pattern is Axh the next transaction is assumed to be an additional Read Fast 4-Byte transaction that does not provide command bits. That transaction starts with address, followed by mode bits, followed by optional latency. Then the memory contents, at the address given, are shifted out on DQ1_SO.

4.7.2.2 Read SDR dual I/O transaction

The Read SDR Dual I/O transaction provides high data throughput using Dual I/O SDR (1S-2S-2S) protocol. This protocol does not support DLP for capture of data. The option of wrapped read length is available. It supports 3- or 4-byte address options. It supports the mode bits and continuous read transactions. This transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum 166MHz clock frequency (see [Transaction table on page 91](#)).

4.7.2.3 Read SDR quad output transaction

The Read SDR Quad Output transaction uses the SDR Quad Output (1S-1S-4S) protocol. This protocol supports the DLP for capture of data. The option of wrapped read length is available. It supports 3- or 4-byte address options. This transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum 166MHz clock frequency (see [Transaction table on page 91](#)).

4.7.2.4 Read SDR and DDR quad I/O transaction

The Read SDR Quad I/O transaction uses the SDR Quad I/O (1S-4S-4S) protocol and Read DDR Quad I/O transaction uses the DDR Quad I/O (1S-4D-4D) protocol. These protocols supports the DLP for capture of data. The option of wrapped read length is available. Both transactions also support the mode bits and continuous read transactions. In SDR Quad I/O transaction, the mode bit pattern is Axh and the next transaction is assumed to be an additional SDR Quad I/O transaction that does not provide command bits.

In DDR Quad I/O transaction, the mode bit pattern is A5h and the next transaction is assumed to be an additional DDR Quad I/O transaction that does not provide command bits. They support 3- or 4-byte address options. These transactions use latency cycles set by (CFR2V[3:0]) to enable maximum 166MHz clock frequency (see [Transaction table on page 91](#)).

4.7.2.5 Read QPI SDR and DDR transaction

The Read QPI SDR transaction uses the SDR QPI(4S-4S-4S) protocol and Read QPI DDR transaction uses the DDR QPI (4S-4D-4D) protocol. These protocols supports the DLP for capture of data. The option of wrapped read length is available. Both transactions also support the mode bits and continuous read transactions. In SDR QPI transaction, the mode bit pattern is Axh and the next transaction is assumed to be an additional SDR QPI transaction that does not provide command bits.

In DDR QPI transaction, the mode bit pattern is A5h and the next transaction is assumed to be an additional DDR QPI transaction that does not provide command bits. They support 3- or 4-byte address options. These transactions use latency cycles set by (CFR2V[3:0]) to enable maximum 166MHz clock frequency (see [Transaction table on page 91](#)).

4.7.2.6 Read memory array related registers and transactions

Table 29 Read memory array related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related dual I/O transactions (see Table 74 on page 96) | Related quad SPI transactions (see Table 77 on page 98) |
|---|--|---|---|
| Configuration Register 2 (CFR2N, CFR2V) (see Table 48 on page 78) | Read SDR (RDAY1_4_0, RDAY1_C_0) | Read SDR Dual I/O (RDAY3_4_0, RDAY3_C_0) | Read SDR Quad Output (RDAY4_4_0, RDAY4_C_0) |
| Configuration Register 4 (CFR4N, CFR4V) (see Table 52 on page 81) | Read Fast SDR (RDAY2_4_0, RDAY2_C_0) | Continuous Read SDR Dual I/O (RDAY6_4_0, RDAY6_C_0) | Read SDR Quad I/O (RDAY5_4_0, RDAY5_C_0) |
| Data Learning Pattern (DLPN, DLPV) (see Table 63 on page 87) | - | - | Continuous Read SDR Quad I/O (RDAY6_4_0, RDAY6_C_0) |
| | - | - | Read DDR Quad I/O (RDAY7_4_0, RDAY7_C_0) |
| | - | - | Continuous Read DDR Quad I/O (RDAY8_4_0, RDAY8_C_0) |
| | - | - | Read QPI SDR (RDAY5_4_0, RDAY5_C_0) |
| | - | - | Continuous Read QPI SDR (RDAY6_4_0, RDAY6_C_0) |
| | - | - | Read QPI DDR (RDAY7_4_0, RDAY7_C_0) |
| | - | - | Continuous Read QPI DDR (RDAY8_4_0, RDAY8_C_0) |

4.7.3 Read registers transactions

There are multiple registers for reporting embedded operation status or controlling device configuration options. Registers contain both volatile and nonvolatile bits. There are two ways to read the Registers. The Read Any Register transaction provides a way to read all device registers: nonvolatile and volatile by address selection. There are also dedicated Register Read transactions, which are defined per register and only read the contents of that register.

4.7.3.1 Read any register

The Read Any Register (RDARG_C_0) transaction is the best way to read all device registers, both nonvolatile and volatile. The transaction includes the address of the register to be read (see [Transaction table on page 91](#)). This is followed by a number of latency cycles set by (CFR2V[3:0]) for reading nonvolatile registers and CFR3V[7:6] for reading volatile registers. See [Table 49](#) for NV Registers latency cycles and [Table 51](#) for Volatile Registers latency cycles. Then, the selected register contents are returned. If the read access is continued, the same addressed register contents are returned until the transaction is terminated; only one byte register location is read by each RDARG_C_0 transaction. For registers with more that one byte of data, the RDARG_C_0 transaction must again be used to read each byte of data.

The maximum clock frequency for the RDARG_C_0 transaction is 166MHz.

The RDARG_C_0 transaction can be used during embedded operations to read Status Register 1 (STR1V). It is not used for reading registers such as ASP PPB Access Register (PPAV) and ASP Dynamic Block Access Register (DYAV). There are separate commands required to select and read the location in the array accessed. The RDARG_C_0 transaction will read invalid data from the PASS Register locations if the ASP Password protection mode is selected by programming ASPR[2:0]. Reading undefined locations provides undefined data.

4.7.3.2 Read status registers transaction

The Read Status Register (RDSR1_0_0, RDSR2_0_0) transactions allow the Status Registers' volatile contents to be read. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166MHz.

The volatile version of Status Registers contents can be read at any time, even while a program, erase, or write operation is in progress.

It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

4.7.3.3 Read configuration register transaction

The Read Configuration Register (RDCR1_0_0) transaction allows the Configuration registers volatile contents be read. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166MHz.

The volatile version of Status Registers contents can be read at any time, even while a program, erase, or write operation is in progress.

It is possible to read Configuration Registers continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

4.7.3.4 Read dynamic protection bit (DYB) access register transaction

The Read DYB Access Register (RDDYB_4_0, RDDYB_C_0) transaction reads the contents of the DYB Access Register. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166MHz. It is possible to read DYB Access register continuously, however the address of the DYB register does not increment, so the entire DYB array cannot be read in this fashion. Each location must be read with a separate Read DYB transaction.

4.7.3.5 Read persistent protection bit (PPB) access register transaction

The Read PPB Access Register (RDPBB_4_0, RDPBB_C_0) transaction reads the contents of the PPB Access Register. The transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum clock frequency of 166MHz. It is possible to read PPB Access Register continuously, however the address of the PPB register does not increment, so the entire PPB array cannot be read in this fashion. Each location must be read with a separate Read PPB transaction.

4.7.3.6 Read PPB lock registers transaction

The Read PPB Lock Register (RDPLB_0_0) transactions allow the content of the nonvolatile registers to be read. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166MHz. It is possible to read PPB Lock Bit continuously.

4.7.3.7 Read ECC data unit status

The Read ECC Data Unit Status (RDECC_4_0, RDECC_C_0) transaction is used to determine the ECC status of the addressed unit data. In this transaction, the LSb of the address must be aligned to an ECC data unit. This transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166MHz.

The byte contents of the ECC Status for the selected ECC unit is then output. Any following data will be indeterminate. To read the next ECC unit status, another RDECC_4_0 or RDECC_C_0 transaction should be sent out to the next address, incremented by 16 [Data Unit size/8] bytes.

Features

4.7.3.8 Read register related registers and transactions

Table 30 Read register related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|---|--|
| Configuration Register 2 (CFR2N, CFR2V) (see Table 48 on page 78) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| | Read Status Register 1 (RDSR1_0_0) | Read Status Register 1 (RDSR1_0_0) |
| Configuration Register 3 (CFR3N, CFR3V) (see Table 50 on page 80) | Read Status Register 2 (RDSR2_0_0) | Read Status Register 2 (RDSR2_0_0) |
| | Read DYB (RDDYB_4_0, RDDYB_C_0) | Read DYB (RDDYB_4_0, RDDYB_C_0) |
| | Read PPB (RDPPB_4_0, RDPPB_C_0) | Read PPB (RDPPB_4_0, RDPPB_C_0) |
| | Read PPB Lock (RDPLB_0_0) | Read PPB Lock (RDPLB_0_0) |
| | Read ECC Status (RDECC_4_0, RDECC_C_0) | Read ECC Status (RDECC_4_0, RDECC_C_0) |
| | Read Configuration Register 1 (RDCR1_0_0) | Read Configuration Register 1 (RDCR1_0_0) |

4.7.4 Data learning pattern (DLP)

The device supports Data Learning Pattern (DLP) which allows the host controller to optimize the data capture window. The READ preamble training is only available in Quad Mode READs. The programmable training pattern is stored in a DLP Register. To enable training, a non-zero pattern must be stored in the DLP Register. The device outputs the pattern during the latency cycles. Bus Turnaround between the end of the address input by the host and the pattern output by the device is not a concern since the first three latency clock cycles are treated as dummy cycles. All IO signals transition the same data learning pattern bits.

The device outputs the learning pattern during latency cycles. The pattern driven on the IO signals depends on the number of latency cycles available for the READ transaction. If the latency is set to at least 9 clock cycles for SDR operation, the device will output the pattern on the IOs on the last 8 clock cycles before outputting the READ data. However, if the latency is set to less than 9 clock cycles, no data learning pattern is outputted. If the latency is set to at least 5 clock cycles for DDR operation, the device will output the pattern on the IOs on the last 4 clock cycles before outputting the READ data. However, if the latency is set to less than 4 clock cycles, no data learning pattern is outputted.

4.7.4.1 Data learning pattern related registers and transactions

Table 31 DLP related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|---|--|
| Data Learning Register (DLPN, DLPV) (see Table 48 on page 78) | Program Data Learning Pattern (PRDLP_0_1) | Program Data Learning Pattern (PRDLP_0_1) |
| | Write Data Learning Pattern (WRDLP_0_1) | Write Data Learning Pattern (WRDLP_0_1) |
| | Read Data Learning Pattern Register (RDDLP_0_0) | Read Data Learning Pattern Register (RDDLP_0_0) |

4.8 Write

There are write transactions for writing to the Registers. These write transactions can use the SPI and Quad SPI protocols as mentioned in the Transaction Protocols section:

4.8.1 Write enable transaction

The Write Enable (WRENB_0_0) transaction sets the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to 1. The WRPGEN bit must be set to 1 by issuing the Write Enable (WRENB_0_0) Transaction to enable write, program, and erase transactions (see [Transaction table on page 91](#)).

4.8.2 Write enable for volatile registers

The volatile Status and Configuration registers, can be written by sending the WRENV_0_0 transaction followed by any write register transactions. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical nonvolatile bit write cycles or affecting the endurance of the status or configuration nonvolatile register bits. The WRENV_0_0 transaction is used only to direct the following write register transaction to change the volatile status and configuration register bit values.

4.8.3 Write disable transaction

The Write Disable (WRDIS_0_0) transaction clears the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to 0.

The WRPGEN bit can be cleared to 0 by issuing the Write Disable (WRDIS_0_0) transaction to disable commands that requires WRPGEN be set to 1 for execution. The WRDIS_0_0 transaction can be used by the user to protect memory areas against inadvertent write, program, or erase operations that can corrupt the contents of the memory. The WRDIS_0_0 transaction is ignored during an embedded operation while RDYBSY bit = 1 (STR1V[0]) (see [Transaction table on page 91](#)).

4.8.4 Clear program and erase failure flags transaction

The Clear Program and Erase Failure Flags (CLPEF_0_0) transaction resets bit STR1V[5] (Erase Error Flag) and bit STR1V[6] (Program Error Flag) to 0. This transaction will be accepted even when the device remains busy with RDYBSY set to 1, as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this transaction is executed (see [Transaction table on page 91](#)).

4.8.5 Clear ECC status register transaction

The Clear ECC Status Register (CLECC_0_0) transaction resets bit ECSV[4] (2-bit ECC Detection), bit ECSV[3] (1-bit ECC Correction), INSV[1:0] ECC detection status bits, Address Trap Register EATV[31:0], and ECC Detection Counter ECTV[15:0]. It is not necessary to set the WRPGEN bit before this transaction is executed. The Clear ECC Status Register transaction will be accepted even when the device remains busy with WRPGEN set to 1, as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this command is executed (see [Transaction table on page 91](#)).

4.8.6 Write registers transactions

The Write Registers (WRREG_0_1) transaction allows new values to be written to both the Status and Configuration Registers. Before the Write Registers transaction can be accepted by the device, a Write Enable or Write Enable for Volatile Registers transaction must be received. After the Write Enable command has been decoded successfully, the device will set the WRPGEN in the Status Register to enable any write operations.

The Write Registers transaction is entered by shifting the instruction and the data bytes on DQ0_SI. The Status and Configuration Registers are one data byte in length.

The WRR operation first erases the register then programs the new value as a single operation. The Write Registers transaction will set the PRGERR or ERSERR bits if there is a failure in the WRREG_0_1 operation.

4.8.7 Write any register transaction

The Write Any Register (WRARG_C_1) transaction provides a way to write any device register, nonvolatile or volatile. The transaction includes the address of the register to be written, followed by one byte of data to write in the addressed register (see [Transaction table on page 91](#)).

Before the WRARG_C_1 transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded, which sets the Write/Program Enable bit (WRPGEN) in the Status Register to enable any write operations. The RDYDSY bit in STR1V[0] can be checked to determine when the operation is completed. The PRGERR and ERSERR bits in STR1V[6:5] can be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits can be modified. Some bits are read only, some are OTP, and some are designated Reserved (DNU).

Read only bits are never modified and the related bits in the WRARG_C_1 transaction data byte are ignored without setting a program or erase error indication (PRGERR or ERSERR in STR1V[6:5]). Hence, the value of these bits in the WRARG_C_1 data byte do not matter.

OTP bits can only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Nonvolatile bits which are changed by the WRARG_C_1 data, require nonvolatile register write time (t_w) to be updated. The update process involves an erase and a program operation on the nonvolatile register bits. If either the erase or program portion of the update fails, the related error bit and RDYBSY bit in STR1V will be set to 1.

Status Register 1 can be repeatedly read (polled) to monitor the RDYBSY bit (STR1V[0]) and the error bits (STR1V[6,5]) to determine when the register write is completed or failed. If there is a write failure, the CLPEF_0_0 transaction is used to clear the error status and enable the device to return to standby state.

The ASP PPB Lock Register (PPLV) register cannot be written by the WRARG_C_1 transaction. Only the Write PPB Lock Bit (WRPLB_0_0) transaction can write the PPLV Register.

The Data Integrity Check Register cannot be written by the WRARG_C_1 transaction. The Data Integrity Check Register is loaded by running the Data Integrity Check transaction (DICHK_4_1).

4.8.8 Write PPB lock bit

The Write PPB Lock Bit (WRPLB_0_0) transaction clears the PPB Lock Register PPLV[0] to zero. The PPBLCK bit is used to protect the PPB bits. When PPLV[0] = 0, the PPB Program/Erase transaction will be aborted. In Read Password Protection mode, PPBLCK bit is also used to control the high order bits of the address by forcing the address range to be limited to one sector where boot code is stored, until the read password is supplied (see [Transaction table on page 91](#)).

Before the WRPLB_0_0 transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded by the device, which sets the Write/Program Enable (WRPGEN) in the Status Register 1 to enable any write operations.

While the operation is in progress, the Status Register can still be read to check the value of the RDYBSY bit. The WRPGEN bit is a 1 during the self-timed operation, and is a 0 when it is completed. When the Write PPB Lock transaction is completed, the RDYBSY bit is set to a 0 (see [Transaction table on page 91](#)).

Features

4.8.9 Write transactions related registers and transactions

Table 32 Write transactions related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|---|---|--|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| | Write Registers (WRREG_0_1) | Write Registers (WRREG_0_1) |
| | Write Enable Volatile (WRENV_0_0) | Write Enable Volatile (WRENV_0_0) |
| | Write Disable (WRDIS_0_0) | Write Disable (WRDIS_0_0) |
| ECC Status Register (ECSV) (see Table 55 on page 83) | Clear Program and Erase Failure Flags (CLPEF_0_0) | Clear Program and Erase Failure Flags (CLPEF_0_0) |
| | Clear ECC Status Register (CLECC_0_0) | Clear ECC Status Register (CLECC_0_0) |
| Address Trap Register (EATV) (see Table 56 on page 83) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_C_1) |
| ECC Detection Counter (ECTV) (see Table 57 on page 84) | Write PPB Lock Bit (WRPLB_0_0) | Write PPB Lock Bit (WRPLB_0_0) |

4.9 Program

There are program transactions for programming data to the Memory Array, Secure Silicon Region and Persistent Protection Bits.

These program transactions can use SPI or Quad SPI protocols:

Before any program transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded by the device. Program transactions can only be executed by the device if the Write/Program Enable (WRPGEN) in the Status Register is set to '1' to enable program operations. When a program transaction is completed, the WRPGEN bit is reset to a '0'.

While the program transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a '1' during the self-timed program transaction, and is a '0' when it is completed.

The PGMERR bit in STR1V[6] may be checked to determine if any error occurred during the program transaction.

A program transaction applied to a sector that has been Write Protected through any of the protection schemes, will not be executed and will set the PGMERR status fail bit.

The program transactions will be initiated when CS# is driven into the logic HIGH state.

4.9.1 Program granularity

The HS/L-T family supports multi-pass programming (bit walking) where programming a "0" over a "1" without performing the sector erase operation. Bit-walking is allowed for the non-AEC-Q100 industrial temperature range (–40°C to +85°C) of this device. It is required to perform only one programming operation (single-pass programming) on each ECC data unit between erase operations for the higher temperature range (–40°C to +105°C) and (–40°C to +125°C) devices and all AEC-Q100 devices.

Multi-pass programming without an erase operation will disable the device's ECC functionality for that data unit. Note that if 2-bit ECC is enabled, multi-pass Programming within the same sector will result in a Program Error.

4.9.2 Page programming

Page Programming is done by loading a Page Buffer with data to be programmed and issuing a programming transaction to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming transaction. Page Programming allows up to a page size (either 256- or 512-bytes) to be programmed in one operation. The page size is determined by the Configuration Register 3 bit CFR3V[4]. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each Page Programming operation. It is recommended that a multiple of 16-byte length and aligned Program Blocks be written. This ensures that ECC is not disabled. For the very best Page Program throughput, programming should be done in full pages of 512 bytes aligned on 512-byte boundaries with each Page being programmed only once.

4.9.3 Program page transaction

The Program Page transaction (PRPGE_4_1, PRPGE_C_1) programs data into the memory array. If data more than a page size (256B or 512B) is sent to the device, then the space between the starting address and the page aligned end boundary, the data loading sequence will wrap from the last byte in the page to the zero byte location of the same page and begin overwriting any data previously loaded in the page. If less than a page of data is sent to the device, then the sent data bytes will be programmed in sequence, starting at the provided address within the page, without having any effect on the other bytes of the same page. The programming process is managed by the device internal control logic. The PRGERR bit indicates if an error has occurred in the programming transaction that prevents successful completion of programming. This includes attempted programming of a protected area (see [Transaction table on page 91](#)).

4.9.4 Program secure silicon region transaction

The Program Secure Silicon transaction (PRSSR_C_1) programs data in the SSR, which is in a different address space from the main array data and is OTP. The SSR is 1024 bytes, so the address bits from A31 to A10 must be zero for this transaction (see [Transaction table on page 91](#)). It is required to align start address to 32 bits while programming SSR space, which means the address bits A1 and A0 should be 0'b and host should deassert CS# to align with 32 bits.

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to 1.

Each SSR memory space can be programmed one or more times, provided that the region is not locked.

Attempting to program zeros in a region that is locked will fail with the PRGERR bit in STR1V[6] set to 1.

Programming once, even in a protected area does not cause an error and does not set PRGERR bit. Subsequent programming can be performed only on the unprogrammed bits (that is, 1 data). Programming more than once within an ECC unit will disable ECC on that data unit.

4.9.5 Program persistent protection bit (PPB)

The Program Persistent Protect Bit (PRPPB_4_0, PRPPB_C_0) transaction programs a bit in the PPB Register to protect the sector of the provided address from being programmed or erased (see [Transaction table on page 91](#)).

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation. Program PPB bit transaction will abort when trying to program the PPB bits protected by ASPPPB (ASPO[3]), ASPPRM (ASPO[0]) and PPBLCK (PPLV[0]) bit.

4.9.6 Program related registers and transactions

Table 33 Program related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|---|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| | Program Page (PRPGE_4_1, PRPGE_C_1) | Program Page (PRPGE_4_1, PRPGE_C_1) |
| Advance Sector Protect Register (ASPO) (see Table 58 on page 84) | Program Secure Silicon (PRSSR_C_1) | Program Secure Silicon (PRSSR_C_1) |
| ASP PPB Lock (PPLV) (see Table 60 on page 86) | Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0) | Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0) |
| ECC Status Register (ECSV) (see Table 55 on page 83) | Clear Program and Erase Failure Flags (CLPEF_0_0) | Clear Program and Erase Failure Flags (CLPEF_0_0) |

4.10 Erase

There are erase transactions for erasing data bits to 1 (all bytes are FFh) for the Memory Array and Persistent Protection Bits.

Before any erase transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded by the device. Erase transactions can only be executed by the device if the Write/Program Enable bit (WRPGEN) in the Status Register is set to '1' to enable erase operations. When an erase transaction is completed, the WRPGEN bit is reset to a '0'.

While the erase transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a '1' during the self-timed erase transaction, and is a '0' when it is completed.

The ERSERR bit in STR1V[5] can be checked to determine if any error occurred during the erase transaction.

An erase transaction applied to a sector that has been Write Protected through the Block Protection bits or ASP, will not be executed and will set the ERSERR status fail bit.

Erase transactions will be initiated when CS# is driven into the logic HIGH state.

When the device is shipped from the factory the default erase state is all bytes are FFh.

4.10.1 Erase 4KB sector transaction

The Erase 4KB Sector (ER004_4_0, ER004_C_0) transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh) (see [Transaction table on page 91](#)).

This transaction is ignored when the device is configured for uniform sectors only (CFR3V[3] = 1). If the Erase 4KB sector transaction is issued to a non-4KB sector address, the device will abort the operation and will not set the ERSERR status fail bit.

4.10.2 Erase 256KB sector transaction

The Erase 256KB Sector (ER256_4_0, ER256_C_0) transaction sets all bits in the addressed sector to 1 (all bytes are FFh) (see [Transaction table on page 91](#)).

A device configuration option (CFR3V[3]) determines if the Hybrid Sector Architecture is in use. When CFR3V[3] = 0, 4KB sectors overlay a portion of the highest or lowest address 128KB or 64KB of the device address space. If a sector erase transaction is applied to a 256KB sector that is overlaid by 4KB sectors, the overlaid 4KB sectors are not affected by the erase. Only the visible (non-overlaid) portion of the 128KB or 192KB sector is erased. When CFR3V[3] = 1, there are no 4KB sectors in the device address space and the Sector Erase transaction always operates on fully visible 256KB sectors.

When BLKCHK is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to be erased, the erase operation is aborted. The erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally.

4.10.3 Erase chip transaction

The Erase Chip (ERCHP_0_0) transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array (see [Transaction table on page 91](#)).

An Erase Chip transaction can be executed only when the Block Protection (BP2, BP1, BP0) bits are set to 0's. If the BP bits are not zero, the transaction is not executed and ERSERR status fail bit is not set. The transaction will skip any sectors protected by the Advance Sector Protection DYB or PPB and the ERSERR status fail bit will not be set.

4.10.4 Erase persistent protection bit (PPB) transaction

The Erase PPB transaction (ERPPB_0_0) sets all PPB bits to 1 (see [Transaction table on page 91](#)). This transaction will abort if PPB bits are protected by ASPPPB (ASPO[3]), ASPPRM (ASPO[0]) and PPBLCK (PPLV[0]) bit.

4.10.5 Erase status and count

4.10.5.1 Evaluate erase status transaction

The Evaluate Erase Status (EVERS_C_0) transaction verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased, then the erase status bit (STR2V[2]) is set to 1. If the selected sector was not completely erased STR2V[2] is 0. The Write/Program Enable transaction (to set the WRPGEN bit) is not required before this transaction. However, the RDYBSY bit is set by the device itself and cleared at the end of the operation, as visible in STR1V[0] when reading status (see [Transaction table on page 91](#)).

The Evaluate Erase Status transaction can be used to detect when erase operations that have failed due to loss of power, reset, or failure during the erase operation. The transaction requires t_{EES} to complete and update the erase status in STR2V. The RDYBSY bit (STR1V[0]) can be read to determine when the Evaluate Erase Status transaction is completed. If a sector is found not erased with STR2V[2] = 0, the sector must be erased again to ensure reliable storage of data in the sector.

4.10.5.2 Sector erase count transaction

The Sector Erase Count (SEERC_C_0) transaction outputs the number of erase cycles for the addressed sector. The erase cycle count is stored in the Sector Erase Count (SECV[22:0]) Register, and can be read by using the Read Any Register transaction (RDARG_C_0). The RDYBSY bit is set by the device itself and cleared at the end of the operation, as visible in STR1V[0] when reading status (see [Transaction table on page 91](#)).

The transaction requires t_{SEC} to complete and update the SECV[22:0] Register. The RDYBSY bit (STR1V[0]) may be read to determine when the Sector Erase Count Transaction finished. The SECV[23] bit is used to determine if the reported sector erase count is corrupted and was reset.

4.10.6 Erase related registers and transaction

Table 34 Erase related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|---|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| Status Register 2 (STR2V) (see Table 44 on page 75) | Erase 4KB Sector (ER004_4_0, ER004_C_0) | Erase 4KB Sector (ER004_4_0, ER004_C_0) |
| | Erase 256KB Sector (ER256_4_0, ER256_C_0) | Erase 256KB Sector (ER256_4_0, ER256_C_0) |
| ASP PPB Lock (PPLV) (see Table 60 on page 86) | Erase Chip (ERCHP_0_0) | Erase Chip (ERCHP_0_0) |
| ECC Status Register (ECSV) (see Table 55 on page 83) | Evaluate Erase Status (EVERS_C_0) | Evaluate Erase Status (EVERS_C_0) |
| Sector Erase Count Register (SECV) (see Table 67 on page 88) | Sector Erase Count (SEERC_C_0) | Sector Erase Count (SEERC_C_0) |
| | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) |

4.11 Suspend and resume embedded operation

HL-T/HS-T device can interrupt and suspend the running embedded operations such as Erase, Program, or Data Integrity Check. It can also resume the suspended operation once the host finishes the intermediate operation and sends the respective resume transaction to the device.

4.11.1 Erase, program, or data integrity check suspend

The Suspend transaction allows the system to interrupt a program, erase, or data integrity check operation and then read from any other non erase-suspended sector, non-program-suspended-page or the array. The Device Ready/Busy Status Flag (RDYBSY) in Status Register 1 (STR1V[0]) must be checked to know when the program, erase, or data integrity check operation has stopped.

4.11.1.1 Program suspend

- Program Suspend is valid only during a programming operation.
- The Program Operation Suspend Status flag (PROGMS) in Status Register-2 (STR2V[0]) can be used to determine if a programming operation has been suspended or was completed at the time RDYBSY changes to 0.
- A program operation can be suspended to allow a read operation.
- Reading at any address within a program-suspended page produces undetermined data.

4.11.1.2 Erase suspend

- Erase Suspend is valid only during a sector erase operation.
- The Erase operation Suspend status flag (ERASES) in Status Register-2 (STR2V[1]) can be used to determine if an erase operation has been suspended or was completed at the time RDYBSY changes to 0.
- A Chip Erase operation cannot be suspended.
- An Erase operation can be suspended to allow a program operation or a read operation.
- During an erase suspend, the DYB array can be read to examine sector protection.
- A new erase operation is not allowed with an already suspended erase, program, or data integrity check operation. An erase transaction is ignored in this situation.
- Reading at any address within an erase-suspended sector produces undetermined data.

4.11.1.3 Data Integrity Check Suspend

- Data Integrity Check Suspend is valid only during a Data Integrity Check Calculation operation.
- The Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag (DICRCS) in Status Register-2 (STR2V[4]) can be used to determine if a data integrity check operation has been suspended or was completed at the time RDYBSY changes to 0.
- A data integrity check operation can be suspended to allow a read operation.

The Write Any Register or Erase Persistent Protection Bit transactions are not allowed during Erase, Program, or Data Integrity Check Suspend. It is therefore not possible to alter the Block Protection or PPB bits during Erase Suspend. If there are sectors that may need programming during Erase suspend, these sectors should be protected only by DYB bits that can be turned OFF during Erase Suspend.

The time required for the suspend operation to complete is t_{PEDS} .

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the RDYBSY bit in the Status Register 1, just as in the standard program operation.

Features

Table 35 lists the transactions allowed during the suspend operation.

Table 35 Transactions allowed during suspend

| Transaction name | Allowed during erase suspend | Allowed during program suspend | Allowed during data integrity check suspend |
|---|------------------------------|--------------------------------|---|
| Write Disable (WRDIS_0_0) | | No | No |
| Read Status Register 1 (RDSR1_0_0) | | Yes | Yes |
| Write Enable (WRENB_0_0) | | No | No |
| Write Enable Volatile (WRENV_0_0) | | | |
| Read Status Register 2 (RDSR2_0_0) | | Yes | Yes |
| Read Configuration Register 1 (RDCR1_0_0) | | No | No |
| Program Page (PRPGE_4_1, PRPGE_C_1) | | | |
| Read ECC Status (RDECC_4_0, RDECC_C_0) | | | |
| Clear ECC Status Register (CLECC_0_0) | | | |
| Read PPB Lock Bit (RDPLB_0_0) | | Yes | Yes |
| Resume Program / Erase / Data Integrity Check (RSEPD_0_0) | | | |
| Resume Program / Erase (RSEPA_0_0) | | | |
| Program SSR (PRSSR_C_1) | | No | No |
| Read SSR (RDSSR_C_0) | | Yes | |
| Read Unique ID (RDUID_0_0) | | | |
| Read SFDP (RSFDP_3_0) | | | |
| Read Quad Manufacturer and device Identification (RDQID_0_0) | Yes | | |
| Read Any Register (RDARG_C_0) | | | |
| Software Reset Enable (SRSTE_0_0) | | Yes | Yes |
| Clear Program and Erase Failure Flags (CLPEF_0_0) | | | |
| Software Reset (SFRST_0_0) | | | |
| Legacy Software Reset (SFRSL_0_) | | | |
| Read Identification Register (RDIDIN_0_0) (manufacturer and device identification) | | | |
| Suspend Program / Erase / Data Integrity Check (SPEPD_0_0) | | No | No |
| Suspend Program / Erase (SPEPA_0_0) | | | |
| Read DYB (RDDYB_4_0, RDDYB_C_0) | | | Yes |
| Read PPB (RDPPB_4_0, RDPPB_C_0) | | | |
| Read SDR (RDAY1_C_0, RDAY1_4_0) | | | |
| Read Fast SDR (RDAY2_C_0, RDAY2_4_0) | | Yes | |
| Read SDR Dual I/O (RDAY3_C_0, RDAY3_4_0) | | | |
| Read SDR Quad Output (RDAY4_C_0, RDAY4_4_0) | | | |
| Read SDR Quad I/O (RDAY5_C_0, RDAY5_4_0) | | | |
| Read DDR Quad I/O (RDAY7_C_0, RDAY7_4_0) | | | |
| Read Data Learning Pattern (RDDLP_0_0) | Yes | Yes | Yes |

4.11.2 Erase, program, or data integrity check resume

An Erase, Program, or Data Integrity Check Resume transaction must be written to resume a suspended operation. After program or read operations are completed during a Program, Erase or Data Integrity Check suspend, the Resume transaction is sent to resume the suspended operation.

After an Erase, Program, or Data Integrity Check Resume transaction is issued, the RDYBSY bit in Status Register 1 will be set to a 1 and the programming operation will resume if one is suspended. If no program operation is suspended, the suspended erase operation will resume. If there is no suspended program, erase or data integrity check operation, the resume transaction is ignored.

Program, Erase, or Data Integrity Check operations may be interrupted as often as necessary. For example, a program suspend transaction could immediately follow a program resume transaction, but for a program or erase operation to progress to completion there must be some period of time between resume and the next suspend transaction greater than or equal to t_{PEDRS} .

Figure 55 shows the flow of suspend and resume operation.

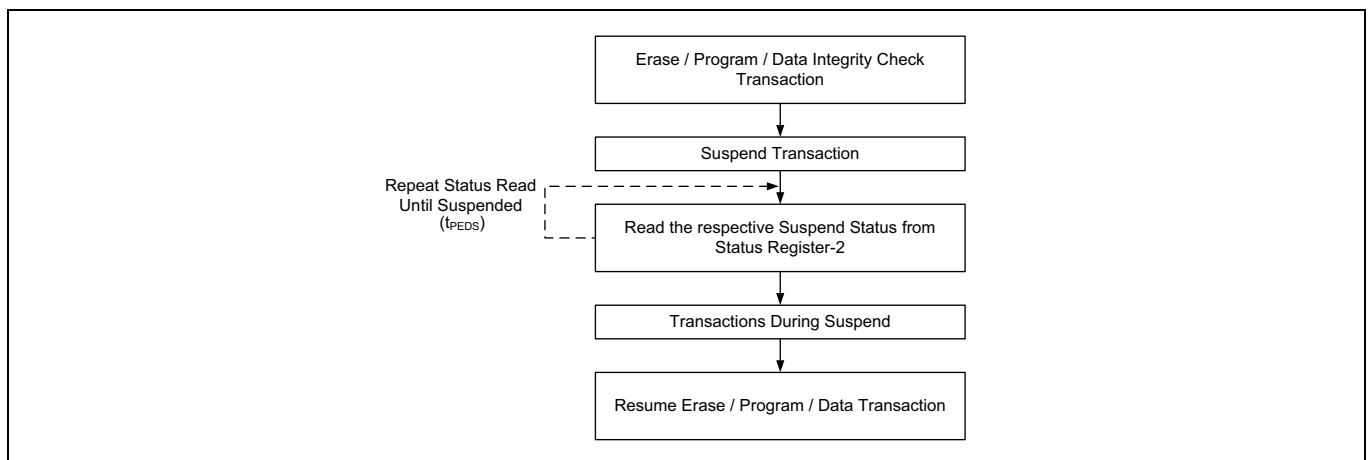


Figure 55 Suspend and resume sequence

4.11.3 Suspend and resume related registers and transactions

Table 36 Erase related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|--|---|
| Status Register 1 (STR1N, STR1V) (see Table 41 on page 73) | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0) | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0) |
| Status Register 2 (STR2V) (see Table 44 on page 75) | Resume Erase / Program / Data Integrity Check (RSEPD_0_0) | Resume Erase / Program / Data Integrity Check (RSEPD_0_0) |
| | Suspend Erase / Program (SPEPA_0_0) | Suspend Erase / Program (SPEPA_0_0) |
| | Resume Erase / Program (RSEPA_0_0) | Resume Erase / Program (RSEPA_0_0) |
| | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_C_0) |
| | Read Status Register -1 (RDSR1_0_0) | Read Status Register -1 (RDSR1_4_0) |
| | Read Status Register - 2 (RDSR2_0_0) | Read Status Register - 2 (RDSR2_4_0) |

4.12 Reset

HL-T/HS-T devices support four types of reset mechanisms.

- Hardware Reset (using RESET# input pin and DQ3_RESET# pin)
- Power-on reset (POR)
- CS# signaling reset
- Software Reset

4.12.1 Hardware reset (using RESET# input pin and DQ3_RESET# pin)

The RESET# input initiates the reset operation with a transition from logic HIGH to logic LOW for $> t_{RP}$, and causes the device to perform the full reset process that is performed during POR. The hardware reset process requires a period of t_{RH} to complete. See [Table 84](#) for timing specifications.

The DQ3_RESET# input initiates the reset operation under the following when CS# is HIGH for more than t_{CS} time or when Quad or QPI mode is not enabled. The DQ3_RESET# input has an internal pull-up to V_{CC} and may be left unconnected if Quad or QPI mode is not used. The t_{CS} delay after CS# goes HIGH gives the memory or host system time to drive DQ3 HIGH after its use as a Quad or QPI mode I/O signal while CS# was LOW. The internal pull-up to V_{CC} will then hold DQ3_RESET# HIGH until the host system begins driving DQ3_RESET#. The DQ3_RESET# input is ignored while CS# remains HIGH during t_{CS} , to avoid an unintended Reset operation. If CS# is driven LOW to start a new transaction, DQ3_RESET# is used as DQ3.

When the device is not in Quad or QPI mode or, when CS# is HIGH, and DQ3_RESET# transitions from V_{IL} to V_{IH} for $> t_{RP}$, following t_{CS} , the device will reset register states in the same manner as POR. The hardware reset process requires a period of t_{RH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

Additional DQ3_RESET# notes

- If both RESET# and DQ3_RESET# input options are available use only one reset option in your system. DQ3_RESET# input reset operation can be disabled by setting $CFR2N[5] = 0$ setting the DQ3_RESET to only operate as DQ3. The RESET# input can be disabled by not connecting or tying the RESET# input to V_{IH} . RESET# and DQ3_RESET# must be HIGH for t_{RS} following t_{PU} , before going LOW again to initiate a hardware reset.
- When DQ3_RESET# is driven LOW for at least a minimum period of time (t_{RP}), following t_{CS} , the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write transactions for the duration of t_{RH} . The device resets the interface to standby state.
- If Quad or QPI mode and the DQ3_RESET# feature are enabled, the host system should not drive DQ3 LOW during t_{CS} , to avoid driver contention on DQ3. Immediately following transactions that transfer data to the host in Quad or QPI mode, for example: Quad I/O Read, the memory drives DQ3_RESET# HIGH during t_{CS} , to avoid an unintended Reset operation. Immediately following transactions that transfer data to the memory in Quad mode, for example: Page Program, the host system should drive DQ3_RESET# HIGH during t_{CS} , to avoid an unintended Reset operation. DQ3_RESET# LOW is ignored during t_{CS} if Quad mode is enabled.

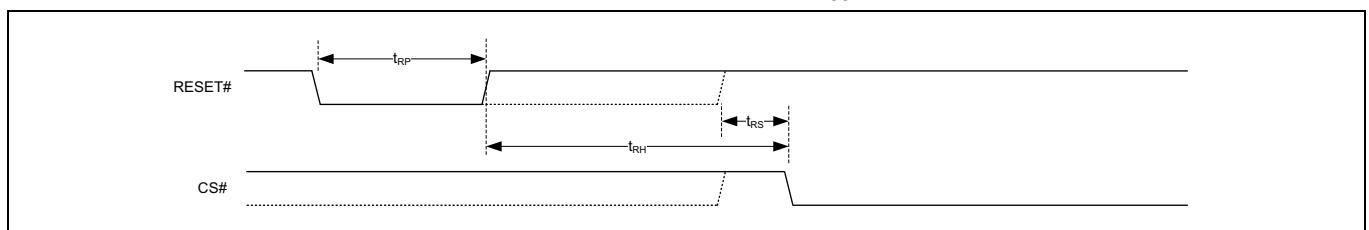


Figure 56 Hardware reset using RESET# input (Reset pulse = t_{RP} (min))

Features

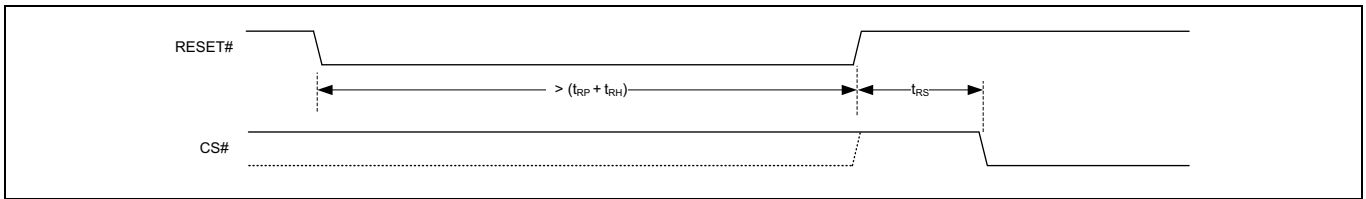


Figure 57 Hardware reset using RESET# input (Reset pulse $> (t_{RP} + t_{RH})$)

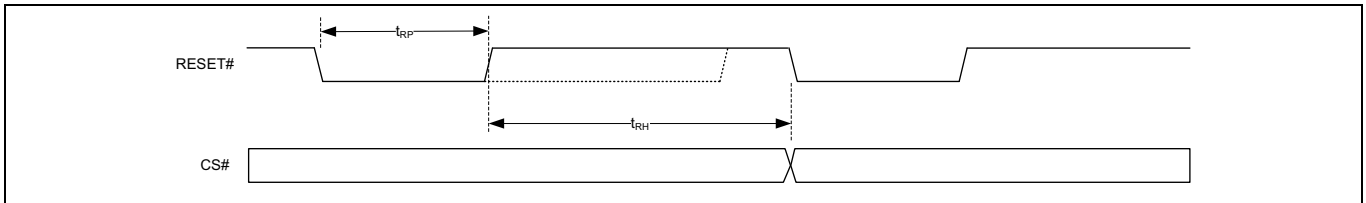


Figure 58 Hardware reset using RESET# input (Back to back hardware reset)

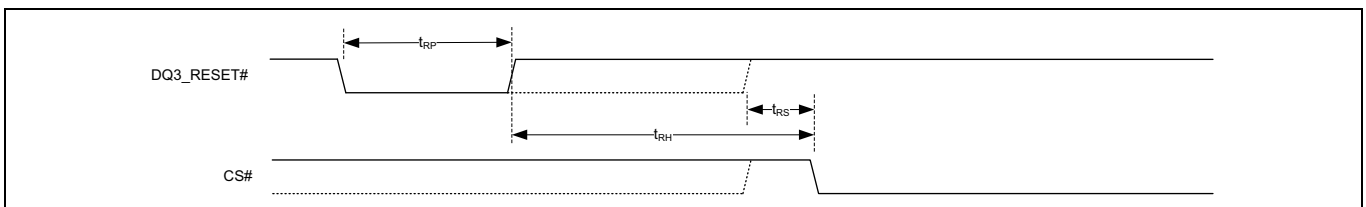


Figure 59 Hardware reset when quad or QPI Mode is disabled and DQ3_RESET# is enabled

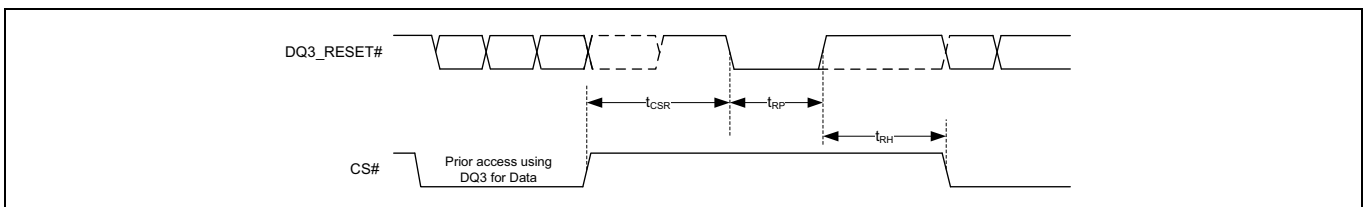


Figure 60 Hardware reset when quad or QPI Mode and DQ3_RESET# are enabled

4.12.2 Power-on reset (POR)

The device executes a POR process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see [Figure 61](#) and [Figure 62](#)). The device must not be selected during power-up (t_{PU}). Therefore, CS# must rise with V_{CC} . No transactions may be sent to the device until the end of t_{PU} . See [Table 84](#) for timing specifications.

RESET# is ignored during POR. If RESET# is LOW during POR and remains LOW through and beyond the end of t_{PU} , CS# must remain HIGH until t_{RS} after RESET# returns HIGH.

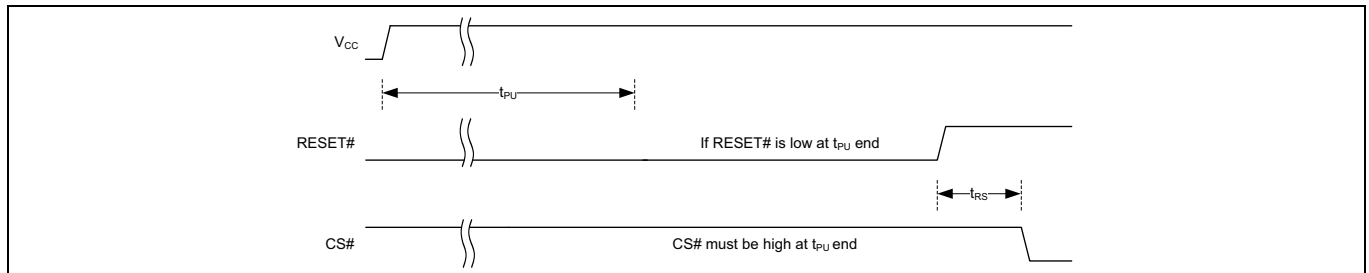


Figure 61 Reset LOW at the end of POR

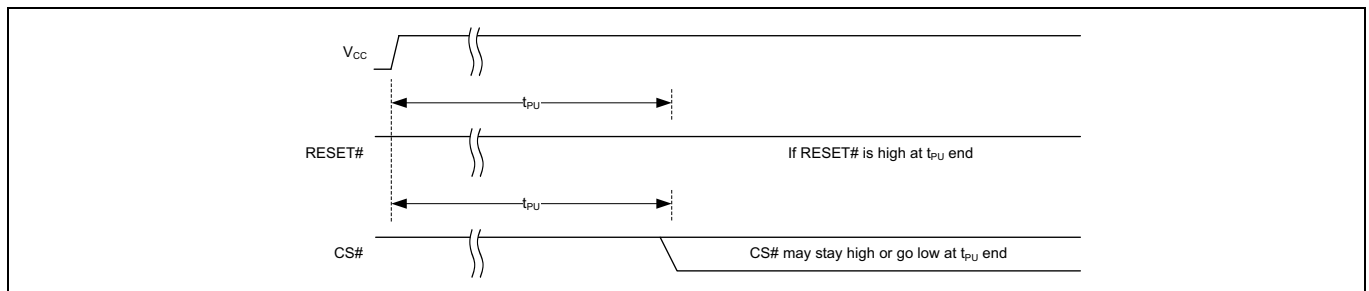


Figure 62 Reset HIGH at the end of POR

4.12.3 CS# signaling reset

The CS# Signaling Reset requires CS# and DQ0 signals. This reset method defines a signaling protocol, using existing signals, to initiate an SPI flash hardware reset, independent of the device operating mode or number of package pins.

The Signaling Protocol is shown in [Figure 63](#). See [Table 84](#) for timing specifications. The CS# signaling reset steps are as follows:

- CS# is driven active LOW.
- CK remains stable in either HIGH or LOW state.
- CS# and DQ0 are both driven LOW.
- CS# is driven HIGH (inactive).
- Repeat the above four steps, each time alternating the state of DQ0 for a total of four times.
- Reset occurs after the fourth CS# cycle completes and it goes HIGH (inactive).

After the fourth CS# pulse, the slave triggers its internal reset, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write transactions for the duration of t_{RESET} . Then the device will be in standby state.

Features

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. Hence, CS# signaling reset is useful for packages that don't support a RESET# pin to provide behavior identical to Hardware Reset.

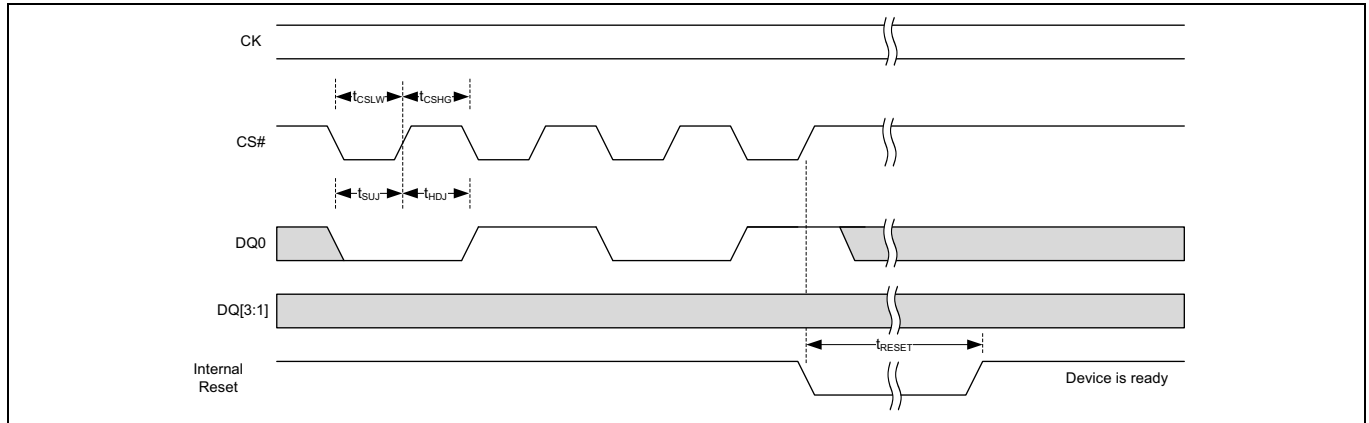


Figure 63 CS# signaling reset protocol

4.12.4 Software reset

Software controlled Reset transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values except the protection registers. It also terminates the embedded operations. A reset transaction (SFRST_0_0) is executed when CS# is brought HIGH at the end of the transaction and requires t_{SR} time to execute. See [Table 84](#) for timing specifications.

The Reset Enable (SRSTE_0_0) transaction is required immediately before a Reset transaction (SFRST_0_0) such that a software reset is a sequence of the two transactions. Any transaction other than SFRST_0_0 following the SRSTE_0_0 transaction will clear the reset enable condition and prevent a later SFRST_0_0 transaction from being recognized.

The Reset (SFRST_0_0) transaction immediately following a SRSTE_0_0 transaction, initiates the software reset process. During software reset, only RDSR1_0_0 and RDARG_C_0 of Status Register 1 are supported operations as long as the volatile and nonvolatile configuration states of the device are the same. If the configuration state is changing during software reset, reading Status Register 1 should only be done after the software reset time has elapsed.

The software reset is independent of the state of RESET#. If RESET# is HIGH or Unconnected, and the software reset transactions are issued, the device will perform software reset.

The Legacy Software Reset (SFRSL_0_0) is a single transaction that initiates the software reset process. This command is disabled by default but can be enabled by programming CFR3V[0] = 1, for software compatibility with CYPRESS™ legacy devices.

4.12.4.1 Software reset related registers and transactions

Table 37 Erase related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|-------------------|--|---|
| N/A | Software Reset Enable (SRSTE_0_0) | Software Reset Enable (SRSTE_0_0) |
| | Software Reset (SFRST_0_0) | Software Reset (SFRST_0_0) |
| | Legacy Software Reset (SFRSL_0_0) | Legacy Software Reset (SFRSL_0_0) |

Features

4.12.5 Reset behavior

Table 38 Reset behavior

| Transaction / Register name | POR | Hardware reset and CS# signaling reset | Software reset |
|--|---|---|---|
| Summary | <ul style="list-style-type: none"> • Device Reset • Status Bits Reset • All Volatile Registers Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations | <ul style="list-style-type: none"> • Device Reset • Status Bits Reset • All Volatile Registers Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations | <ul style="list-style-type: none"> • Device Reset • Status Bits Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations |
| Interface Requirements | <ul style="list-style-type: none"> • All Inputs - Ignored • All Outputs - Tristated | <ul style="list-style-type: none"> • All Inputs - Ignored • All Outputs - Tristated | Transactions (SRSTE_0_0, SFRST_0_0) |
| Status Registers | Load from Nonvolatile Registers | Load from Nonvolatile Registers | Load from Nonvolatile Registers |
| Configuration Registers | Load from Nonvolatile Registers | Load from Nonvolatile Registers | Load from Nonvolatile Registers |
| Protection Registers | PPB Lock Register - Load based on ASPO[2:1] | PPB Lock Register - Load based on ASPO[2:1] | PPB Lock Register - No Change |
| | DYB Access Register - Load based on ASPO[4] | DYB Access Register - Load based on ASPO[4] | DYB Access Register - No Change |
| | Password Register - Load based on ASPO[2] and ASPO[0] | Password Register - Load based on ASPO[2] and ASPO[0] | Password Register - No Change |
| ECC Status Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Data Learning Pattern Register | Load from Nonvolatile Registers | Load from Nonvolatile Registers | No Change |
| AutoBoot Register | Load from Nonvolatile Registers | Load from Nonvolatile Registers | No Change |
| Data Integrity Check Register | Load 0x00 | Load 0x00 | Load 0x00 |
| ECC Error Count Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Address Trap Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Infineon® Endurance Flex architecture Register | Load from Nonvolatile Registers | Load from Nonvolatile Registers | No Change |
| I/O Mode | Load from Nonvolatile Registers | Load from Nonvolatile Registers | No Change |
| Memory/Register Erase in Progress | Not Applicable | Abort Erase | Abort Erase |
| Memory/Register Program in Progress | Not Applicable | Abort Program | Abort Program |
| Memory/Register Read in Progress | Not Applicable | Abort Read | Not Applicable |

4.13 Power modes

4.13.1 Active power and standby power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB} . See [Table 82](#) for parameter specifications.

4.13.2 Deep power down (DPD) mode

Although the standby current during normal operation is relatively low, standby current can be further reduced with the DPD mode. The lower power consumption makes the DPD mode especially useful for battery powered applications.

4.13.2.1 Enter DPD

The device can enter DPD mode in two ways:

1. Enter DPD Mode using Transaction
2. Enter DPD Mode upon Power-up or Reset

Enter DPD Mode using the Enter Deep Power Down Mode Transaction

The DPD mode is enabled by sending the Enter Deep Power Down Mode Transaction (ENDPD_0_0) then waiting for a delay of t_{ENTDPD} . The CS# pin must be driven HIGH after the command byte has been latched. If this is not done, then the DPD transaction will not be executed. After CS# is driven HIGH, the power-down state will be entered within the time duration of t_{ENTDPD} (see [Table 84](#) for timing specifications) and power consumption drops to I_{DPD} . See [Table 82](#) for parameter specifications.

DPD can only be entered from an idle state. The DPD transaction is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register 1 volatile, Device Ready/Busy Status Flag (RDYBSY) bit being cleared to zero ($STR1V[0] = RDYBSY = 0$). It is not allowed to send any transaction to device during t_{ENTDPD} time.

Enter DPD Mode upon Power-up or Reset

If the DPDPOR configuration bit is enabled ($CFR4NV[2] = 1$), the device will be in DPD mode after the completion of Power-up, Hardware Reset or CS# Signaling Reset. During POR or Reset the CS# should follow the voltage applied on VCC to enter DPD mode as shown in [Figure 64](#). It is not allowed to send any transaction to device during t_{ENTDPD} time.

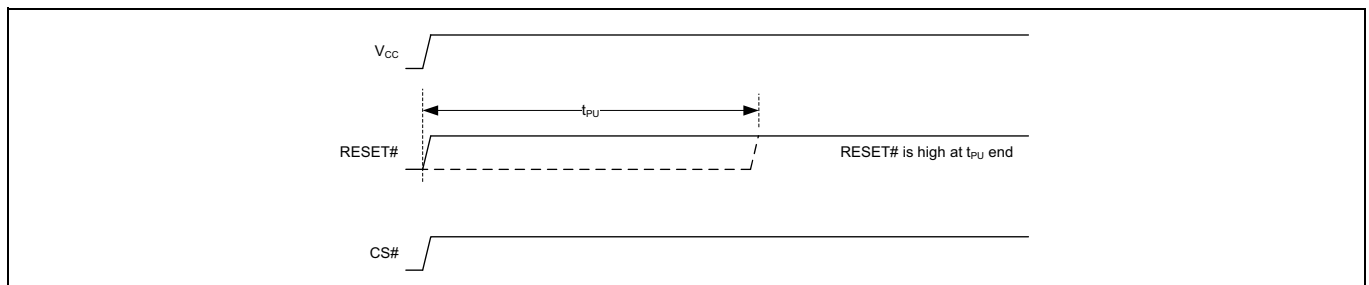


Figure 64 Enter DPD mode upon power-up or reset

4.13.2.2 Exit DPD

Device leaves DPD mode in one of the following ways:

Exit DPD Mode upon Hardware Reset

When the device is in DPD and $CFR4NV[2] = 0$, a Hardware reset will return the device to Standby mode.

Exit DPD Mode upon CS# Pulse

Device exits DPD upon receipt of CS# pulse of width t_{CSDPD} . The CS# should be driven HIGH after the pulse. HIGH to LOW transition on CS# is required to start a transaction cycle after the DPD exit. It takes t_{EXTDPD} to come out of DPD mode. The device will not respond until after t_{EXTDPD} .

Features

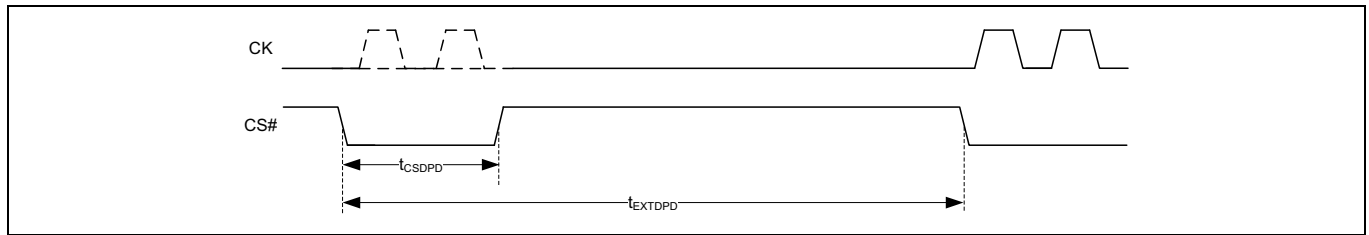


Figure 65 Exit DPD mode

The device maintains its configuration during DPD, meaning the device exits DPD in the same state as it entered. Registers such as the ECC Status, ECC Error Detection Counter, Address Trap, and Interrupt Status Registers will be cleared.

4.13.2.3 DPD related registers and transactions

Table 39 Erase related registers and transactions

| Related registers | Related SPI transactions (see Table 73 on page 91) | Related quad SPI transactions (see Table 77 on page 98) |
|--|---|--|
| Configuration Register 4 (CFR4N, CFR4V) (see Table 52 on page 81) | Enter Deep Power Down Mode (ENDPD_0_0) | Enter Deep Power Down Mode (ENDPD_0_0) |

4.14 Power up and power down

The device must not be selected at power up or power down until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power up, and then for a further delay of t_{PU}
- V_{SS} at power down

4.14.1 Power up

The device ignores all transactions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see Figure 66). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU} . No transaction should be sent to the device until the end of t_{PU} .

The device draws I_{POR} current during t_{PU} . After power up (t_{PU}), the WRPGEN bit is reset and there is the option to be in the DPD mode or Standby mode. The DPDPOR bit in Configuration Register 4 (CFR4N[2]) controls if the device will be in DPD or Standby mode after the completion of POR (see Table 52). If the DPDPOR bit is enabled (CFR4N[2] = 1) the device is in DPD mode after power up. A Hardware reset (RESET# and DQ3_RESET#) required to return the device to Standby mode after POR.

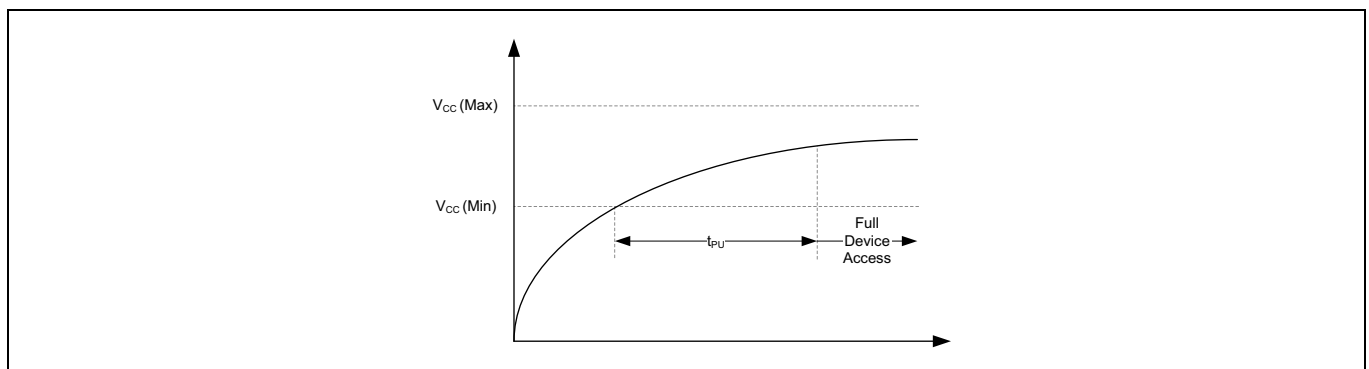


Figure 66 Power up

4.14.2 Power down

During power down or voltage drops below $V_{CC}(\text{cut-off})$, the voltage must drop below $V_{CC}(\text{Low})$ for a period of t_{PD} for the part to initialize correctly on power up (see [Figure 67](#)). If during a voltage drop the V_{CC} stays above $V_{CC}(\text{cut-off})$ the part will stay initialized and will work correctly when V_{CC} is again above $V_{CC}(\text{min})$. In the event POR did not complete correctly after power up, the assertion of the RESET# signal will restart the POR process.

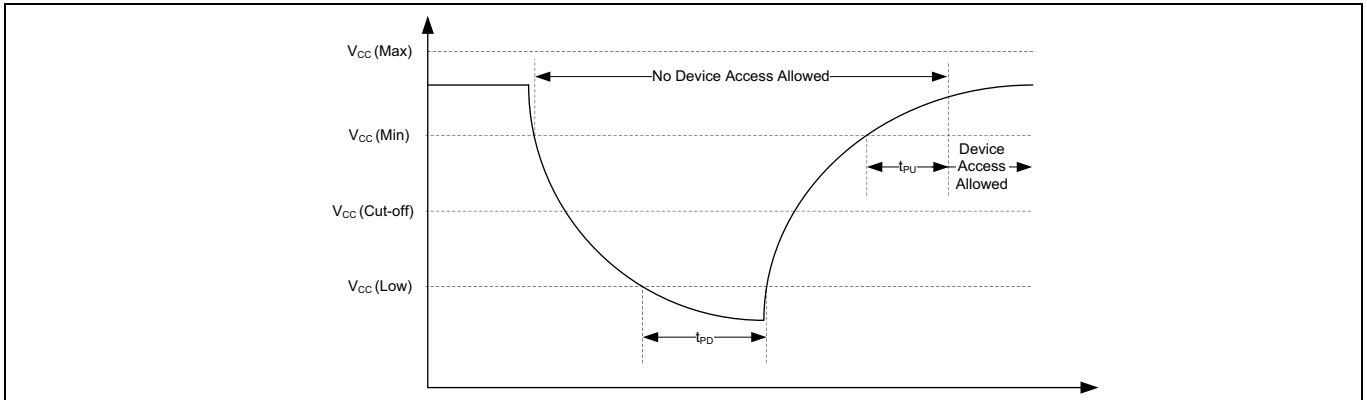


Figure 67 Power down and voltage drop

5 Registers

Registers are small groups of storage cells used to configure as well as report the status of the device operations. HL-T/HS-T family of devices use separate nonvolatile and volatile storage groups to implement the different register bit types for legacy compatibility as well as new functionality. Each register is organized as a group of volatile bits with associated nonvolatile bits (if permanence is required). During power-up, hardware reset or software reset, the data in the nonvolatile bits of the register is transferred to the volatile bits to provide the default state of the volatile bits. When writing new data to nonvolatile bits of the register, the volatile bits are also updated with the new data. However, when writing new data to the volatile register bits the nonvolatile bits retain the old data. The register structure is shown in [Figure 68](#).

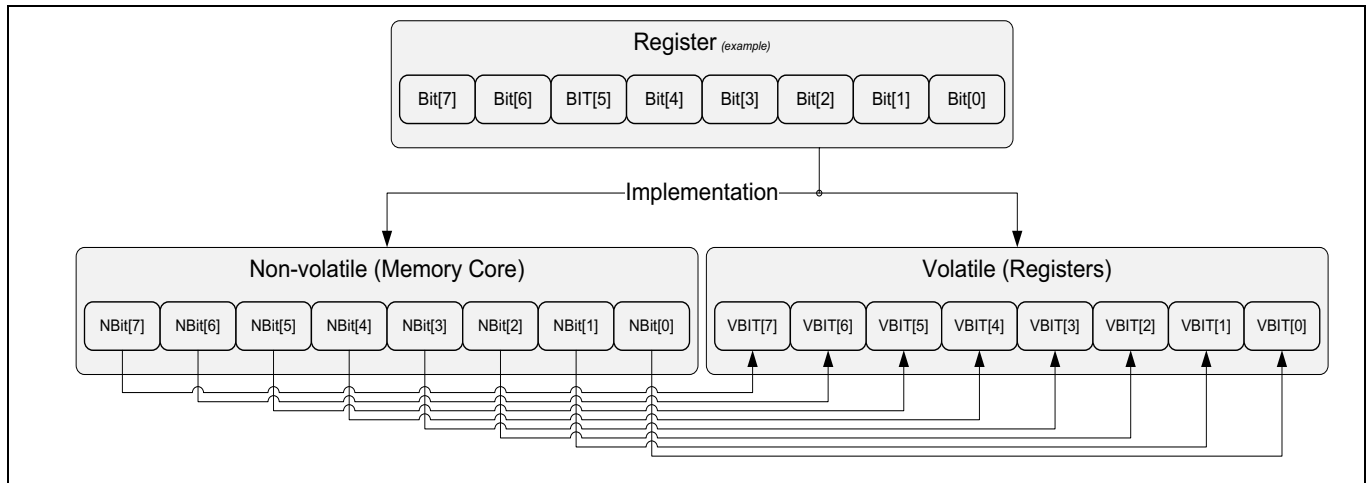


Figure 68 Register structure

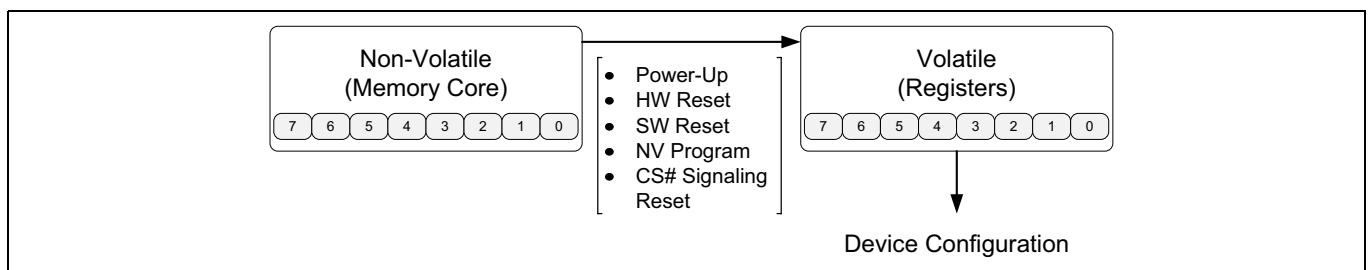


Figure 69 Data movement within register components

Registers

5.1 Register naming convention

Table 40 Register bit description convention

| Bit Number | Name | Function | Read/Write | Factory default (binary) | Description |
|---|------|----------|---|-----------------------------|--|
| REGNAME#T[x] T = N, V, O Descending Order | - | - | Possible Options: N/A - Not Applicable R - Readable Only R/W - Readable and Writable R/1 - Readable and One Time Programmable | Possible Options: 0 1 | Format: Description of the Configuration bit 0 = Option '0' selection of the Bit 1 = Option '1' selection of the Bit Dependency: Is this Bit part of a function which requires multiple bits for implementation? |

5.2 Status register 1 (STR1x)

Status Register 1 contains both status and control bits. The functionality of supported Status Register 1 type is described in [Table 41](#).

Table 41 Status register 1^[22]

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|----------------------|--------|---|---|--------------------------|--|
| STR1N[7] STR1V[7] | STCFWR | Status Register 1 and Configuration Register 1,2,3,4 Protection Selection against write (erase/program) | N->R/W V->R/W | 0 | Description: The STCFWR bit selects enabling and disabling writes (erase/program) to Status Register 1 and configuration registers 1, 2, 3, 4 based on WP# (Write Protect Pin) in Single SPI mode. When STCFWR bit is enabled with WP# LOW, any transaction that can change status or configuration registers is ignored, effectively locking the state of the device. If WP#/DQ[2] is HIGH (irrespective of STCFWR), Status and Configuration Registers can be changed. Selection Options: 1 = WP# based protection is enabled 0 = WP# based protection is disabled Dependency: N/A |
| STR1V[6] | PRGERR | Programming Error Status Flag | V->R | 0 | Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a '1', it indicates that there was an error in the last programming operation. PRGERR bit is also set when a program operation is attempted within a protected memory region. When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/software reset (see Table 42). Note The device will only go to standby mode once the PRGERR flag is cleared. Selection Options: 0 = Last programming operation was successful 1 = Last programming operation was unsuccessful Dependency: N/A |
| STR1V[5] | ERSERR | Erasing Error Status Flag | V->R | 0 | Description: The ERSERR bit indicates erase operation success or failure. When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when an erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/software reset (see Table 43). Note The device will only go to standby mode once the ERSERR flag is cleared. Selection Options: 0 = Last erase operation was successful 1 = Last erase operation was unsuccessful Dependency: N/A |

Note

22. STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

Registers

Table 41 Status register 1^[22] (continued)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|--------------------------|-------------|---|--|--------------------------|---|
| STR1N[4:2] STR1V[4:2] | LBPROT[2:0] | Legacy Block Protection based Memory Array size selection | If PLPROT = 0 N -> R/W V -> R/W If PLPROT = 1 N -> R V -> R | 000 | Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 1/64, 1/4, 1/2, etc. or bottom 1/64, 1/4, 1/2, etc., or up to the entire array is protected. Note If PLPROT bit - Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture (CFR1x[4]) is set to a '1', the LBPROT[2:0] bits cannot be erased or programmed. Selection Options: 000 = Protection is disabled 001 = 1/64th of the (top/bottom) array protection is enabled 010 = 1/32nd of the (top/bottom) array protection is enabled 111 = All sectors are protected Dependency: TBPROT (CFR1x[5]) |
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | V -> R | 0 | Description: The WRPGEN bit must be set to '1' to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable and Write Enable Volatile transactions set the WRPGEN bit to '1' to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a '0' to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to '0' at the end of any successful program, erase or register write operation. After a power down / power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to '0'. Selection Options: 0 = Program, erase or register write is disabled 1 = Program, erase or register write is enabled Dependency: N/A |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | V -> R | 0 | Description: The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions. Note The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags transaction must be executed to return the device to standby mode. Selection Options: 0 = Device is in standby mode ready to receive new operation transactions 1 = Device is busy and unable to receive new operation transactions Dependency: N/A |

Note

22. STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

Table 42 PRGERR summary

| Error flag | Symbol | Conditions |
|---------------|--------|--|
| Program Error | PRGERR | Bits cannot be programmed '1' to '0' |
| | | Trying to program in a protected region |
| | | If ASP0[2] or ASP0[1] is 0, any nonvolatile register write attempting to change the value of CFR1N[6:2]/CFR1V[6:2] |
| | | After the Password Protection Mode is selected and ASP Password Register update transaction executed |
| | | SafeBoot Failure |
| | | Configuration Failure |

Registers

Table 43 ERSERR summary

| Error flag | Symbol | Conditions |
|-------------|--------|---|
| Erase Error | ERSERR | Sector Device Erase - All bits cannot be erased to '1's |
| | | Trying to erase a protected region |
| | | Register Erase - All bits cannot be erased to '1's during Erase portion of Register Write |
| | | SafeBoot Failure |

5.3 Status register 2 (STR2x)

Status Register 2 provides device status on operations. The functionality of supported Status Register 2 type is described in [Table 44](#).

Table 44 Status register 2^[23]

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|---|---|--------------------------|---|
| STR2V[7:5] | RESRVD | Reserved for future use | V -> R | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| STR2V[4] | DICRCS | Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag | V -> R | 0 | Description: The DICRCS bit is used to determine when the device is in Memory Array Data Integrity Cyclic Redundancy Check suspend mode. Selection Options: 0 = Memory Array Data Integrity Cyclic Redundancy Check is not in suspend mode 1 = Memory Array Data Integrity Cyclic Redundancy Check is in suspend mode Dependency: N/A |
| STR2V[3] | DICRCA | Memory Array Data Integrity Cyclic Redundancy Check Abort Status Flag | V -> R | 0 | Description: The DICRCA bit indicates that the Memory Array Data Integrity Cyclic Redundancy Check calculation operation was aborted. The abort condition is based on ending address (ENDADD) and starting address (STRADD) relationship. If ENDADD < STRADD + 3, then DICRCA will be set and the device will return to the Standby state. DICRCA flag gets cleared at the next Data Integrity Cyclic Redundancy Check calculation operation when ENDADD ≥ STRADD + 3. Selection Options: 0 = Memory Array Data Integrity Cyclic Redundancy Check calculation is not aborted 1 = Memory Array Data Integrity Cyclic Redundancy Check calculation is aborted Dependency: N/A |
| STR2V[2] | SESTAT | Sector Erase Success/Failure Status Flag | V -> R | 0 | Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction must be executed prior to reading SESTAT bit which specifies the sector address. Selection Options: 1 = Addressed sector was erased successfully 0 = Addressed sector was not erased successfully Dependency: N/A |
| STR2V[1] | ERASES | Erase operation Suspend Status Flag | V -> R | 0 | Description: The ERASES bit is used to indicate if the Erase operation is suspended. Selection Options: 0 = Erase operation is not in suspend mode 1 = Erase operation is in suspend mode Dependency: N/A |
| STR2V[0] | PROGMS | Program operation Suspend Status Flag | V -> R | 0 | Description: The PROGMS bit is used to indicate if the Program operation is suspended. Selection Options: 0 = Program operation is not in suspend mode 1 = Program operation is in suspend mode Dependency: N/A |

Note

23. STR2x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid. STR2x bits are valid only when STR1V[0] / RDYBSY = 0.

5.4 Configuration register 1 (CFR1x)

Configuration Register 1 controls interface and data protection functions.

Table 45 Configuration register 1

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|----------------------|--------|--|--|-----------------------------|---|
| CFR1N[7] CFR1V[7] | RESRVD | Reserved for future use | N -> R/W V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR1N[6] CFR1V[6] | SP4KBS | Split 4KB Sectors selection between top and bottom address space | If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R | 0 | Description: The SP4KBS bit selects whether the 4KB sectors are grouped together or evenly split between High and LOW address ranges (see Table 46). Selection Options: 0 = 4KB Sectors are grouped together 1 = 4KB Sectors are split between High and Low Addresses Dependency: TB4KBS(CFR1N[2]) |
| CFR1N[5] CFR1V[5] | TBPROT | Top or Bottom Protection selection for Legacy Protection Mode | If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R | 0 | Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range. The bit also selects a memory address range (lowest or highest) to remain readable is available for reading during Read Password Protection mode even before a successful Password entry is completed (see Table 47). Selection Options: 0 = Legacy Protection is applicable in the top half of the address range 1 = Legacy Protection is applicable in the bottom half of the address range Dependency: LBPROT[2:0] (STR1x[3:1]) |
| CFR1N[4] CFR1V[4] | PLPROT | Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture | N -> R/1 V -> R | 0 | Description: The PLPROT bit permanently protects the Legacy Block Protection and 4KB Sector location. It thereby permanently protects the memory array protection scheme and sector architecture (see Table 47). Note PLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase. It is recommended to configure these bits before configuring the PLPROT bit. Selection Options: 0 = Legacy Block Protection and 4KB Sector Location are not protected 1 = Legacy Block Protection and 4KB Sector Location are protected Dependency: N/A |
| CFR1N[3] CFR1V[3] | RESRVD | Reserved for future use | N -> R/W V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR1N[2] CFR1V[2] | TB4KBS | Top or Bottom Address Range selection for 4KB Sector Block | If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R | 0 | Description: The TB4KBS bit defines the logical address location of the 4KB sector block. The 4KB sector block replaces the fitting portion of the highest or lowest address sector (see Table 46). Selection Options: 0 = 4KB Sector Block is in the bottom of the memory address space 1 = 4KB Sector Block is in the top of the memory address space Dependency: SP4KBS (CFR1x[6]) |

Registers

Table 45 Configuration register 1 (continued)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|----------------------|--------|--|---|--------------------------|---|
| CFR1N[1] CFR1V[1] | QUADIT | Quad SPI Interface Selection - I/O width set to 4 bits (1-1-4, 1-4-4) | N -> R/W V -> R/W | 0 | Description: The QUADIT bit selects the I/O width of the device. When configured to 4-bits (QUAD), WP# becomes DQ2 and DQ3_RESET# becomes DQ3. The QUADIT transactions require Opcode sent on a single I/O, Address either on a single or all four I/Os and Data always sent on all four I/Os. Selection Options: 0 = Data Width set to 1 or 2 bits wide (1x - Single, 2x - Dual) 1 = Data Width set to 4 wide (4x - Quad) Dependency: N/A |
| CFR1N[0] CFR1V[0] | TLPROT | Temporary Locking selection of Legacy Block Protection and Sector Architecture | N -> R V -> R/W | 0 | Description: The TLPROT bit temporarily protects the Legacy Block Protection and 4KB Sector location. Upon power-up or a hardware reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme and sector architecture from any changes. Note TLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase. Selection Options: 0 = Legacy Block Protection and 4KB Sector Location are not protected 1 = Legacy Block Protection and 4KB Sector Location are temporarily protected Dependency: N/A |

Table 46 4KB parameter sector location selection

| SP4KBS | TB4KBS | 4KB location |
|--------|--------|---|
| 0 | 0 | 4KB physical sectors at bottom (Low address) |
| 0 | 1 | 4KB physical sectors at top, (High address) |
| 1 | X | 4KB Parameter sectors are split between top (High Address) and bottom (Low Address) |

Table 47 PLPROT and TLPROT protection

| PLPROT | TLPROT | Array protection and 4K sector |
|--------|--------|--|
| 0 | 0 | Unprotected (Unlocked) |
| 1 | x | TBPROT, LBPROTx, SP4KBS, TB4KBS - Permanently Protected (Locked) |
| 0 | 1 | TBPROT, LBPROTx, SP4KBS, TB4KBS, Protected (Locked) till next Power-down |

5.5 Configuration register 2 (CFR2x)

Configuration Register 2 controls interface, memory read latency and address byte length selection.

Table 48 Configuration register 2

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|--------------------------|-------------|---|---|--------------------------|--|
| CFR2N[7] CFR2V[7] | ADRBYT | Address Byte Length selection between 3 or 4 bytes for Instructions | N -> R/W V -> R/W | 0 | Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes. Selection Options: 0 = Instructions will use 3 Bytes for address 1 = Instructions will use 4 Bytes for address Dependency: N/A |
| CFR2N[6] CFR2V[6] | QPI-IT | QPI Interface & Protocol Selection - I/O width set to 4 bits (4-4-4) | N -> R/W V -> R/W | 0 | Description: The QPI-IT bit selects the I/O width of the device to be 4-bits wide. When configured to 4-bits (QPI-IT, QUADIT), WP# becomes DQ2 and DQ3_RESET# becomes DQ3. The QPI-IT transactions require Opcode, Address and Data always sent on all four I/Os. Selection Options: 0 = Data Width set to 1 or 2 bits wide (1x - Single, 2x - Dual) - Legacy Protocol 1 = Data Width set to 4 wide (4x - Quad) - QPI Protocol Dependency: N/A |
| CFR2N[5] CFR2V[5] | DQ3RST | DQ3 and RESET Selection for DQ3 - Multiplexed operation on I/O #3 | N -> R/W V -> R/W | 0 | Description: The DQ3RST bit controls the RESET# behavior on DQ3 signal. When enabled, a LOW on DQ3 will perform a hardware reset while CS# is HIGH. This multiplexed functionality on DQ3 is only available when QUADIT or QPI-IT interface modes are enabled. Disabling QUADIT or QPI-IT modes makes DQ3 a dedicated RESET# pin. Selection Options: 0 = DQ3 has no multiplexed RESET# function 1 = DQ3 performs a hardware reset when LOW provided CS# is HIGH Dependency: N/A |
| CFR2N[4] CFR2V[4] | RESRVD | Reserved for future use | N -> R/W V -> R/W | 0 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR2N[3:0] CFR2V[3:0] | MEMLAT[3:0] | Memory Array Read Latency selection - Dummy cycles required for initial data access | N -> R/W V -> R/W | 1000 | Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and nonvolatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see Table 49). Selection Options: 0000 = 0 Latency Cycle Selection based on transaction opcodes 1111 = 15 Latency Cycles Selection based on transaction opcodes Dependency: N/A |

Registers

Table 49 Latency code (cycles) versus frequency^[24, 25, 26, 28]

| Latency Code / cycles | Read transaction maximum frequency (MHz) | | | | | |
|-----------------------|---|-------------------|--|---|--|--|
| | RDAY2_C_0 (1-1-1) RDSSR_C_0 (1-1-1) RDECC_C_0 (1-1-1) RDECC_4_0 (1-1-1) RDARG_C_0 (1-1-1) ^[27] RDAY4_C_0 (1-1-4) RDAY4_4_0 (1-1-4) RDPPB_C_0 (1-1-1) RDPPB_4_0 (1-1-1) | RDAY2_4_0 (1-1-1) | RDAY3_C_0 (1-2-2) RDAY3_4_0 (1-2-2) | RDAY2_4_0 (4-4-4) RDAY5_4_0 (4-4-4) RDAY5_C_0 (4-4-4) RDAY5_C_0 (1-4-4) RDAY5_4_0 (1-4-4) RDPPB_C_0 (4-4-4) RDPPB_4_0 (4-4-4) | RDSSR_C_0 (4-4-4) ^[29] RDARG_C_0 (4-4-4) ^[27] RDECC_C_0 (4-4-4) RDECC_4_0 (4-4-4) | RDAY7_C_0 (1-4-4) RDAY7_4_0 (1-4-4) RDAY7_C_0 (4-4-4) RDAY7_4_0 (4-4-4) |
| | Mode Cycle = 0 | Mode Cycle = 8 | Mode Cycle = 4 | Mode Cycle = 2 | Mode Cycle = 0 | Mode Cycle = 1 |
| 0 | 50 | 156 | 81 | 43 | 18 | N/A |
| 1 | 68 | 166 | 93 | 56 | 31 | N/A |
| 2 | 81 | 166 | 106 | 68 | 43 | 43 |
| 3 | 93 | 166 | 118 | 81 | 56 | 56 |
| 4 | 106 | 166 | 131 | 93 | 68 | 68 |
| 5 | 118 | 166 | 143 | 106 | 81 | 81 |
| 6 | 131 | 166 | 156 | 118 | 93 | 93 |
| 7 | 143 | 166 | 166 | 131 | 106 | 102 |
| 8 (Default) | 156 | 166 | 166 | 143 | 118 | 102 |
| 9 | 166 | 166 | 166 | 156 | 131 | 102 |
| 10 | 166 | 166 | 166 | 166 | 143 | 102 |
| 11 | 166 | 166 | 166 | 166 | 156 | 102 |
| 12 | 166 | 166 | 166 | 166 | 166 | 102 |
| 13 | 166 | 166 | 166 | 166 | 166 | 102 |
| 14 | 166 | 166 | 166 | 166 | 166 | 102 |
| 15 | 166 | 166 | 166 | 166 | 166 | 102 |

Notes

- 24. When using the ECC error reporting mechanisms, the read output data must be at least 2 bytes for correct ECC reporting.
- 25. CK frequency > 166MHz SDR, or > 102MHz DDR is not supported by this family of devices.
- 26. The Fast Read 4-byte address, QPI, Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI, protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. For example, the legacy Quad I/O transaction has two Continuous Read mode cycles following the address. Therefore, the legacy Quad I/O transaction without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency, the frequency of the Quad I/O transaction can be increased to allow operation up to the maximum supported 166MHz frequency.
- 27. Read Any Register transaction uses these latency cycles for reading nonvolatile registers.
- 28. Read SFDP transaction always have a dummy cycle of 8 and the maximum frequencies for different interfaces related to eight dummy cycles. Read Unique ID has 32 cycles of latency.
- 29. Secure Silicon Read (4-4-4) latency cycle > 0.

5.6 Configuration register 3 (CFR3x)

Configuration register 3 controls transaction behavior.

Table 50 Configuration register 3

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|--------------------------|-------------|--|---|-----------------------------|---|
| CFR3N[7:6] CFR3V[7:6] | VRGLAT[1:0] | Volatile Register Read Latency selection - Dummy cycles required for initial data access | N -> R/W V -> R/W | 00 | Description: The VRGLAT[1:0] bits control the read latency (dummy cycles) delay in all variable latency register read transactions. VRGLAT[1:0] selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see Table 51). Selection Options: 00, 01, 10, 11 Latency Cycles Selection based on transaction opcodes Dependency: N/A |
| CFR3N[5] CFR3V[5] | BLKCHK | Blank Check selection during Erase operation for better endurance | N -> R/W V -> R/W | 0 | Description: When this feature is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to be erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally. Selection Options: 0 = Blank Check is disabled before executing an erase operation 1 = Blank Check evaluation is enabled before executing an erase operation Dependency: N/A |
| CFR3N[4] CFR3V[4] | PGMBUF | Program Buffer Size selection | N -> R/W V -> R/W | 0 | Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time. Note If programming data exceeds the program buffer size, data gets wrapped. Selection Options: 0 = 256 Byte Write Buffer Size 1 = 512 Byte Write Buffer Size Dependency: N/A |
| CFR3N[3] CFR3V[3] | UNHYSA | Uniform or Hybrid Sector Architecture selection | N -> R/W V -> R | 0 | Description: The UNHYSA bit selects between uniform (all 256KB sectors) or hybrid (4KB sectors and 256KB sectors) sector architecture. If hybrid sector architecture is selected, 4KB sector block is made part of the main flash array address map. The 4KB sector block can overlay at either the highest or the lowest address range of the device. If uniform sector architecture is selected, 4KB sector block is removed from the address map and all sectors are of uniform size. Note Hybrid sector architecture also enables 4KB Sector Erase transaction (20h). Otherwise, 4KB Sector Erase transaction, if issued, is ignored by the device. Selection Options: 0 = Hybrid Sector Architecture (combination of 4KB sectors and 256KB sectors) 1 = Uniform Sector Architecture (all 256KB sectors) Dependency: SP4KBS(CFR1N[6]), TB4KBS(CFR1N[2]) |
| CFR3N[2] CFR3V[2] | CLSRSM | Clear Status or Resume transaction 30h selection | N -> R/W V -> R/W | 0 | Description: The CLSRSM bit selects how the 30h transaction is used in the device. CLSRSM controls whether 30h transaction is used as clear status transaction or as an alternate Program / Erase / Data Integrity Check resume transaction. Selection Options: 0 = Clear Status Register transaction 1 = Program / Erase / Data Integrity Check Resume transaction Dependency: N/A |
| CFR3N[1] CFR3V[1] | RESRVD | Reserved for future use | N -> R/W V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR3N[0] CFR3V[0] | LSFRST | Legacy Software Reset transaction F0h selection | N -> R/W V -> R/W | 0 | Description: The LSFRST bit selects the software reset transaction. It allows the legacy F0h single transaction for software reset. Selection Options: 0 = Legacy Software Reset is disabled 1 = Legacy Software Reset is enabled Dependency: N/A |

Registers

Table 51 Register latency code (cycles) versus frequency^[30, 32]

| Latency code | Frequency | Fast read registers (No address) | Regular read registers (No address) | Regular read registers (With address) |
|--------------|-----------|--|--|---|
| | | RDSR1_0_0 (1-1-1) RDSR1_0_0 (4-4-4) RDSR2_0_0 (1-1-1) RDCR1_0_0 (1-1-1) RDDLP_0_0 (1-1-1) RDIDN_0_0 (1-1-1) RDIDN_0_0 (4-4-4) RDPLB_0_0 (1-1-1) RDQID_0_0 (1-4-4, 4-4-4) | RDSR2_0_0 (4-4-4) RDCR1_0_0 (4-4-4) RDDLP_0_0 (4-4-4) RDPLB_0_0 (4-4-4) | RDDYB_C_0 (1-1-1) (4-4-4) RDDYB_4_0 (1-1-1) (4-4-4) RDARG_C_0 ^[31] (1-1-1) (4-4-4) |
| 00 (Default) | 50MHz | 0 | 0 | 0 |
| 01 | 133MHz | 0 | 1 | 1 |
| 10 | 133MHz | 1 | 1 | 1 |
| 11 | 166MHz | 2 | 2 | 2 |

Notes

- 30. CK frequency > 166MHz SDR, or 102MHz DDR is not supported by this family of devices.
- 31. Read Any Register transaction uses these latency cycles for reading volatile registers.
- 32. Read SFDP transaction always have a dummy cycle of 8 and the maximum frequencies for different interfaces related to eight dummy cycles. Read Unique ID has 32 cycles of latency.

5.7 Configuration register 4 (CFR4x)

Configuration Register 4 controls the main flash array read transactions burst wrap behavior and output driver impedance.

Table 52 Configuration register 4

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|--------------------------|-------------|---|---|--------------------------|--|
| CFR4N[7:5] CFR4V[7:5] | IOIMPD[2:0] | I/O Driver Output Impedance selection | N -> R/W V -> R/W | 000 | Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements. Selection Options: 000 = 45Ω (Factory Default) 001 = 120Ω 010 = 90Ω 011 = 60Ω 100 = 45Ω 101 = 30Ω 110 = 20Ω 111 = 15Ω Dependency: N/A |
| CFR4N[4] CFR4V[4] | RBSTWP | Read Burst Wrap Enable selection | N -> R/W V -> R/W | 0 | Description: The RBSTWP bit selects the read burst wrap feature. It allows the device to enter and exit burst wrapped read mode during normal operation. The wrap length is selected by RBSTWL[1:0] bits. Selection Options: 0 = Read Wrapped Burst disabled 1 = Read Wrapped Burst enabled Dependency: RBSTWL[1:0] (CFR4x[1:0]) |
| CFR4N[3] CFR4V[3] | ECC12S | Error Correction Code (ECC) 1-bit or 1-bit/2-bit error correction selection | N -> R/W V -> R/W | 1 | Description: The ECC12S bit selects between 1-bit ECC error detection/correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. This configuration option affects Address Trap Register and ECC Counter Register functionalities as well. The host needs to erase and reprogram the data in the SEMPER™ Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa). Selection Options: 0 = 1-bit ECC Error Detection/Correction 1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection Dependency: N/A |

Registers

Table 52 Configuration register 4 (continued)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|--------------------------|-------------|--|---|-----------------------------|--|
| CFR4N[2] CFR4V[2] | DPDPOR | Deep Power Down power saving mode entry selection upon POR | N -> R/W V -> R | 0 | Description: The DPDPOR bit selects if the device will be in either Deep Power Down (DPD) mode or the Standby mode after the completion of POR. If enabled, DPDPOR configures the device to start in DPD mode to reduce current consumption until the device is needed. If the device is in DPD, a pulse on CS# or a Hardware reset will return the device to Standby mode. Selection Options: 0 = Standby mode is entered upon the completion of POR 1 = Deep Power Down Power mode is entered upon the completion of POR Dependency: N/A |
| CFR4N[1:0] CFR4V[1:0] | RBSTWL[1:0] | Read Burst Wrap Length selection | N -> R/W V -> R/W | 00 | Description: The RBSTWL[1:0] bits select the read burst wrap length and alignment during normal operation. It selects the fixed length/aligned group of 8-, 16-, 32-, or 64-bytes (see Table 53). Selection Options: 00 = 8 Bytes Wrap length 01 = 16 Bytes Wrap length 10 = 32 Bytes Wrap length 11 = 64 Bytes Wrap length Dependency: RBSTWP (CFR4x[4]) |

Table 53 Output data wrap sequence

| Wrap boundary (Bytes) | Start address (Hex) | Address sequence (Hex) |
|--------------------------|------------------------|---|
| Sequential | XXXXXX03 | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18. |
| 8 | XXXXXX00 | 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02. |
| 8 | XXXXXX07 | 07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01. |
| 16 | XXXXXX02 | 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03. |
| 16 | XXXXXX0C | 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E. |
| 32 | XXXXXX0A | 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F. |
| 32 | XXXXXX1E | 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00. |
| 64 | XXXXXX03 | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02. |
| 64 | XXXXXX2E | 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D. |

5.8 Memory array data integrity check CRC register (DCRV)

The memory array Data Integrity Check CRC Register (DCRV) stores the results of the CRC calculation on the data contained between the specified starting and ending addresses.

Table 54 Memory array data integrity check CRC register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------|--------------|--------------------------------------|---|--------------------------|---|
| DCRV[31:0] | DTCRCV[31:0] | Memory Array Data CRC Checksum Value | V -> R | 0x00000000 | Description: The DTCRCV[31:0] bits store the checksum value of the CRC process on the memory array data contained within the starting address and the ending address. Selection Options: Checksum Value Dependency: N/A |

Registers

5.9 ECC status register (ECSV)

The ECC Status Register (ECSV) contains the ECC status of any error correction action performed on the unit data whose byte was addressed during last read.

Note Unit data is defined as the number of bytes over which the ECC is calculated. HL-T/HS-T family devices have a 16 bytes (128 bits) unit data.

Table 55 ECC status register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|---|---|-----------------------------|--|
| ECSV[7:5] | RESRVD | Reserved for future use | V -> R | 000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| ECSV[4] | ECC2BT | ECC Error 2-bit Error Detection Flag | V -> R | 0 | <p>Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT.</p> <p>Note ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.</p> <p>Note ECC1BT is not valid if ECC2BT status flag is set.</p> <p>Selection Options: 0 = No 2-Bit ECC Error was detected in the data unit (16 bytes) 1 = 2-bit ECC Error was detected in the data unit (16 bytes)</p> <p>Dependency: CFR4x[3]</p> |
| ECSV[3] | ECC1BT | ECC Error 1-bit Error Detection and Correction Flag | V -> R | 0 | <p>Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT.</p> <p>Note ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.</p> <p>Selection Options: 0 = No 1-Bit ECC Error was detected in the data unit (16 bytes) 1 = 1-bit ECC Error was detected in the data unit (16 bytes)</p> <p>Dependency: N/A</p> |
| ECSV[2:0] | RESRVD | Reserved for future use | V -> R | 000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |

5.10 ECC address trap register (EATV)

The ECC Address Trap Register (EATV) stores the address of the ECC unit data where either a 1-Bit/2-Bit error or only a 1-Bit error occurred during a read operation. It stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC transaction.

Table 56 ECC address trap register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------|--------------|---|---|--------------------------|--|
| EATV[31:0] | ECCATP[31:0] | ECC 1-bit and 2-bit Error Address Trap Register | V -> R | 0x00000000 | <p>Description: The Address Trap Register (ECCATP[31:0]) stores the ECC unit data address where a 1-Bit/2-Bit error occurred during a read operation. ECCATP[31:0] stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC Status Register transaction (CLECC_0_0).</p> <p>Note ECCATP[31:0] is only updated during Read Instruction.</p> <p>Note Mask non-valid upper ECCATP address bits from ECC unit address.</p> <p>Note Clear ECC Status Register transaction (CLECC_0_0), POR or Hardware/Software reset clears the EATV[31:0] to 0x00000000.</p> <p>Selection Options: ECC Error Data Unit Address</p> <p>Dependency: N/A</p> |

Registers

5.11 ECC error detection count register (ECTV)

The ECC Error Detection Counter Register (ECTV) stores the number of either 1-Bit/2-Bit or only 1-Bit ECC errors have occurred during read operations since the last POR or hardware/software reset.

Table 57 ECC count register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------|--------------|--|---|--------------------------|---|
| ECTV[15:0] | ECCCNT[15:0] | ECC 1-bit and 2-bit Error Count Register | V -> R | 0x0000 | <p>Description: The ECCCNT[15:0] stores the number of 1-bit/2-bit ECC errors occurred during read operations since the last POR or hardware/software reset.</p> <p>Note ECCCNT[15:0] is only updated during Read Instruction.</p> <p>Note Only one ECC error is counted for each data unit. If multiple read transactions access the same unit data containing an ECC error, the ECCCNT[15:0] will increment each time the unit data is read.</p> <p>Note Once the count reaches 0xFFFF, the ECCCNT[15:0] will stop incrementing</p> <p>Note POR or Hardware/Software reset clears the ECCCNT[15:0] to 0x0000.</p> <p>Selection Options: ECC Error Count</p> <p>Dependency: N/A</p> |

5.12 Advanced sector protection register (ASPO)

The ASP Register (ASPO) configures the behavior of Advanced Sector Protection scheme.

Table 58 Advanced sector protection register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|---|---|-----------------------------|---|
| ASPO[15:6] | RESRVD | Reserved for future use | N -> R/1 | 1111111111 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| ASPO[5] | ASPRDP | Read Password Based Protection Selection | N -> R/1 | 1 | <p>Description: The ASPRDP bit selects the Read Password Mode Protection mode. Read Password Protection mode works in conjunction with Password Protection mode to protect all sectors from Read/Erase/Program. Based on TBPROT configuration bit (CFR1x[5]), either the top or bottom sector is available for reading.</p> <p>Selection Options: 0 = Read Password Protection Mode is enabled 1 = Read Password Protection Mode is disabled</p> <p>Dependency: TBPROT (CFR1x[5])</p> |
| ASPO[4] | ASPDYB | Dynamic Protection (DYB) for all sectors at power-up Selection | N -> R/1 | 1 | <p>Description: The ASPDYB bit selects whether all DYB bits (sectors) are in the protected state following power-up or hardware reset. DYB bits will individually need to be reset to change sector protections.</p> <p>Selection Options: 0 = DYB based sector protection enabled at power-up or hardware reset 1 = DYB based sector protection disabled at power-up or hardware reset</p> <p>Dependency: N/A</p> |
| ASPO[3] | ASPPPB | Permanent Protection (PPB) bits for all sectors programmability Selection | N -> R/1 | 1 | <p>Description: The ASPPPB bit selects whether all PPB bits are OTP making PPB sector protection permanent.</p> <p>Note ASPPPB disables PPB erase transaction (ERPPB_0_0).</p> <p>Selection Options: 0 = PPB bits are OTP 1 = PPB bits can be erased and programmed as desired</p> <p>Dependency: N/A</p> |

Registers

Table 58 Advanced sector protection register (continued)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|---|---|-----------------------------|--|
| ASPO[2] | ASPPWD | Password Based Protection Selection | N -> R/1 | 1 | Description: The ASPPWD bit selects the Password Protection Mode. Password Protection mode protects all PPB bits till the correct password is entered. The ASPPWD can also be used in combination with the ASPRDP to protect all registers and all memory from erase/program and to protect sectors from being read as well till the correct password is provided - except for top or bottom sector which is available for reading based on TBPROT configuration bit (CFR1x[5]). Note When ASPPWD is selected, ASPO[15:0], CFR1N[7:2] and PWDO[63:0] are protected against Write operations. Selection Options: 0 = Password Protection Mode is enabled 1 = Password Protection Mode is disabled Dependency: N/A |
| ASPO[1] | ASPPER | Persistent Protection Selection (Register Protection Selection) | N -> R/1 | 1 | Description: The ASPPER bit selects the Persistent Protection Mode. The Persistent Protection mode (ASPPER) protects the ASPO[15:0], CFR1x[6, 5, 4, 2] and CFR3x[3] registers from erase or program. Selection Options: 0 = Persistent Protection Mode is enabled 1 = Persistent Protection Mode is disabled Dependency: N/A |
| ASPO[0] | ASPPRM | Permanent Protection Selection | N -> R/1 | 1 | Description: The ASPPRM bit selects the Permanent Protection Mode. The Permanent Protection mode (ASPPRM) permanently protects the PPB bits from erase or program. ASPPRM bit should be programmed once all the PPB based sector protections are finalized. Note Permanent protection is independent of the PPBLOCK bit. Selection Options: 0 = Permanent Protection Mode is enabled 1 = Permanent Protection Mode is disabled Dependency: N/A |

5.13 ASP password register (PWDO)

The ASP Password Register (PWDO) is used to permanently define a password.

Table 59 Password register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------|--------------|-------------------|---|--------------------------|---|
| PWDO[63:0] | PASWRD[63:0] | Password Register | N -> R/1 | 0xFFFFFFFF FFFF | Description: The PASWRD[63:0] permanently stores a password used in password protected modes of operation. When the Password Protection Mode is enabled, this register will output the undefined data upon read password request. Selection Options: Password Dependency: N/A |

Registers

5.14 ASP PPB lock register (PPLV)

The PPBLCK bit in the ASP PPB Lock Register (PPLV) is used to protect the PPB bits.

Table 60 ASP PPB lock register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|------------------------------------|---|-----------------------------|--|
| PPLV[7:1] | RESVRD | Reserved for future use | V -> R | 0000000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| PPLV[0] | PPBLCK | PPB Temporary Protection Selection | V -> R/W | 1, ASPO[2:1] | Description: The PPBLCK bit is used to temporarily protect all the PPB bits. Selection Options: 1 = PPB Bits can be erased or programmed 0 = PPB bits are protected against erase or program till the next POR or hardware reset Dependency: N/A |

5.15 ASP PPB access register (PPAV)

The ASP PPB Access Register (PPAV) is used to provide the state of each sector's PPB protection bit.

Table 61 ASP PPB access register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory Default (binary) | Description |
|------------|-------------|------------------------------------|---|-----------------------------|--|
| PPAV[7:0] | PPBACS[7:0] | Sector Based PPB Protection Status | N -> R/W | 11111111 | Description: The PPBACS[7:0] bits are used to provide the state of the individual sector's PPB bit. Selection Options: FF = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 1, not protecting that sector from program or erase operations 00 = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A |

5.16 ASP dynamic block access register (DYAV)

The ASP DYB Access Register (DYAV) is used to provide the state of each sector's DYB protection bit.

Table 62 ASP DYB access register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|-------------|------------------------------------|---|-----------------------------|--|
| DYAV[7:0] | DYBACS[7:0] | Sector Based DYB Protection Status | V -> R/W | 11111111 | Description: The DYBACS[7:0] bits are used to provide the state of the individual sector's DYB bit. Selection Options: FF = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 1, not protecting that sector from program or erase operations 00 = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A |

Registers

5.17 Data learning register (DLPx)

The Data Learning Pattern Register (DLPx) contains the 8-bit Data Learning pattern.

Table 63 Data learning register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------------------|-------------|---------------------------------|---|--------------------------|--|
| DLPN[7:0] DLPV[7:0] | DTLRPT[7:0] | Data Learning Pattern Selection | N -> R/W V -> R/W | 0x00 | Description: The DTLRPT[7:0] bits provide the data pattern which is output during Read Latency cycles. This pattern is transferred to the host during SDR/DDR read transaction latency cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits. Selection Options: Pattern Dependency: N/A |

Table 64 DLR feature summary

| Interface Type | SDR | DDR |
|-----------------|-----|-----|
| 1-1-1 | N/A | N/A |
| 1-2-2 | | |
| 1-1-4 | Yes | Yes |
| 1-4-4 | | |
| 4-4-4 | | |
| AutoBoot | N/A | N/A |
| Register Access | | |

Table 65 Data learning pattern behavior

| Interface data type | Latency type 1 | Latency type 2 |
|---------------------|--|-------------------------------|
| SDR | Greater than or equal to 9; DLP on last 8 Clock Cycles | Less than 9; DLP is truncated |
| DDR | Greater than or equal to 5; DLP on last 4 Clock Cycles | Less than 5; DLP is truncated |

5.18 AutoBoot register (ATBN)

The AutoBoot Register (ATBN) provides a means to automatically read boot code as part of the power-on reset, or hardware reset process.

Table 66 AutoBoot Register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory Default (binary) | Description |
|------------|-------------|--|---|-----------------------------|--|
| ATBN[31:9] | STADR[22:0] | Starting Address Selection where AutoBoot will start reading data from | N -> R/W | 0000000000000000 0000000 | Description: The STADR[22:0] bits set the starting address from which the device will output the read data. Selection Options: Address Bits Dependency: N/A |
| ATBN[8:1] | STDLY[7:0] | AutoBoot Read Starting Delay Selection | N -> R/W | 00000000 | Description: The STDLY[7:0] bits specify the initial delay (clock cycles) needed by the host before it can accept data. Note STDLY[7:0]=0x00 is valid up to 50MHz. STDLY[7:0] > 0x00 or higher is valid up to 166MHz. Selection Options: Address Bits Dependency: N/A |
| ATBN[0] | ATBTEN | AutoBoot Feature Selection | N -> R/W | 0 | Description: The ATBTEN bit enables or disables the AutoBoot feature. Selection Options: 0 = AutoBoot feature disabled 1 = AutoBoot feature enabled Dependency: N/A |

5.19 Sector Erase Count Register (SECV)

The Sector Erase Count Register (SECV) contains the number of times the addressed sector has been erased.

Table 67 Sector Erase Count Register

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (hex) | Description |
|------------|--------------|---|---|--------------------------|---|
| SECV[23] | SECCPT | Sector Erase Count Corruption Status Flag | V -> R | 0x0 | Description: The SECCPT bit is used to determine if the reported sector erase count is corrupted and was reset. Note If SECCPT is set due to count corruption, it will reset to 0 on the next successful erase operation on the selected sector. Selection Options: 0 = Sector Erase Count is not corrupted and is valid 1 = Sector Erase Count is corrupted and is not valid Dependency: N/A |
| SECV[22:0] | SECVAL[22:0] | Sector Erase Count Value | V -> R | 0x000000 | Description: The SECVAL[22:0] bits store the number of times a sector has been erased. Selection Options: Value Dependency: N/A |

5.20 Infineon® Endurance Flex architecture selection register (EFXx)

The Infineon® Endurance Flex architecture selection registers (EFXx) define the long retention / high endurance regions based on a four pointer based architecture.

Table 68 Infineon® Endurance Flex architecture selection register (pointer 4)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|-------------|-------------|---|---|-----------------------------|---|
| EFX40[10:2] | EPTAD4[8:0] | Infineon® Endurance Flex architecture Pointer 4 Address Selection | N -> R/1 | 11111111 | Description: The EPTAD4[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A |
| EFX40[1] | ERGNT4 | Infineon® Endurance Flex architecture Pointer 4 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT4 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A |
| EFX40[0] | EPTEB4 | Infineon® Endurance Flex architecture Pointer 4 Enable# Selection | N -> R/1 | 1 | Description: The EPTEB4 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A |

Registers

Table 69 Infineon® Endurance Flex architecture selection register (pointer 3)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|-------------|-------------|---|---|-----------------------------|---|
| EFX30[10:2] | EPTAD3[8:0] | Infineon® Endurance Flex architecture Pointer 3 Address Selection | N -> R/1 | 11111111 | Description: The EPTAD3[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A |
| EFX30[1] | ERGNT3 | Infineon® Endurance Flex architecture Pointer 3 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT3 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A |
| EFX30[0] | EPTEB3 | Infineon® Endurance Flex architecture Pointer 3 Enable# Selection | N -> R/1 | 1 | Description: The EPTEB3 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A |

Table 70 Infineon® Endurance Flex architecture selection register (pointer 2)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|-------------|-------------|---|---|-----------------------------|---|
| EFX20[10:2] | EPTAD2[8:0] | Infineon® Endurance Flex architecture Pointer 2 Address Selection | N -> R/1 | 11111111 | Description: The EPTAD2[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A |
| EFX20[1] | ERGNT2 | Infineon® Endurance Flex architecture Pointer 2 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT2 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A |
| EFX20[0] | EPTEB2 | Infineon® Endurance Flex architecture Pointer 2 Enable# Selection | N -> R/1 | 1 | Description: EPTEB2 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A |

Registers

Table 71 Infineon® Endurance Flex architecture selection register (pointer 1)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|-------------|-------------|---|---|-----------------------------|---|
| EFX10[10:2] | EPTAD1[8:0] | Infineon® Endurance Flex architecture Pointer 1 Address Selection | N -> R/1 | 11111111 | Description: The EPTAD1[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A |
| EFX10[1] | ERGNT1 | Infineon® Endurance Flex architecture Pointer 1 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT1 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A |
| EFX10[0] | EPTEB1 | Infineon® Endurance Flex architecture Pointer 1 Enable# Selection | N -> R/1 | 1 | Description: The EPTEB1 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A |

Table 72 Infineon® Endurance Flex architecture selection register (pointer 0)

| Bit number | Name | Function | Read/Write N = Nonvolatile V = Volatile | Factory default (binary) | Description |
|------------|--------|---|---|-----------------------------|---|
| EFX00[1] | GBLSEL | All Sectors based Region type Selection | N -> R/1 | 1 | Description: The GBLSEL bit defines whether all sectors are defined as long retention region or high endurance region. Note If all other pointer registers are disabled, this bit defines the behavior of the entire memory space and is hardwired to start at Sector 0. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A |
| EFX00[0] | WRLVEN | Wear Leveling Enable Selection | N -> R/1 | 1 | Description: The WRLVEN bit enables/disables the wear leveling feature. Selection Options: 0 = Wear Leveling Disabled 1 = Wear Leveling Enabled Dependency: N/A |

6 Transaction table

6.1 1-1-1 transaction table

Table 73 1-1-1 transaction table

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|-----------------|---|---|--------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Read Device ID | RDIDN_0_0 | Read manufacturer and device identification transaction provides read access to manufacturer and device identification. | - | 9F (CMD) | - | - | - | - | - | - | - | - | Figure 12 | 166 | N/A |
| | RSFDP_3_0 | Read JEDEC Serial Flash Discoverable Parameters transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP). | - | 5A (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | 50 | 3 |
| | RDUID_0_0 | Read Unique ID accesses a factory programmed 64-bit number which is unique to each device. | - | 4C (CMD) | - | - | - | - | - | - | - | - | Figure 12 | 166 | N/A |
| RDSR1_0_0 | Read Status Register 1 transaction allows the Status Register 1 contents to be read from DQ1/SO. | - | 05 (CMD) | - | - | - | - | - | - | - | - | | | | |
| RDSR2_0_0 | Read Status Register-2 transaction allows the Status Register-2 contents to be read from DQ1/SO. | - | 07 (CMD) | - | - | - | - | - | - | - | - | | | | |
| Register Access | RDCR1_0_0 | Read Configuration Register-1 transaction allows the Configuration Register-1 contents to be read from DQ1/SO. | - | 35 (CMD) | - | - | - | - | - | - | - | - | Figure 13 | 166 | 3 |
| | RDARG_C_0 | Read Any Register transaction provides a way to read all addressed nonvolatile and volatile device registers. | - | 65 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | | |
| | RDARG_C_0 | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | 4 | |
| | WRENB_0_0 | Write Enable sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program, and erase transactions. | - | 06 (CMD) | - | - | - | - | - | - | - | - | Figure 7 | 166 | N/A |
| | WRENV_0_0 | Write Enable Volatile enable write of volatile Registers. | - | 50 (CMD) | - | - | - | - | - | - | - | - | | | |
| | WRDIS_0_0 | Write Disable sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program, and erase transactions execution. | - | 04 (CMD) | - | - | - | - | - | - | - | - | | | |
| | WRREG_0_1 | Write Register transaction provides a way to write Status Register 1 and Configuration Registers 1 - 4 | WRENB_0_0 | 01 (CMD) | Input STR1 data [7:0] | Input CFR1 data [7:0] | Input CFR2 data [7:0] | Input CFR3 data [7:0] | Input CFR4 data [7:0] | - | - | - | Figure 11 | 166 | N/A |
| WRRSB_0_1 | SafeBoot Write Register transaction to recover the device from configuration corruption. | WRENB_0_0 | 01 (CMD) | Input STR1 data [7:0] | Input CFR1 data [7:0] | Input CFR2 data [7:0] | Input CFR3 data [7:0] | Input CFR4 data [7:0] | Input 0x00 | - | - | | | | |

Table 73 1-1-1 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length | |
|-----------------|---|--|--------------------------|--------------|----------------------|--------------------|-------------------|------------------|------------------|------------------|-----------------|----------------|--------------------|-----------------|----------------|---|
| Register Access | WRARG_C_1 | Write Any Register transaction provides a way to write all addressed nonvolatile and volatile device registers. | WRENB_0_0 | 71 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | Figure 10 | 166 | 3 | |
| | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | 4 | | | | | |
| | CLPEF_0_0 | Clear Program and Erase Failure Flags transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag) Note This command may be disabled and the instruction value instead used for a program / erase resume command. See Configuration register 3 (CFR3x) on page 80 . | - | 30 (CMD) | - | - | - | - | - | - | - | - | Figure 7 | | N/A | |
| | | | - | 82 (CMD) | - | - | - | - | - | - | - | | | | | |
| | | | - | B7 (CMD) | - | - | - | - | - | - | - | | | | | |
| EN4BA_0_0 | Enter 4 Byte Address Mode transaction sets the Address Legth bit CFR2V[7] to 1 | - | B7 (CMD) | - | - | - | - | - | - | - | - | Figure 12 | | | | |
| EX4BA_0_0 | Exit 4 Byte Address Mode transaction sets the Address Length bit CFR2V[7] to 0 | - | B8 (CMD) | - | - | - | - | - | - | - | | | | | | |
| RDDL_0_0 | Read Data Learning Pattern Register transaction reads the DLP pattern. | - | 41 (CMD) | - | - | - | - | - | - | - | - | Figure 12 | | | | |
| Register Access | PRDLP_0_1 | Program Data Learning Pattern transaction programs DLP pattern into the Nonvolatile registers | WRENB_0_0 | 43 (CMD) | Input DLP data [7:0] | - | - | - | - | - | - | - | Figure 11 | 166 | | |
| | WRDLP_0_1 | Write Data Learning Pattern transaction writes DLP pattern into the Volatile register. | WRENB_0_0 | 4A (CMD) | Input DLP data [7:0] | - | - | - | - | - | - | - | | | | |
| | WRAUB_0_1 | AutoBoot Register Write transaction writes AutoBoot pattern into the register. | WRENB_0_0 | 15 (CMD) | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | - | - | - | | | | |
| ECC | RDECC_C_0 | Read ECC Status is used to determine the ECC status of the addressed data unit. | - | 19 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | | 166 | 3 |
| | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | | | |
| ECC | RDECC_4_0 | - | - | 18 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | Figure 7 | N/A | | |
| | CLECC_0_0 | Clear ECC Status Register transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | - | 1B (CMD) | - | - | - | - | - | - | - | - | | | | |
| CRC | DICHK_4_1 | Data Integrity Check transaction causes the device to perform a Data Integrity Check over a user defined address range. | - | 5B (CMD) | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24] | End ADDR [23:16] | End ADDR [15:8] | End ADDR [7:0] | Figure 9 | | | 4 |

Table 73 1-1-1 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length | |
|-------------------|---|---|---|----------------|--------------|--------------|--------------|--------------------|--------------------|--------------------|--------------|--------------|--------------------|-----------------|----------------|---|
| Read Flash Array | RDAY1_C_0 | Read SDR transaction reads out the memory contents starting at the given address. | - | 03 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 14 | 50 | 3 | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | | |
| | RDAY1_4_0 | | - | 13 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | |
| | RDAY2_C_0 | | Read Fast SDR transaction reads out the memory contents starting at the given address. | - | 0B (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | 166 | 3 |
| | | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | |
| | RDAY2_4_0 | | | - | 0C (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | - |
| PRPGE_C_1 | Program Page programs 256B or 512B data to the memory array in one transaction. | WRENB_0_0 | | 02 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | Figure 10 | 3 | | |
| | | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | | 4 | | |
| PRPGE_4_1 | | WRENB_0_0 | | 12 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | - | | |
| ER004_C_0 | | Erase 4KB Sector transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh). | WRENB_0_0 | 20 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 8 | 3 | | |
| | ADDR [31:24] | | | | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | | | |
| ER004_4_0 | WRENB_0_0 | | 21 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | | | |
| ER256_C_0 | Erase 256KB Sector transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh). | | WRENB_0_0 | D8 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 7 | 3 | | |
| | | ADDR [31:24] | | | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | | | |
| ER256_4_0 | | WRENB_0_0 | DC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | | | |
| ERCHP_0_0 | | Erase Chip transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. | WRENB_0_0 | 60 or C7 (CMD) | - | - | - | - | - | - | - | - | - | N/A | | |
| Erase Flash Array | EVERS_C_0 | Evaluate Erase Status transaction verifies that the last erase operation on the addressed sector was completed successfully. | - | D0 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 8 | 3 | | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | | |
| | SEERC_C_0 | | Sector Erase Count transaction outputs the number of erase cycles for the sector of the inputted address from the Sector Erase Count Register. | - | 5D (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | 3 | | |
| | | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | |

Table 73 1-1-1 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|-----------------------------|--|---|--------------------------|--------------|--------------------|---------------------|--------------|--------------------|--------------------|--------------------|--------------|--------------|--------------------|-----------------|----------------|
| Suspend / Resume | SPEPD_0_0 | Suspend Erase / Program / Data Integrity Check transaction allows the system to interrupt a programming, erase or data integrity check operation | - | 75 (CMD) | - | - | - | - | - | - | - | - | Figure 7 | 166 | N/A |
| | SPEPA_0_0 | Suspend Erase / Program alternate transaction allows the system to interrupt a programming or erase. | - | 85 (CMD) | - | - | - | - | - | - | - | - | | | |
| | | | - | B0 (CMD) | - | - | - | - | - | - | - | - | | | |
| | RSEPD_0_0 | Resume Erase / Program / Data Integrity Check transaction allows the system to resume a programming, erase or data integrity check operation | - | 7A (CMD) | - | - | - | - | - | - | - | - | | | |
| RSEPA_0_0 | Resume Erase / Program alternate transaction allows the system to resume a programming, erase or data integrity check operation | - | 8A (CMD) | - | - | - | - | - | - | - | - | | | | |
| | | - | 30 (CMD) | - | - | - | - | - | - | - | - | - | | | |
| Secure Silicon Region Array | PRSSR_C_1 | Program Secure Silicon Region transaction programs data in 1024 bytes of Secure Silicon Region | WRENB_0_0 | 42 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | Figure 10 | 166 | 4 |
| | | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | | | |
| | RDSSR_C_0 | Read Secure Silicon Region transaction reads data from the SSR. | - | 4B (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | |
| Advanced Sector Protection | PRASP_0_1 | ASP Register Write | WRENB_0_0 | 2F (CMD) | ASP Low Byte [7:0] | ASP High Byte [7:0] | - | - | - | - | - | - | Figure 11 | 166 | N/A |
| | RDDYB_C_0 | Read Dynamic Protection Bit transaction reads the contents of the DYB Access register. | - | FA (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| | | | - | | E0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | | | - |
| | WRDYB_C_1 | Write Dynamic Protection Bit transaction writes to the DYB Access register | WRENB_0_0 | FB (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | Figure 10 | | 3 |
| WRENB_0_0 | | | E1 (CMD) | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | | 4 | |

Table 73 1-1-1 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length | |
|----------------------------|------------------|---|--------------------------|--------------|----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------------|-----------------|----------------|--|
| Advanced Sector Protection | RDPPB_C_0 | Read Persistent Protection Bit transaction reads the contents of the PPB Access register | - | FC (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 13 | 166 | 3 | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 | |
| | RDPPB_4_0 | | - | E2 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 | |
| | PRPPB_C_0 | Program Persistent Protection Bit transaction programs / writes the PPB register to enable the sector protection. | WRENB_0_0 | FD (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 8 | | 3 | |
| | PRPPB_4_0 | | WRENB_0_0 | E3 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 | |
| | ERPPB_0_0 | Erase Persistent Protection Bit transaction sets all persistent protection bits to 1. | WRENB_0_0 | E4 (CMD) | - | - | - | - | - | - | - | - | Figure 7 | | N/A | |
| | WRPLB_0_0 | Write PPB Protection Lock Bit transaction clears the PPB Lock to 0. | WRENB_0_0 | A6 (CMD) | - | - | - | - | - | - | - | - | | | | |
| | RDPLB_0_0 | Read Program Persistent Protection Lock Bit transaction shifts out the 8-bit PPB Lock register contents with MSb first | - | A7 (CMD) | - | - | - | - | - | - | - | - | Figure 12 | | | |
| | PGPWD_0_1 | Program Password transaction programs the 64-bit password to flash device. | WRENB_0_0 | E8 (CMD) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | Figure 11 | | | |
| | PWDUL_0_1 | Password Unlock transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | - | E9 (CMD) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | | | | |
| Reset | SRSTE_0_0 | Software Reset Enable command is required immediately before a SFRST_0_0 transaction | - | 66 (CMD) | - | - | - | - | - | - | - | - | Figure 7 | | | |
| | SFRST_0_0 | Software Reset transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values | SRSTE_0_0 | 99 (CMD) | - | - | - | - | - | - | - | - | | | | |
| | SFRSL_0_0 | Legacy Software Reset transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values | - | F0 (CMD) | - | - | - | - | - | - | - | - | | | | |
| Deep Power Down | ENDPD_0_0 | Enter Deep Power Down Mode transaction shifts device in the lowest power consumption mode | - | B9 (CMD) | - | - | - | - | - | - | - | - | | | | |

6.2 1-2-2 Transaction Table

Table 74 1-2-2 transaction table

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|------------------|------------------|--|--------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Read Flash Array | RDAY3_C_0 | Read SDR Dual I/O transaction reads out the memory contents starting at the given address. | - | BB (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | Figure 16 | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | 4 |
| | RDAY3_4_0 | | - | BC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | Figure 17 | | 3 |
| | RDAY6_C_0 | | RDAY3_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | | | 4 |
| | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | | - |
| | RDAY6_4_0 | | RDAY3_4_0 | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | | - |

6.3 1-1-4 transaction table

Table 75 1-1-4 transaction table

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|------------------|------------------|---|--------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Read Flash Array | RDAY4_C_0 | Read SDR Quad Output transaction reads out the memory contents starting at the given address. | - | 6B (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 18 | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| | RDAY4_4_0 | | - | 6C (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | |



6.4 1-4-4 transaction table

Table 76 1-4-4 transaction table

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|---------------------------------|---|---|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Read Manufacturer and Device ID | RDQID_0_0 | Read Quad manufacturer and device identification transaction provides read access to manufacturer and device identification. | - | AF (CMD) | - | - | - | - | - | - | - | - | Figure 23 | 166 | N/A |
| | RDAY5_C_0 | Read SDR Quad I/O transaction reads out the memory contents starting at the given address. | - | EB (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | Figure 19 | | 3 |
| RDAY5_4_0 | - | | ADDR [31:24] | | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | 4 | | | |
| RDAY6_C_0 | Continuous Read SDR Quad I/O transaction reads out the memory contents starting at the given address. | | RDAY5_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | 3 | | | |
| RDAY6_4_0 | | RDAY5_4_0 | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | 4 | | | | |
| Read Flash Array | RDAY7_C_0 | Read DDR Quad I/O transaction reads out the memory contents starting at the given address. | - | ED (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | Figure 21 | 102 | 3 |
| | RDAY7_4_0 | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | 4 |
| | RDAY8_C_0 | | Continuous Read DDR Quad I/O transaction reads out the memory contents starting at the given address. | RDAY7_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | | 3 |
| | RDAY8_4_0 | RDAY7_4_0 | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | 4 | | | |
| | RDAY7_C_0 | Continuous Read SDR Quad I/O transaction reads out the memory contents starting at the given address. | RDAY5_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | 3 | | | |
| | RDAY7_4_0 | | RDAY5_4_0 | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | 4 | | | |

6.5 4-4-4 transaction table

Table 77 4-4-4 transaction table

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|-----------------|--|---|--------------------------|--------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Read device ID | RDIDN_0_0 | Read manufacturer and device identification transaction provides read access to manufacturer and device identification. | - | 9F (CMD) | - | - | - | - | - | - | - | - | Figure 31 | 166 | N/A |
| | RSFDP_3_0 | Read JEDEC Serial Flash Discoverable Parameters transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP). | - | 5A (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 35 | 50 | 3 |
| | RDQID_0_0 | Read Quad manufacturer and device identification transaction provides read access to manufacturer and device identification. | - | AF (CMD) | - | - | - | - | - | - | - | - | Figure 31 | 166 | N/A |
| | RDUID_0_0 | Read Unique ID accesses a factory programmed 64-bit number which is unique to each device. | - | 4C (CMD) | - | - | - | - | - | - | - | - | | | |
| Register access | RDSR1_0_0 | Read Status Register 1 transaction allows the Status Register 1 contents to be read from DQ1/SO. | - | 05 (CMD) | - | - | - | - | - | - | - | - | Figure 31 | 166 | N/A |
| | RDSR2_0_0 | Read Status Register-2 transaction allows the Status Register-2 contents to be read from DQ1/SO. | - | 07 (CMD) | - | - | - | - | - | - | - | - | | | |
| | RDCR1_0_0 | Read Configuration Register-1 transaction allows the Configuration Register-1 contents to be read from DQ1/SO. | - | 35 (CMD) | - | - | - | - | - | - | - | - | | | |
| | RDARG_C_0 | Read Any Register transaction provides a way to read all addressed nonvolatile and volatile device registers. | - | 65 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 35 | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | |
| | WRENB_0_0 | Write Enable sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program, and erase transactions. | - | 06 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | 166 | N/A |
| | WRENV_0_0 | Write Enable Volatile enable write of volatile Registers. | - | 50 (CMD) | - | - | - | - | - | - | - | - | | | |
| | WRDIS_0_0 | Write Disable sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program, and erase transactions execution. | - | 04 (CMD) | - | - | - | - | - | - | - | - | | | |
| | WRREG_0_1 | Write Register transaction provides a way to write Status Register 1 and Configuration Registers 1 - 4 | WRENB_0_0 | 01 (CMD) | Input STR1 data [7:0] | Input CFR1 data [7:0] | Input CFR2 data [7:0] | Input CFR3 data [7:0] | Input CFR4 data [7:0] | - | - | - | Figure 35 | 166 | N/A |
| WRARG_C_1 | Write Any Register transaction provides a way to write all addressed nonvolatile and volatile device registers. | WRENB_0_0 | 71 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | Figure 35 | 3 | | | |
| | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | | - | 4 | | |

Table 77 4-4-4 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length | |
|------------------|------------------|---|--------------------------|--------------|----------------------|--------------------|-------------------|------------------|------------------|------------------|-----------------|----------------|--------------------|-----------------|----------------|---|
| Register access | CLPEF_0_0 | Clear Program and Erase Failure Flags transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag) | - | 30 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | 166 | N/A | |
| | | Note This command may be disabled and the instruction value instead used for a program / erase resume command. See Configuration register 3 (CFR3x) on page 80. | - | 82 (CMD) | - | - | - | - | - | - | - | - | | | | - |
| | EN4BA_0_0 | Enter 4 Byte Address Mode transaction sets the Address Legth bit CFR2V[7] to 1 | - | B7 (CMD) | - | - | - | - | - | - | - | - | | | | |
| | EX4BA_0_0 | Exit 4 Byte Address Mode transaction sets the Address Legth bit CFR2V[7] to 0 | - | B8 (CMD) | - | - | - | - | - | - | - | - | | | | |
| | RDDL_0_0 | Read Data Learning Pattern Register transaction reads the DLP pattern. | - | 41 (CMD) | - | - | - | - | - | - | - | - | Figure 31 | | | |
| | PRDLP_0_1 | Program Data Learning Pattern transaction programs DLP pattern into the Nonvolatile registers | WRENB_0_0 | 43 (CMD) | Input DLP data [7:0] | - | - | - | - | - | - | - | Figure 35 | | N/A | |
| | WRDLP_0_1 | Write Data Learning Pattern transaction writes DLP pattern into the Volatile register. | WRENB_0_0 | 4A (CMD) | Input DLP data [7:0] | - | - | - | - | - | - | - | | | | |
| | WRAUB_0_1 | AutoBoot Register Write transaction writes AutoBoot pattern into the register. | WRENB_0_0 | 15 (CMD) | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | - | - | - | | | | |
| ECC | RDECC_C_0 | Read ECC Status is used to determine the ECC status of the addressed data unit. | - | 19 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 35 | 166 | 3 | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | | | | | |
| | RDECC_4_0 | - | 18 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | 4 | | | |
| | CLECC_0_0 | Clear ECC Status Register transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | - | 1B (CMD) | - | - | - | - | - | - | - | - | Figure 24 | | N/A | |
| CRC | DICHK_4_1 | Data Integrity Check transaction causes the device to perform a Data Integrity Check over a user defined address range. | - | 5B (CMD) | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24] | End ADDR [23:16] | End ADDR [15:8] | End ADDR [7:0] | Figure 28 | | 4 | |
| Read flash array | RDAY5_C_0 | Read QPI SDR transaction reads out the memory contents starting at the given address. | - | EB (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | Figure 35 | 166 | 3 | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | | |
| | RDAY2_4_0 | | - | 0C (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | | 4 |
| | RDAY5_4_0 | | - | EC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | | |

Table 77 4-4-4 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|---------------------|------------------|--|--------------------------|----------------|--------------|--------------|--------------|--------------------|--------------------|--------------------|--------------|--------------|--------------------|-----------------|----------------|
| Read flash array | RDAY6_C_0 | Continuous Read QPI SDR transaction reads out the memory contents starting at the given address. | RDAY5_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | - | Figure 33 | 166 | 3 |
| | RDAY6_4_0 | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | | 4 |
| | RDAY7_C_0 | Read QPI DDR transaction reads out the memory contents starting at the given address. | - | ED (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | Figure 35 | | 3 |
| | RDAY7_4_0 | | | EE (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | | | 4 |
| | RDAY8_C_0 | Continuous Read QPI DDR transaction reads out the memory contents starting at the given address. | RDAY7_C_0 | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | - | Figure 35 | | 3 |
| | RDAY8_4_0 | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Mode [7:0] | - | - | - | - | | | 4 |
| Program flash array | PRPGE_C_1 | Program Page programs 256B or 512B data to the memory array in one transaction. | WRENB_0_0 | 02 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | Figure 26 | 3 | |
| | PRPGE_4_1 | | | 12 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | | 4 | |
| Erase flash array | ER004_C_0 | Erase 4KB Sector transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh). | WRENB_0_0 | 20 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 26 | 3 | |
| | ER004_4_0 | | | 21 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | 4 | |
| | ER256_C_0 | Erase 256KB Sector transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh). | WRENB_0_0 | D8 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 26 | 3 | |
| | ER256_4_0 | | | DC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | 4 | |
| | ERCHP_0_0 | Erase Chip transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. | WRENB_0_0 | 60 or C7 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | N/A | |



Table 77 4-4-4 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|-----------------------------|---|--|--------------------------|--------------|--------------------|---------------------|--------------|--------------------|--------------------|--------------------|--------------|--------------|--------------------|-----------------|----------------|
| Erase flash array | EVERS_C_0 | Evaluate Erase Status transaction verifies that the last erase operation on the addressed sector was completed successfully. | - | D0 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | Figure 35 | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | |
| | SEERC_C_0 | Sector Erase Count transaction outputs the number of erase cycles for the sector of the inputted address from the Sector Erase Count Register. | - | 5D (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | 4 | | | |
| Suspend / resume | SPEPD_0_0 | Suspend Erase / Program / Data Integrity Check transaction allows the system to interrupt a programming, erase or data integrity check operation | - | 75 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | 166 | N/A |
| | SPEPA_0_0 | Suspend Erase / Program alternate transaction allows the system to interrupt a programming or erase. | - | 85 (CMD) | - | - | - | - | - | - | - | - | | | |
| | | | - | B0 (CMD) | - | - | - | - | - | - | - | - | | | |
| | RSEPD_0_0 | Resume Erase / Program / Data Integrity Check transaction allows the system to resume a programming, erase or data integrity check operation | - | 7A (CMD) | - | - | - | - | - | - | - | - | | | |
| - | | | 8A (CMD) | - | - | - | - | - | - | - | - | | | | |
| RSEPA_0_0 | Resume Erase / Program alternate transaction allows the system to resume a programming, erase or data integrity check operation | - | 8A (CMD) | - | - | - | - | - | - | - | - | - | | | |
| | | - | 30 (CMD) | - | - | - | - | - | - | - | - | - | | | |
| Secure silicon region array | PRSSR_C_1 | Program Secure Silicon Region transaction programs data in 1024 bytes of Secure Silicon Region | WRENB_0_0 | 42 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | Figure 35 | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | | | 4 |
| | RDSSR_C_0 | Read Secure Silicon Region transaction reads data from the SSR. | - | 4B (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| Advanced sector protection | PRASP_0_1 | ASP Register Write | WRENB_0_0 | 2F (CMD) | ASP Low Byte [7:0] | ASP High Byte [7:0] | - | - | - | - | - | - | 3 | N/A | |
| | RDDYB_C_0 | Read Dynamic Protection Bit transaction reads the contents of the DYB Access register. | - | FA (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | 3 | | |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | 4 | | |
| RDDYB_4_0 | - | E0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | 4 | | | |

Table 77 4-4-4 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length | | | | | | | | |
|----------------------------|---|--|--------------------------|----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------------|-----------------|----------------|-----|-----------|-----|-----------|-----|-----------|-----|---|
| Advanced sector protection | WRDYB_C_1 | Write Dynamic Protection Bit transaction writes to the DYB Access register | WRENB_0_0 | FB (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | Figure 35 | 166 | 3 | | | | | | | | |
| | WRDYB_4_1 | | | E1 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | | | 4 | | | | | | | | |
| | RDPPB_C_0 | Read Persistent Protection Bit transaction reads the contents of the PPB Access register | - | FC (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | | Figure 26 | 166 | 3 | | | | | | |
| | RDPPB_4_0 | | | E2 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | | | 4 | | | | | | |
| | PRPPB_C_0 | Program Persistent Protection Bit transaction programs / writes the PPB register to enable the sector protection. | WRENB_0_0 | FD (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | | | | | Figure 24 | 166 | 3 | | | | |
| | PRPPB_4_0 | | | E3 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | | | | | 4 | | | | |
| | ERPPB_0_0 | Erase Persistent Protection Bit transaction sets all persistent protection bits to 1. | WRENB_0_0 | E4 (CMD) | - | - | - | - | - | - | - | - | | | | | | | Figure 31 | 166 | - | | |
| | WRPLB_0_0 | Write PPB Protection Lock Bit transaction clears the PPB Lock to 0 | WRENB_0_0 | A6 (CMD) | - | - | - | - | - | - | - | - | | | | | | | | | - | - | |
| | RDPLB_0_0 | Read Program Persistent Protection Lock Bit transaction shifts out the 8-bit PPB Lock register contents with MSb first | - | A7 (CMD) | - | - | - | - | - | - | - | - | | | | | | | | | - | - | - |
| | PGPWD_0_1 | Program Password transaction programs the 64-bit password to flash device. | WRENB_0_0 | E8 (CMD) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | | | | | | | | | Figure 35 | N/A | - |
| PWDUL_0_1 | Password Unlock transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | - | E9 (CMD) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | - | - | | | | | | | | | | |
| Reset | SRSTE_0_0 | Software Reset Enable command is required immediately before a SFRST_0_0 transaction | - | 66 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | 166 | | | | | | | | | - |
| | SFRST_0_0 | Software Reset transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values | SRSTE_0_0 | 99 (CMD) | - | - | - | - | - | - | - | - | | | - | - | | | | | | | |



Table 77 4-4-4 transaction table (continued)

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max freq. (MHz) | Address length |
|-----------------|------------------|---|--------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------------|-----------------|----------------|
| Reset | SFRSL_0_0 | Legacy Software Reset transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values | - | F0 (CMD) | - | - | - | - | - | - | - | - | Figure 24 | 166 | N/A |
| Deep Power Down | ENDPD_0_0 | Enter Deep Power Down Mode transaction shifts device in the lowest power consumption mode | - | B9 (CMD) | - | - | - | - | - | - | - | | | | |

7 Electrical characteristics

7.1 Absolute maximum ratings^[33, 34, 35]

| | |
|--|---------------------------------|
| Storage Temperature Plastic Packages..... | -65 °C to +150 °C |
| Ambient Temperature with Power Applied..... | -65 °C to +125 °C |
| V _{CC} (HL-T)..... | -0.5V to +4.0V |
| V _{CC} (HS-T)..... | -0.5V to +2.5V |
| Input voltage with respect to Ground (V _{SS})..... | -0.5V to V _{CC} + 0.5V |
| Output Short Circuit Current..... | 100 mA |

7.2 Operating range

Operating ranges define those limits between which the functionality of the device is guaranteed.

7.2.1 Power supply voltages

| | |
|-------------------------------------|--------------|
| V _{CC} (HL-T Devices)..... | 2.7V to 3.6V |
| V _{CC} (HS-T Devices)..... | 1.7V to 2.0V |

7.2.2 Temperature ranges^[36]

Table 78 Temperature ranges

| Parameter | Symbol | Devices | Spec | | Unit |
|---------------------|----------------|---|------|------|------|
| | | | Min | Max | |
| Ambient Temperature | T _A | Industrial / Automotive AEC-Q100 Grade 3 | -40 | +85 | °C |
| | | Industrial Plus / Automotive AEC-Q100 Grade 2 | | +105 | |
| | | Automotive AEC-Q100 Grade 1 | | +125 | |

Note

36. Industrial Plus, Automotive Grade-2 and Automotive Grade-1 operating and performance parameters will be determined by device characterization and may vary from standard industrial or Automotive Grade-3 temperature range devices as currently shown in this specification.

Notes

- 33. See [Input signal overshoot on page 106](#) for allowed maximums during signal transition.
- 34. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
- 35. Stresses above those listed under [Absolute maximum ratings\[33, 34, 35\] on page 104](#) may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical characteristics

7.3 Thermal resistance

Table 79 Thermal resistance

| Parameter | Description | Test condition | Device | 24-ball BGA | 16-lead SOIC | 8-contact WSON | Unit |
|-----------|--|--|--------|-------------|--------------|----------------|------|
| Theta JA | Thermal Resistance (Junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. With Still Air (0 m/s). | 256T | 35.2 | 36.4 | 31 | °C/W |
| | | | 512T | 40.4 | 35 | 32.7 | |
| | | | 01GT | 37 | 28.3 | - | |
| Theta JB | Thermal Resistance (Junction to board) | | 256T | 19 | 9 | 17.5 | °C/W |
| | | | 512T | 14.5 | 19 | 12.5 | |
| | | | 01GT | 9.7 | 12 | - | |
| Theta JC | Thermal Resistance (Junction to case) | | 256T | 11 | 8 | 13.1 | °C/W |
| | | | 512T | 8 | 9.9 | 13 | |
| | | | 01GT | 7.5 | 7.6 | - | |

7.4 Capacitance characteristics

Table 80 Capacitance

| Package | Input capacitance | | Output capacitance | |
|----------------|-------------------|---------|--------------------|---------|
| | Typical | Maximum | Typical | Maximum |
| 24-ball BGA | 3.0 pF | 6.5 pF | 7.0 pF | 7.5 pF |
| 16-lead SOIC | 4.0 pF | | 7.5 pF | 8.0 pF |
| 8-contact WSON | 3.0 pF | | 6.7 pF | 7.5 pF |

7.5 Latchup characteristics

Table 81 Latchup specification^[37]

| Description | Min | Max | Unit |
|---|------|-----------------------|------|
| Input voltage with respect to V _{SS} on all input only connections | -1.0 | V _{CC} + 1.0 | V |
| Input voltage with respect to V _{SS} on all I/O connections | | | |
| V _{CC} Current | -100 | +100 | mA |

Note

37. Excludes power supply V_{CC}. Test conditions: V_{CC} = 1.8V / 3.0V, one connection at a time tested, connections not being tested are at V_{SS}.

7.6 DC characteristics

7.6.1 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC} . During voltage transitions, inputs or I/Os may overshoot V_{SS} to $-1.0V$ or overshoot to $V_{CC} + 1.0V$, for periods up to 20 ns.

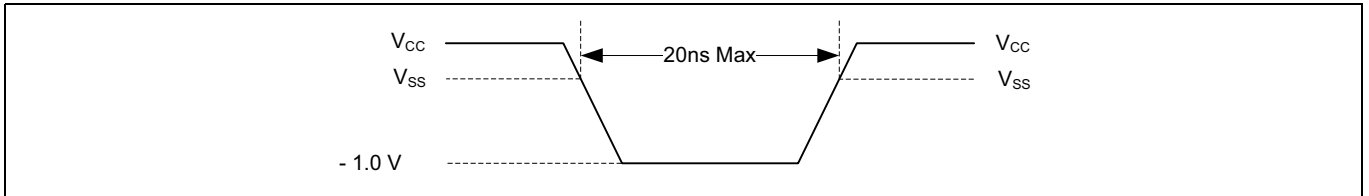


Figure 70 Maximum negative overshoot waveform

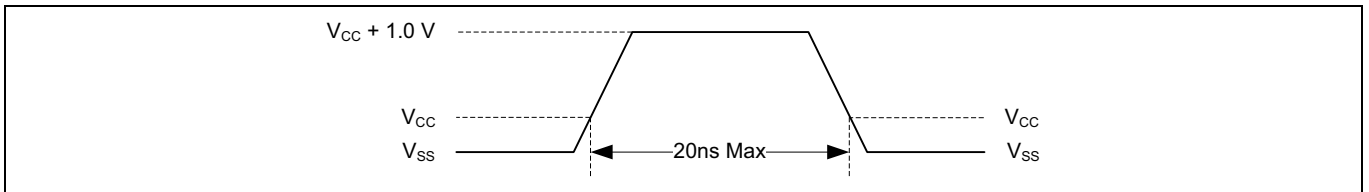


Figure 71 Maximum positive overshoot waveform

Electrical characteristics

7.6.2 DC characteristics (all temperature ranges)

Table 82 DC characteristics^[38, 39]

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|------------------|--|--|---|--|-------------------------------|------|------------------|
| V _{IL} | Input Low Voltage (all V _{CC}) | – | V _{CC} × -0.15 | – | V _{CC} × 0.35 | V | |
| V _{IH} | Input High Voltage (all V _{CC}) | – | V _{CC} × 0.65 | – | V _{CC} × 1.15 | | |
| V _{OL} | Output Low Voltage (all V _{CC}) | At 0.1 mA | – | – | 0.2 | | |
| V _{OH} | Output High Voltage (all V _{CC}) | At -0.1 mA | V _{CC} - 0.20 | – | – | | |
| I _{LI} | Input Leakage Current | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 85 °C | – | – | ±2 | µA | |
| | | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 105 °C | – | – | ±3 | | |
| | | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 125 °C | – | – | ±4 | | |
| I _{LO} | Output Leakage Current | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 85 °C | – | – | ±2 | | |
| | | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 105 °C | – | – | ±3 | | |
| | | V _{CC} = V _{CC} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH} , 125 °C | – | – | ±4 | | |
| I _{CC1} | Active Power Supply Current (READ) ^[39] | SDR @ 50MHz (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | 14 / 18 10 / 10 18 / 14 | 25 / 25 21 / 18 25 / 25 | mA | – |
| | | SDR @ 166MHz (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | 53 53 53 | 69 / 72 69 / 69 69 / 72 | | |
| | | DDR @ 102MHz | – | 50 | 68 | | |
| | | I _{CC2} | Active Power Supply Current (Page Program) (256T / 512T / 01GT) | V _{CC} = V _{CC} Max, CS# = V _{IH} | – | | |
| I _{CC3} | Active Power Supply Current (Write Register and Write Any Register) (256T / 512T / 01GT) | V _{CC} = V _{CC} Max, CS# = V _{IH} | – | 50 | 55 / 55 / 66 | | |
| I _{CC4} | Active Power Supply Current (Sector Erase) (256T / 512T / 01GT) | V _{CC} = V _{CC} Max, CS# = V _{IH} | – | 50 | 55 / 55 / 66 | | |
| I _{CC5} | Active Power Supply Current (Chip Erase) (256T / 512T / 01GT) | V _{CC} = V _{CC} Max, CS# = V _{IH} | – | 50 | 55 / 55 / 66 | | |
| I _{SB} | Standby Current (HS256T / HS512T / HS01GT) | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 85 °C | – | 11 | 160 / 113 / 160 | µA | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 105 °C | – | | 220 / 188 / 220 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 125 °C | – | | 510 / 340 / 510 | | |
| | Standby Current (HL256T / HL512T / HL01GT) | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 85 °C | – | 14 | 160 / 126 / 160 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 105 °C | – | | 425 / 188 / 425 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 125 °C | – | | 560 / 340 / 560 | | |
| I _{DPD} | DPD Current (HS256T / HS512T / HS01GT) | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 85 °C | – | 1.3 | 24 / 18 / 24 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 105 °C | – | | 26 / 18 / 26 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 125 °C | – | | 56 / 31 / 56 | | |

Notes

38. Typical values are at T_{AJ} = 25 °C and V_{CC} = 1.8V/3.0V.

39. Outputs unconnected during read data return. Output switching current is not included.

Electrical characteristics

Table 82 DC characteristics^[38, 39] (continued)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|--------------------------------------|---|---|------|-----|--------------|------|-----------------------|
| I _{DPD} | DPD Current (HL256T / HL512T / HL01GT) | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 85°C | – | 2.2 | 18 / 18 / 26 | μA | – |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 105°C | – | | 18 / 18 / 26 | | |
| | | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} , 125°C | – | | 60 / 31 / 60 | | |
| I _{POR} | POR Current | RESET#, CS# = V _{CC} ; All I/Os = V _{CC} or V _{SS} | – | – | 80 | mA | |
| Power Up / Power Down Voltage | | | | | | | |
| V _{CC} (min) | V _{CC} (minimum operation voltage, HL-T) | – | 2.7 | – | – | V | Figure 66 / Figure 67 |
| | V _{CC} (minimum operation voltage, HS-T) | – | 1.7 | – | – | | |
| V _{CC} (cut-off) | V _{CC} (cut off where re-initialization is needed, HL-T) | – | 2.4 | – | – | V | Figure 67 |
| | V _{CC} (cut off where re-initialization is needed, HS-T) | – | 1.55 | – | – | | |
| V _{CC} (Low) | V _{CC} (low voltage for initialization to occur, HL-T) | – | 0.7 | – | – | V | Figure 67 |
| | V _{CC} (low voltage for initialization to occur, HS-T) | – | 0.7 | – | – | | |

Notes

38. Typical values are at T_{AI} = 25 °C and V_{CC} = 1.8V/3.0V.

39. Outputs unconnected during read data return. Output switching current is not included.

7.7 AC test conditions

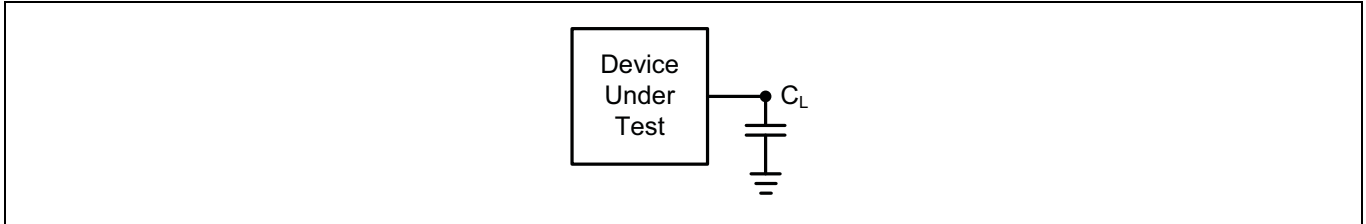


Figure 72 Test Setup

Table 83 AC measurement conditions^[41]

| Parameter | Min | Max | Unit | Reference figure |
|---|-------------------------|------------------------|------|---------------------------|
| Load Capacitance (C _L) | – | 30 | pF | Figure 72 |
| Input Pulse Voltage | 0 | V _{CC} | V | – |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 100MHz (HL-T) ^[40] | 1.03 | - | V/ns | Figure 78 |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 133MHz (HL-T) ^[40] | 1.37 | - | | |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 166MHz (HL-T) ^[40] | 1.72 | - | | |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 100MHz (HS-T) ^[40] | 0.38 | - | | |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 133MHz (HS-T) ^[40] | 0.75 | - | | |
| Input Rise (t _{CRT}) and Fall (t _{CFT}) Slew Rates at 166MHz (HS-T) ^[40] | 0.94 | - | | |
| V _{IL(ac)} | -0.30 × V _{CC} | 0.30 × V _{CC} | V | – |
| V _{IH(ac)} | 0.7 × V _{CC} | 1.30 × V _{CC} | | |
| V _{OH(ac)} | 0.75 × V _{CC} | - | | |
| V _{OL(ac)} | – | 0.25 × V _{CC} | | |
| Input Timing Ref Voltage | 0.5 × V _{CC} | | | |
| Output Timing Ref Voltage | | | | |

Notes

40. Input slew rate measured from input pulse min to max at V_{CC} max.

41. AC characteristics tables assume clock and data signals have the same slew rate (slope).

Timing characteristics

8 Timing characteristics

Table 84 Timing characteristics^[43]

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure | |
|-----------------------------------|--|--------------|-----|--------------|------|------------------|------------------|
| SDR timing characteristics | | | | | | | |
| f_{CK} | Clock Frequency | DC | – | 166 | MHz | – | |
| p_{CK} | CK Clock Period | $1/f_{CK}$ | – | ∞ | | Figure 78 | |
| t_{CH} | Clock High Time | 45% p_{CK} | – | 55% p_{CK} | | | |
| t_{CL} | Clock Low Time | | – | | | | |
| t_{CS} | CS# High Time (Read transactions) | 10 | – | – | | | Figure 79 |
| | CS# High Time Between Transactions (Read transactions when Reset feature and Quad mode are both enabled and aborted transaction) | 20 | – | – | | | |
| | CS# High Time (Program / Erase transactions) | 50 | – | – | | | |
| t_{CSS} | CS# Active Setup Time relative to CK ($f_{CK} \leq 50\text{MHz}$ / $f_{CK} > 50\text{MHz}$) | 5/4 | – | – | | | |
| t_{CSH0} | CS# Active Hold Time (relative to CK in Mode 0) | 4 | – | – | | | |
| t_{CSH3} | CS# Active Hold Time (relative to CK in Mode 3) | 6 | – | – | | | |
| t_{SU} | Data Setup Time (all V_{CC}) ($f_{CK} \leq 50\text{MHz}$ / $f_{CK} > 50\text{MHz}$) | 5 / 2 | – | – | | | |
| t_{HD} | Data Hold Time (all V_{CC}) ($f_{CK} \leq 50\text{MHz}$ / $f_{CK} > 50\text{MHz}$) | | – | – | | | |
| $t_V^{[43]}$ | Clock Low to Output Valid (15pF Loading, 3.0V – 3.6V, 30 Ω Output Impedance, 105°C) (HL-T) Note Guaranteed by design. | 2 | – | 6.5 | ns | Figure 80 | |
| | Clock Low to Output Valid (15pF Loading) (HS-T) | | | 6 | | | |
| | Clock Low to Output Valid (15pF Loading) (HL-T) | | | 8 | | | |
| | Clock Low to Output Valid (30pF Loading) (HS-T) | | | 9 | | | |
| | Clock Low to Output Valid (30pF Loading) (HL-T) | | | 9 | | | |
| t_{HO} | Output Hold Time | 1.5 | – | – | | | |
| $t_{DIS}^{[42]}$ | CS# Inactive to Output Disable Time (HS-T) | – | – | 8 | | | |
| | CS# Inactive to Output Disable Time (HL-T) | – | – | 9 | | | |
| | CS# Inactive to Output Disable Time (when Reset feature and Quad mode are both enabled) | – | – | 20 | | | |
| t_{WPS} | WP# Setup Time (Applicable as a constraint for write register transactions when STCFWR is set to a 1) | 20 | – | – | | | Figure 81 |
| t_{WPH} | WP# Hold Time (Applicable as a constraint for write register transactions when STCFWR is set to a 1) | 20 | – | – | | | |
| $t_{IO_SKEW}^{[49]}$ | Data Skew (First Data Bit to Last Data Bit) | – | – | 0.6 | | – | |
| DDR timing characteristics | | | | | | | |
| f_{CK} | CK Clock Frequency | DC | – | 102 | MHz | – | |

Notes

42. Output HI-Z is defined as the point where data is no longer driven.
43. Applicable across all operating temperature options.
44. If Reset# is asserted during the end of t_{PU} , the device will remain in the reset state and t_{RH} will determine when CS# may go Low.
45. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH} .
46. Typical program and erase times assume the following conditions: 25°C, $V_{CC} = 1.8\text{V}$ and 3.0V; checkerboard data pattern.
47. The programming time for any OTP programming transaction is the same as t_{pp} .
48. The programming time for the PRPPB_4_0 and PRPPB_C_0 transactions is the same as t_{pp} . The erase time for ERPPB_0_0 transaction is the same as t_{SE} .
49. Values are guaranteed by characterization and not 100% tested in production.
50. Guaranteed by design.
51. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Timing characteristics

Table 84 Timing characteristics^[43] (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|-----------------------|--|--------------|-----|--------------|------|------------------|
| t_{PCK} | CK Clock Period | $1/f_{CK}$ | – | ∞ | ns | Figure 78 |
| t_{CH} | Clock High Time | 45% p_{CK} | – | 55% p_{CK} | | |
| t_{CL} | Clock Low Time | | – | | | |
| t_{CS} | CS# High Time (Read transactions) | 10 | – | – | | Figure 83 |
| | CS# High Time Between Transactions (Read transactions when Reset feature and Quad mode are both enabled and aborted transaction) | 20 | – | – | | |
| | CS# High Time (Program / Erase transactions) | 50 | – | – | | |
| t_{CSS} | CS# Active Setup Time relative to CK ($f_{CK} \leq 50\text{MHz}$ / $f_{CK} > 50\text{MHz}$) | 5/4 | – | – | | Figure 83 |
| t_{CSH0} | CS# Active Hold Time (relative to CK in Mode 0) | 4 | – | – | | |
| t_{SU} | Data Setup Time (all V_{CC}) | 2 | – | – | | Figure 84 |
| t_{HD} | Data Hold Time (all V_{CC}) | 1.2 | – | – | | |
| t_V | Clock Low to Output Valid (15pF Loading, 3.0V – 3.6V, 30 Ω Output Impedance, 105°C) (HL-T) | 2 | – | 6.5 | | |
| | Clock Low to Output Valid (15pF Loading) (HS-T) | 2 | – | 6 | | |
| | Clock Low to Output Valid (15pF Loading) (HL-T) | | – | 8 | | |
| t_{HO} | Output Hold Time | 1.5 | – | – | | |
| t_{DIS} | Output Disable Time (HS-T) | – | – | 8 | | |
| | Output Disable Time (HL-T) | – | – | 9 | | |
| | CS# Inactive to Output Disable Time (when Reset feature and Quad mode are both enabled) | – | – | 20 | | |
| $t_{IO_SKEW}^{[49]}$ | Data Skew (First Data Bit to Last Data Bit) | – | – | 0.6 | – | |

Power up / Power down timing

| | | | | | | |
|-----------------|--|----|---|-------------------------------------|-----------------|-----------|
| t_{PU} | $V_{CC}(\text{min})$ to Read operation (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | – | 550 / 600 450 / 500 450 / 500 | μs | Figure 66 |
| t_{PD} | $V_{CC}(\text{Low})$ time | 25 | – | – | | Figure 67 |
| $t_{VR}^{[50]}$ | V_{CC} Power Up ramp rate | 1 | – | – | $\mu\text{s/V}$ | – |
| t_{VF} | V_{CC} Power Down ramp rate | 30 | – | – | | |

Deep power down mode timing

| | | | | | | |
|---------------------|---|------|---|-------------------------------------|---------------|-----------|
| $t_{ENTDPD}^{[50]}$ | Time to Enter DPD mode | – | – | 3 | μs | Figure 65 |
| t_{EXTDPD} | Time to Exit DPD mode (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | – | 520 / 570 380 / 430 380 / 430 | | |
| t_{CSDPD} | Chip Select Pulse Width to Exit DPD | 0.02 | – | 3 | | |

Reset timing^[44, 45]

Notes

42. Output HI-Z is defined as the point where data is no longer driven.
43. Applicable across all operating temperature options.
44. If Reset# is asserted during the end of t_{PU} , the device will remain in the reset state and t_{RH} will determine when CS# may go Low.
45. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH} .
46. Typical program and erase times assume the following conditions: 25°C, $V_{CC} = 1.8\text{V}$ and 3.0V; checkerboard data pattern.
47. The programming time for any OTP programming transaction is the same as t_{pp} .
48. The programming time for the PRPPB_4_0 and PRPPB_C_0 transactions is the same as t_{pp} . The erase time for ERPPB_0_0 transaction is the same as t_{SE} .
49. Values are guaranteed by characterization and not 100% tested in production.
50. Guaranteed by design.
51. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Timing characteristics

Table 84 Timing characteristics^[43] (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|------------------|---|-------------------------------------|-----|--------------|------|------------------|
| t _{CSR} | CS# high before DQ3_RESET# Low | 50 | – | – | ns | Figure 60 |
| t _{RS} | Reset Setup - RESET# High before CS# Low | 50 | – | – | | |
| t _{RH} | Reset Pulse Hold - RESET# Low to CS# Low (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | 550 / 600 450 / 500 450 / 500 | – | – | μs | Figure 56 |
| t _{RP} | RESET# Pulse Width | 200 | – | – | ns | Figure 56 |
| t _{SR} | Internal Device Reset from Software Reset Transaction (256T / 512T / 01GT) | – | – | 90 / 83 / 83 | μs | – |

CS# signaling reset timing

| | | | | | | |
|--------------------|--|-----|---|-------------------------------------|----|-----------|
| t _{CSLW} | Chip Select Low | 500 | – | – | ns | Figure 63 |
| t _{CSHG} | Chip Select High | 500 | – | – | | |
| t _{RESET} | Internal device reset (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | – | 550 / 600 450 / 500 450 / 500 | μs | |
| t _{SUJ} | Data in Setup Time (w.r.t CS#) | 50 | – | – | ns | |
| t _{HDJ} | Data in Hold Time (w.r.t CS#) | 50 | – | – | | |

Embedded algorithm (erase, program, and data integrity check) performance^[46, 47, 48, 51]

| | | | | | | |
|------------------------|--|----|--------------|-------------------------------|------|---|
| t _W | Nonvolatile Register Write Time | – | 44 | 357.5 | ms | – |
| t _{PP} | 256B Page Programming (4KB Sector / 256KB Sector) | – | 430 / 480 | 2175 / 1700 | μs | |
| | 512B Page Programming (4KB Sector / 256KB Sector) | – | 680 / 570 | 2175 / 1700 | | |
| t _{SE} | Sector Erase Time (4KB physical sectors) | – | 42 | 335 | ms | |
| | Sector Erase Time (256KB Infineon® Endurance Flex architecture disabled) | – | 773 | 2677 | | |
| | Sector Erase Time (256KB Infineon® Endurance Flex architecture enabled) | – | 773 | 5869 | | |
| t _{BE} | Chip Erase Time (256Mb) | – | 101 | 348 | sec | |
| | Chip Erase Time (512Mb) | – | 201 | 696 | | |
| | Chip Erase Time (1Gb) | – | 398 | 1381 | | |
| t _{EES} | Evaluate Erase Status Time for 4KB physical sectors (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | 45 | 76 / 76 51 / 51 50 / 54 | μs | |
| | Evaluate Erase Status Time for 256KB physical sectors (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | 45 | | | |
| t _{DIC_SETUP} | Data Integrity Check Calculation Setup Time (256T / 512T / 01GT) | – | 50 / 17 / 17 | – | μs | |
| t _{DIC_RATES} | Data Integrity Check Calculation Rate (Calculation rate over a large (>1024-byte) block of data) | 55 | 65 | – | MBps | |

Notes

42. Output HI-Z is defined as the point where data is no longer driven.
43. Applicable across all operating temperature options.
44. If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go Low.
45. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.
46. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8V and 3.0V; checkerboard data pattern.
47. The programming time for any OTP programming transaction is the same as t_{pp}.
48. The programming time for the PRPPB_4_0 and PRPPB_C_0 transactions is the same as t_{pp}. The erase time for ERPPB_0_0 transaction is the same as t_{SE}.
49. Values are guaranteed by characterization and not 100% tested in production.
50. Guaranteed by design.
51. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Timing characteristics

Table 84 Timing characteristics^[43] (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|--|---|-------------|--------------------|-------------------------------|------|------------------|
| t _{SEC} | Sector Erase Count Time (HL256T / HS256T) (HL512T / HS512T) (HL01GT / HS01GT) | – | 55 | 87 / 87 63 / 63 63 / 70 | μs | - |
| t _{BEC1} | Blank Check single 256KB sector | – | 13 | 17 | ms | |
| t _{BEC2} | Blank Check single 4KB sector | – | 1 | 2 | | |
| t _{PASSWORD} | Password Comparison Time | 80 | 100 | 120 | μs | |
| Program, erase, or data integrity check suspend/resume timing | | | | | | |
| t _{PEDS} | Program/Erase/Data Integrity Check Suspend | – | – | 80 | μs | - |
| t _{PEDRS} | Program/Erase/Data Integrity Check Resume to next Program/Erase/Data Integrity Check Suspend (256T / 512T / 01GT) | 250 / – / – | 100 / 100 / 100 | – | | |

Notes

42. Output HI-Z is defined as the point where data is no longer driven.
43. Applicable across all operating temperature options.
44. If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go Low.
45. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.
46. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8V and 3.0V; checkerboard data pattern.
47. The programming time for any OTP programming transaction is the same as t_{PP}.
48. The programming time for the PRPPB_4_0 and PRPPB_C_0 transactions is the same as t_{pp}. The erase time for ERPPB_0_0 transaction is the same as t_{SE}.
49. Values are guaranteed by characterization and not 100% tested in production.
50. Guaranteed by design.
51. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

8.1 Timing waveforms

8.1.1 Key to timing waveform

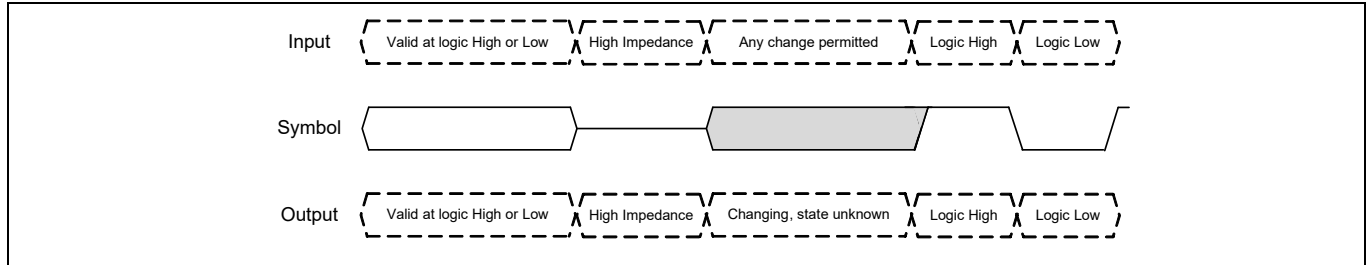


Figure 73 Waveform element meanings

8.1.2 Timing reference levels

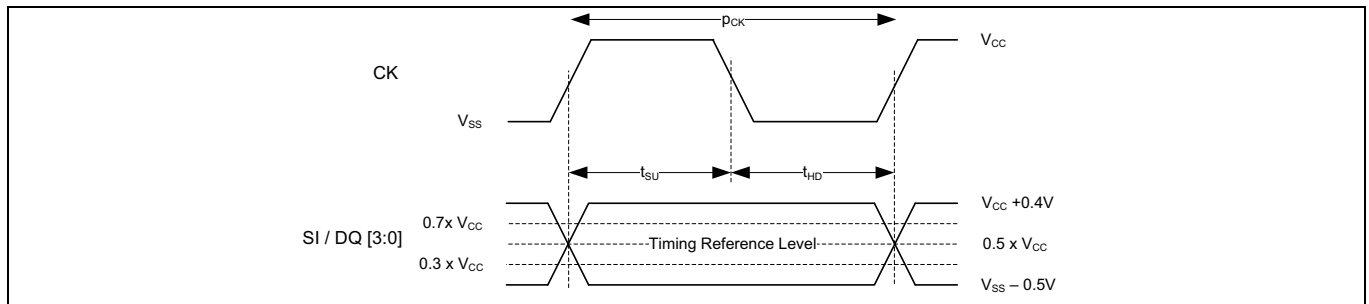


Figure 74 SDR input timing reference levels

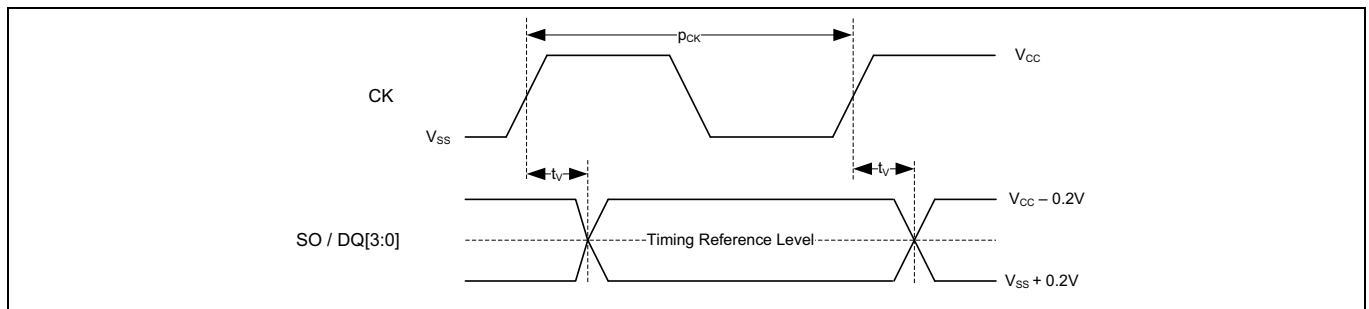


Figure 75 SDR output timing reference level

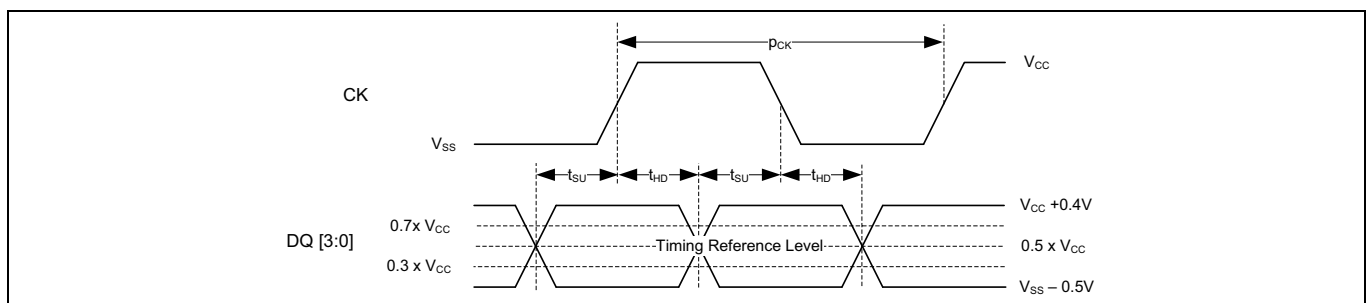


Figure 76 DDR input timing reference level

Timing characteristics

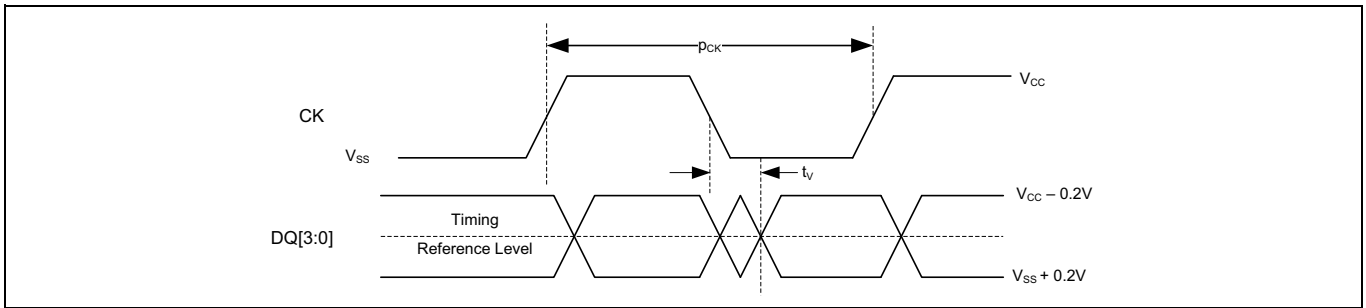


Figure 77 DDR output timing reference level

8.1.3 Clock Timing

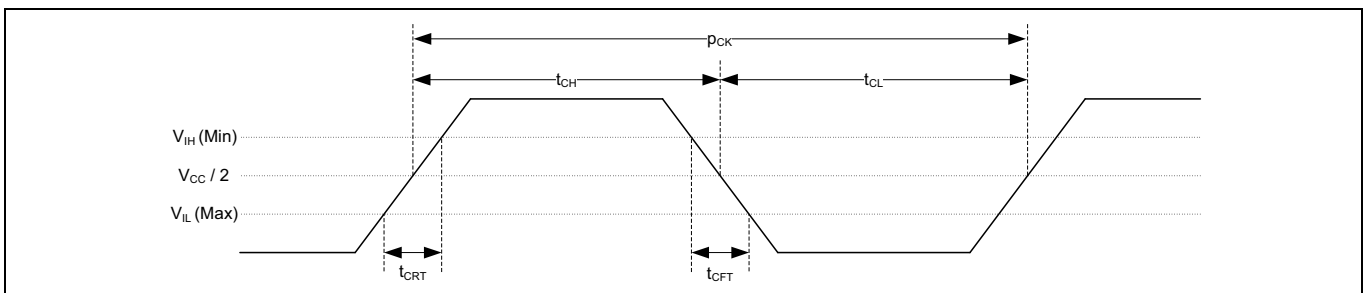


Figure 78 Clock timing

8.1.4 Input / output timing

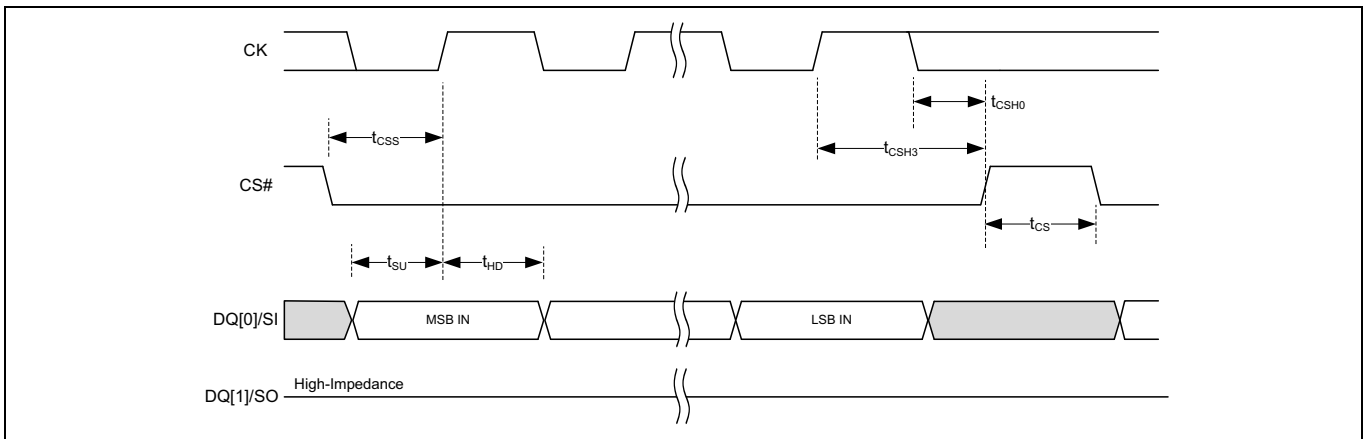


Figure 79 SPI input timing

Timing characteristics

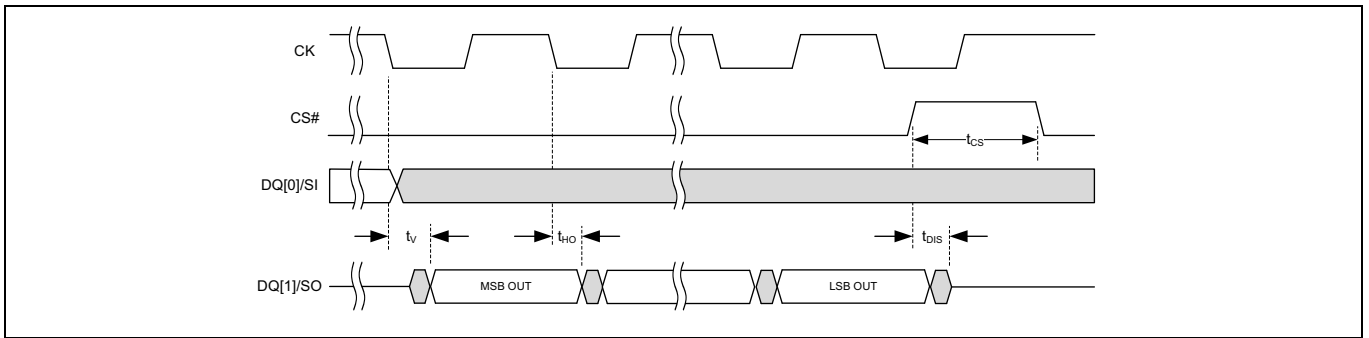


Figure 80 SPI output timing

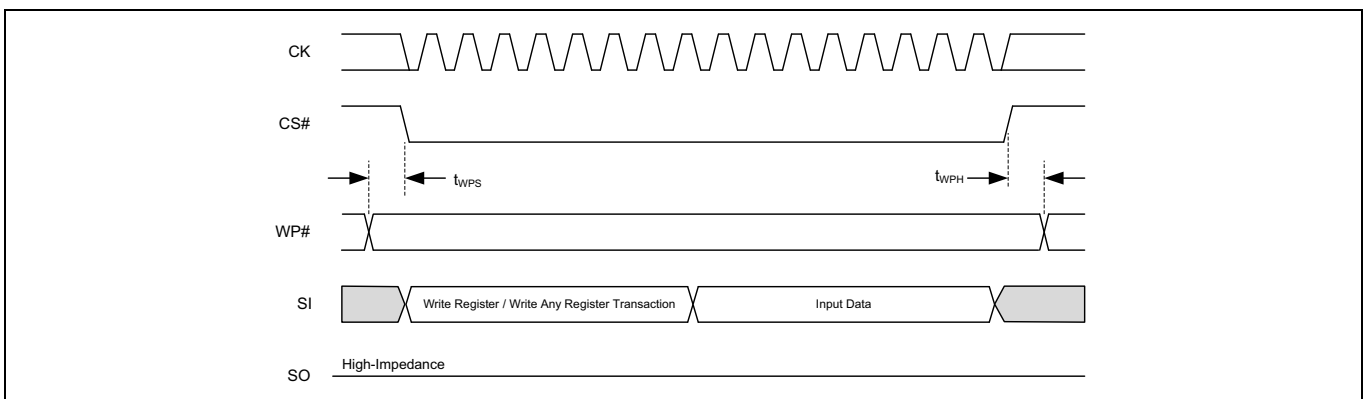


Figure 81 WP# input timing

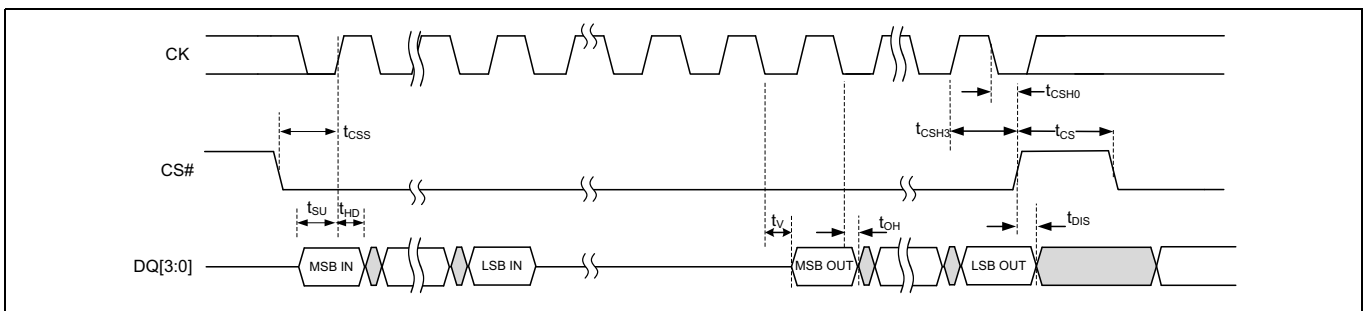


Figure 82 Quad and QPI SDR input and output timing

Timing characteristics

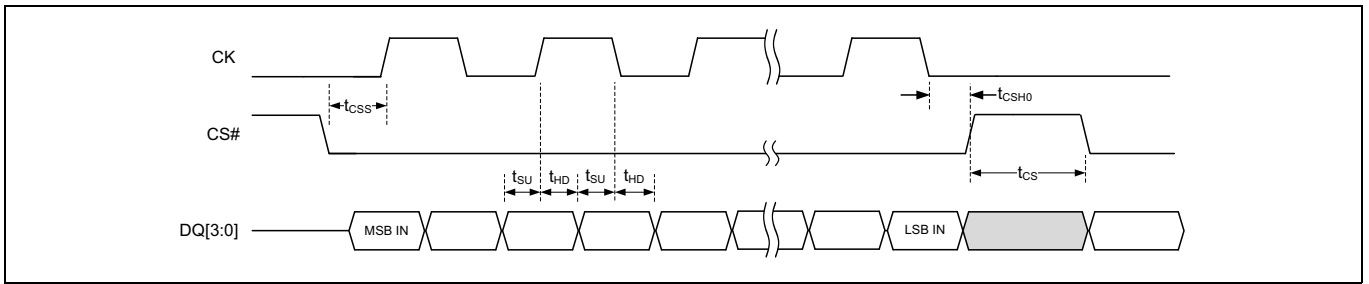


Figure 83 Quad and QPI DDR input timing

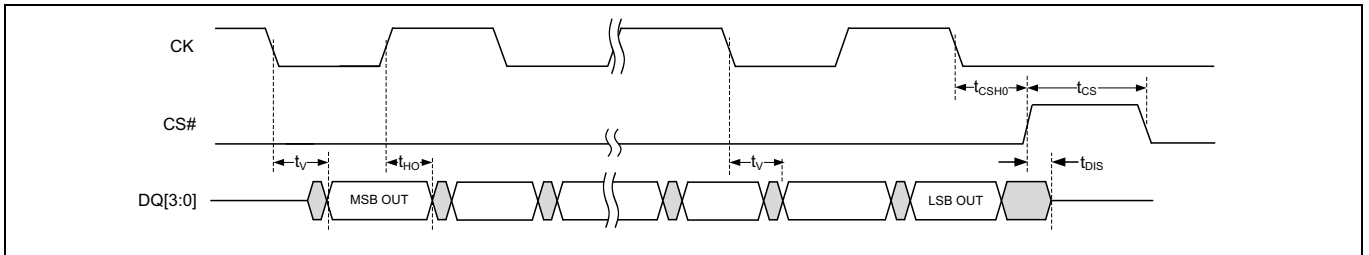


Figure 84 Quad and QPI DDR output timing

Device identification

9 Device identification

9.1 JEDEC SFDP Rev D

9.1.1 JEDEC SFDP Rev D header table

Table 85 JEDEC SFDP Rev D header table

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|----------------------|----------------------|--|
| 00h | SFDP Header | 53h | This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII "S" |
| 01h | | 46h | ASCII "F" |
| 02h | | 44h | ASCII "D" |
| 03h | | 50h | ASCII "P" |
| 04h | | 08h | SFDP Minor Revision (08h = JEDEC JESD216 Revision D) |
| 05h | | 01h | SFDP Major Revision (01h = JEDEC JESD216 Revision D) This is the original major revision. This major revision is compatible with all SFDP reading and parsing software. |
| 06h | | 03h | Number of Parameter Headers (zero based, 03h = 4 parameters) |
| 07h | | FFh | SFDP Access Protocol (Backward Compatible) |
| 08h | | 1st Parameter Header | 00h |
| 09h | 00h | | Parameter Minor Revision (00h = JEDEC JESD216 Revision D) |
| 0Ah | 01h | | Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision. |
| 0Bh | 14h | | Parameter Table Length (14h = 20 DWORDs are in the Parameter table) |
| 0Ch | 00h | | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0100h |
| 0Dh | 01h | | Parameter Table Pointer Byte 1 |
| 0Eh | 00h | | Parameter Table Pointer Byte 2 |
| 0Fh | FFh | | Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID) |
| 10h | 2nd Parameter Header | | 84h |
| 11h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 12h | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 13h | | 02h | Parameter Table Length (2h = 2 DWORDs are in the Parameter table) |
| 14h | | 50h | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) 4-Byte Address Instruction Table byte offset = 0150h address |
| 15h | | 01h | Parameter Table Pointer Byte 1 |
| 16h | | 00h | Parameter Table Pointer Byte 2 |
| 17h | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |
| 18h | | 3rd Parameter Header | 81h |
| 19h | 00h | | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 1Ah | 01h | | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 1Bh | 16h | | Parameter Table Length (16h = 22 DWORDs are in the Parameter table) |
| 1Ch | C8h | | Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) JEDEC Sector Map = 1C8h address |
| 1Dh | 01h | | Parameter Table Pointer Byte 1 |
| 1Eh | 00h | | Parameter Table Pointer Byte 2 |
| 1Fh | FFh | | Parameter ID MSB (FFh = JEDEC defined Parameter) |

Table 85 **JEDEC SFDP Rev D header table** *(continued)*

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|----------------------|------|--|
| 20h | 4th Parameter Header | 87h | Parameter ID LSB (87h = JEDEC Status, Control and Configuration Register Map) |
| 21h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 22h | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 23h | | 1Ch | Parameter Table Length (1Ch = 28 DWORDs are in the Parameter table) |
| 24h | | 58h | Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) JEDEC Status, Control and Configuration Register Map = 158h address |
| 25h | | 01h | Parameter Table Pointer Byte 1 |
| 26h | | 00h | Parameter Table Pointer Byte 2 |
| 27h | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |

9.1.2 JEDEC SFDP Rev D parameter table

For the SFDP data structure, there are three independent parameter tables. Two of the tables have a fixed length and one table has a variable structure and length depending on the device density Ordering Part Number (OPN). The Parameter table is presented as single table in [Table 86](#).

Device identification

Table 86 JEDEC SFDP Rev D parameter table

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|-------------------------------------|---|--|
| 100h | JEDEC Basic Flash Parameter DWORD-1 | E7h | Bits 7:5 = unused = 111b Bit 4 = 50h is Volatile Status Register write instruction and Status Register is default = 0b Bit 3 = Block Protect Bits are nonvolatile / volatile nonvolatile = 0b Bit 2 = Program Buffer > 64Bytes = 1b Bits 1:0 = Uniform 4KB erase is unavailable = 11b |
| 101h | | 20h | Bits 15:8 = 4KB erase opcode = 20h |
| 102h | | FAh | Bit 23 = Unused = 1b Bit 22 = Supports Quad Out (1-1-4) Read = Yes = 1b Bit 21 = Supports Quad I/O (1-4-4) Read = Yes = 1b Bit 20 = Supports Dual I/O (1-2-2) Read = Yes = 1b Bit 19 = Supports DDR = Yes = 1b Bit 18:17 = Number of Address Bytes = 3- or 4-Bytes = 01b Bit 16 = Supports Dual Out (1-1-2) Read = No = 0b |
| 103h | | FFh | Bits 31:24 = Unused = FFh |
| 104h | JEDEC Basic Flash Parameter DWORD-2 | FFh | Density in bits, zero based, 256Mb = 0FFFFFFFh Density in bits, zero based, 512Mb = 1FFFFFFFh Density in bits, zero based, 1Gb = 3FFFFFFFh |
| 105h | | FFh | |
| 106h | | FFh | |
| 107h | | 0Fh (256Mb) 1Fh (512Mb) 3Fh (1Gb) | |
| 108h | JEDEC Basic Flash Parameter DWORD-3 | 48h | Bits 7:5 = number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = number of Quad I/O Dummy cycles = 01000b (Initial Delivery State) |
| 109h | | EBh | Quad I/O instruction code |
| 10Ah | | 08h | Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b |
| 10Bh | | 6Bh | 1-1-4 Quad Out instruction code = 6Bh |
| 10Ch | JEDEC Basic Flash Parameter DWORD-4 | 00h | Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 00000b |
| 10Dh | | FFh | Dual Out instruction code |
| 10Eh | | 88h | Bits 23:21 = number of Dual I/O (1-2-2) Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 01000b (Initial Delivery State) |
| 10Fh | | BBh | Dual I/O instruction code |
| 110h | JEDEC Basic Flash Parameter DWORD-5 | FEh | Bits 7:5 RFU = 111b Bit 4 = QPI supported = Yes = 1b Bits 3:1 RFU = 111b Bit 0 = 2-2-2 not supported = 0b |
| 111h | | FFh | Bits 15:8 = RFU = FFh |
| 112h | | FFh | Bits 23:16 = RFU = FFh |
| 113h | | FFh | Bits 31:24 = RFU = FFh |
| 114h | JEDEC Basic Flash Parameter DWORD-6 | FFh | Bits 7:0 = RFU = FFh |
| 115h | | FFh | Bits 15:8 = RFU = FFh |
| 116h | | 00h | Bits 23:21 = number of 2-2-2 Mode cycles = 000b Bits 20:16 = number of 2-2-2 Dummy cycles = 00000b |
| 117h | | FFh | 2-2-2 instruction code |
| 118h | JEDEC Basic Flash Parameter DWORD-7 | FFh | Bits 7:0 = RFU = FFh |
| 119h | | FFh | Bits 15:8 = RFU = FFh |
| 11Ah | | 48h | Bits 23:21 = Number of QPI Mode cycles = 010b Bits 20:16 = Number of QPI Dummy cycles = 01000b |
| 11Bh | | EBh | QPI mode Quad I/O (4-4-4) instruction code |
| 11Ch | JEDEC Basic Flash Parameter DWORD-8 | 0Ch | Erase type 1 size 2^N Bytes = 2^12 Bytes = 4KB (Initial Delivery State) |
| 11Dh | | 20h | Erase type 1 instruction |
| 11Eh | | 00h | Erase type 2 size 2^N Bytes = Not Supported |
| 11Fh | | FFh | Erase type 2 instruction = Not Supported = FFh |
| 120h | | 00h | Erase type 3 size 2^N Bytes = Not Supported |
| 121h | JEDEC Basic Flash Parameter DWORD-9 | FFh | Erase type 3 instruction = Not Supported = FFh |
| 122h | | 12h | Erase type 4 size 2^N Bytes = 2^18 Bytes = 256KB |
| 123h | | D8h | Erase type 4 instruction = D8h |

Device identification

Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|--------------------------------------|--|--|
| 124h | JEDEC Basic Flash Parameter DWORD-10 | 23h | Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 29:25 = Erase type 4 Erase, Typical time count = 00101b (typ erase time = count +1 * units = 6 * 128 ms = 768 ms) |
| 125h | | FAh | |
| 126h | | FFh | Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 15:11 = Erase type 2 Erase, Typical time count = 11111b (RFU) |
| 127h | | 8Bh | Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16mS = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 00010b (typ erase time = count +1 * units = 3 * 16 ms = 48 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) - 1 = 0011b |
| 128h | JEDEC Basic Flash Parameter DWORD-11 | 82h | Bits 31 = Reserved = 1b Bits 30:29 = Chip Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b (256M, 512M, and 1G) |
| 129h | | E7h | Bits 28:24 = Chip Erase Typical time count = 00001b (256M), 00011b (512M), and 00110b (1G) |
| 12Ah | | FFh | Bits 23:19 = Byte Program Typical Time, additional byte = 11111b Bits 18:14 = Byte Program Typical Time, first byte = 11111b |
| 12Bh | | E1h for 256M E3h for 512M E6h for 1G | Bits 13 = Page Program Typical Time unit (0: 8 μs, 1: 64 μs) = 64 μs = 1b Bits 12:8 = Page Program Typical Time Count = 00111 (typ Program time = count +1 * units = 8 * 64 μs = 512 μs) Bits 7:4 = Page Size (256B) = 2^N bytes = 1000h Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] - 1 = 0010b |
| 12Ch | JEDEC Basic Flash Parameter DWORD-12 | ECh | Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1μs, 10b: 8μs, 11b: 64μs) = 8 μs = 10b |
| 12Dh | | 23h | Bits 28:24 = Suspend in-progress erase max latency count = 01001b, max erase suspend latency = count +1 * units = 10 * 8 μs = 80 μs |
| 12Eh | | 19h | Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count +1 * 64 μs = 2 * 64 μs = 128 μs Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) = 8 μs = 10b Bits 17:13 = Suspend in-progress program max latency count = 01001b, max program suspend latency = count +1 * units = 10 * 8 μs = 80 μs Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count +1 * 64 μs = 2 * 64 μs = 128 μs Bit 8 = Reserved = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b |
| 12Fh | | 49h | |
| 130h | | JEDEC Basic Flash Parameter DWORD-13 | 8Ah |
| 131h | 85h | | Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah |
| 132h | 7Ah | | Bits 15:8 = Program Suspend Instruction = 85h Bits 7:0 = Program Resume Instruction = 8Ah |
| 133h | 75h | | |
| 134h | JEDEC Basic Flash Parameter DWORD-14 | F7h | Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). Bits 1:0 = RFU = 11b |
| 135h | | 66h | Bit 31 = DPD Supported = supported = 0 Bits 30:23 = Enter DPD Instruction = B9h |
| 136h | | 80h | Bits 22:15 = Exit DPD Instruction not supported = 00h Bits 14:13 = Exit DPD to next operation delay units = (00b: 128ns, 01b: 1μs, 10b: 8μs, 11b: 64μs) = 64 μs = 11b Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count+1) * units = (6 + 1) * 64 μs = 448 μs |
| 137h | | 5Ch | |

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Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|--------------------------------------|------|---|
| 138h | JEDEC Basic Flash Parameter DWORD-15 | 8Ch | Bits 31:24 = RFU = FFh Bit 23 = HOLD or RESET Disable = Supported = 1 Bits 22:20 = Quad Enable Requirements = 101b = 101b: QE is bit 1 of the Status Register-2. Status Register-1 is read using Read Status instruction 05h. Status Register-2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 = 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0] = Axh + 1xxb: RFU = 1101b Bits 15:10 = 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_x1xxb: RFU + xx_1xxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxb: Mode Bit[7:0] != Axh + 1x_x1xxb: RFU = 11_0101b Bit 9 = 0-4-4 mode supported = 1b Bits 8:4 = 4-4-4 mode enable sequences = x_xxx1b: Issue instruction 38h. + x_1xxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 01000 Bits 3:0 = 4-4-4 mode disable sequences = xxx1b: Issue FFh instruction + xx0xb: Issue F5h instruction + x1xxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. + 1xxb: Issue the Soft Reset 66/99 sequence = 1100 |
| 139h | | D6h | |
| 13Ah | | DDh | |
| 13Bh | | FFh | |
| 13Ch | JEDEC Basic Flash Parameter DWORD-16 | F9h | Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b: issue instruction B7h (preceding write enable not required) + xx1x_xxxb: Supports dedicated 4-Byte address instruction set. Refer to the vendor datasheet for the instruction set definition. + 1xxx_xxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing = xx_xx1x_xxxb: Hardware reset + xx_x1xx_xxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxb: Power cycle + x1_xxxx_xxxb: Reserved + 1x_xxxx_xxxb: Reserved = 11_1110_0000b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxb: Issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. + 1x_xxxb: Exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 111000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Nonvolatile Register and Write Enable Instruction for Status Register 1 = xxx_xxx1b: Nonvolatile Status Register 1, powers-up to last written value, use instruction 06h to enable write. + xxx_1xxb: Nonvolatile/Volatile Status Register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to nonvolatile status register. Volatile status register may be activated after power-up to override the nonvolatile status register, use instruction 50h to enable write and activate the volatile status register. + xx1_xxxb: Status Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxb: Reserved + 1xx_xxxb: Reserved = 1111001b |
| 13Dh | | 38h | |
| 13Eh | | F8h | |
| 13Fh | | A1h | |
| 140h | JEDEC Basic Flash Parameter DWORD-17 | 00h | Not Supported |
| 141h | | | |
| 142h | | | |
| 143h | | | |
| 144h | JEDEC Basic Flash Parameter DWORD-18 | 00h | Bits 31: 24 = 00h Bit 23 = 1b = JEDEC SPI Protocol Reset implemented as described in JESD252 Bits 22:18 = 01111b Bits 17:0 = 000h |
| 145h | | 00h | |
| 146h | | BCh | |
| 147h | | 00h | |
| 148h | JEDEC Basic Flash Parameter DWORD-19 | 00h | Not Supported |
| 149h | | | |
| 14Ah | | | |
| 14Bh | | | |

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Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|--|------|---|
| 14Ch | JEDEC Basic Flash Parameter DWORD-20 | F7h | Bits 31:16 = Not Supported = 1111_1111_1111_1111b Bit 15:12 = 1111b = 4S-4D-4D Data Strobe is not supported Bit 11:8 = 0101b = 100MHz 4S-4D-4D Bit 7:4 = 1111b = 4S-4S-4S Data Strobe is not supported Bit 0:3 = 0111b = 166MHz 4S-4S-4S |
| 14Dh | | F5h | |
| 14Eh | | FFh | |
| 14Fh | | FFh | |
| 150h | JEDEC 4-Byte Address Instructions Parameter DWORD-1 | 7Bh | Supported = 1, Not Supported = 0 Bits 31:25 = Reserved = 1111_111b Bit 24 = Support for (1-8-8) Page Program Command, Instruction = 8Eh = 0b Bit 23 = Support for (1-1-8) Page Program Command, Instruction = 84h = 0b Bit 22 = Support for (1-8-8) DTR_READ Command, Instruction = FDh = 0b Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7Ch = 0b Bit 19 = Support for nonvolatile individual sector lock write command, Instruction = E3h = 1b Bit 18 = Support for nonvolatile individual sector lock read command, Instruction = E2h = 1b Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1b Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1b Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 1b Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b Bit 12 = Support for Erase Command – Type 4 = 1b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 0b Bit 9 = Support for Erase Command – Type 1 = 1b Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh = 0b Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 0b Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1b Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 1b Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 1b Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 1b Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0b Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 1b Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b |
| 151h | | 92h | |
| 152h | | 0Fh | |
| 153h | | FEh | |
| 154h | JEDEC 4-Byte Address Instructions Parameter DWORD-2 | 21h | Bits 31:24 = D8h / DCh = Instruction fo Erase Type 4 Bits 23:16 = Instruction for Erase Type 3: RFU Bits 15:8 = Instruction for Erase Type 2: RFU Bits 7:0 = 20h / 21h = Instruction for Erase Type 1 |
| 155h | | FFh | |
| 156h | | FFh | |
| 157h | | DCh | |
| 158h | Status, Control and Configuration Register Map DWORD-1 | 00h | Bits 31:0 = Address offset for volatile registers = 00800000h |
| 159h | | 00h | |
| 15Ah | | 80h | |
| 15Bh | | 00h | |
| 15Ch | Status, Control and Configuration Register Map DWORD-2 | 00h | Bits 31:0 = Address offset for nonvolatile registers = 00000000h |
| 15Dh | | 00h | |
| 15Eh | | 00h | |
| 15Fh | | 00h | |
| 160h | Status, Control and Configuration Register Map DWORD-3 | C0h | Bit 31 = Generic Addressable Read Status/Control register command supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands = 3 byte (default) = 10b Bit 27:26 = Use the number of bits as defined in bits 3:0 in this DWORD = 10b Bit 25:22 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b Bit 21:18 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 0000b Bit 17:14 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode note supported = 1111b Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode note supported = 1111b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode note supported = 1111b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b |
| 161h | | FFh | |
| 162h | | C3h | |
| 163h | | EBh | |

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Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|--|------|---|
| 164h | Status, Control and Configuration Register Map DWORD-4 | C8h | Bit 31 = Generic Addressable Read Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for nonvolatile registers = 3 byte (default) = 10b Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for nonvolatile registers in (1S-1S-1S) mode not supported = 10b Bit 25:22 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b Bit 21:18 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 1000b Bit 17:14 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode not supported = 1111b Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode not supported = 1111b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode not supported = 1111b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for nonvolatile registers in (1S-1S-1S) mode = 1000b |
| 165h | | FFh | |
| 166h | | E3h | |
| 167h | | EBh | |
| 168h | Status, Control and Configuration Register Map DWORD-5 | 00h | Bits 7:0 = Command used for write access = read only = 00h |
| 169h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 16Ah | | 00h | Bits 23:16 = Address of register where WIP is located = 00h (status reg -1 volatile) |
| 16Bh | | 90h | Bit 31 = Write In Progress (WIP) bit is supported = 1b Bit 30 = Write In Progress polarity, WIP = 1 means write is in progress = 0b Bits 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b |
| 16Ch | Status, Control and Configuration Register Map DWORD-6 | 06h | Bits 7:0 = Command used for write access = 06h |
| 16Dh | | 05h | Bits 15:8 = Command used for read access = 05h |
| 16Eh | | 00h | Bits 23:16 = Address of register where WEL is located = 00h (status reg -1 volatile) |
| 16Fh | | A1h | Bit 31 = Write Enable (WEL) bit is supported = 1b Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b Bits 29 = Write command is a direct command to set WEL bit = 1b Bits 28 = Bit is accessed by direct commands to set WEL bit = 0b Bit 27 = Local address for WEL bit is found in last byte of the address = 0b Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b |
| 170h | Status, Control and Configuration Register Map DWORD-7 | 00h | Bits 7:0 = Command used for write access = read only = 00h = Read Only |
| 171h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 172h | | 00h | Bits 23:16 = Address of register where Erase Error is located = 00h |
| 173h | | 96h | Bit 31 = Program Error bit supported = 1b Bit 30 = Positive polarity (Program Error = 0 means no error, Program Error = 1 means last Program operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = 0b Bits 26:24 = Bit location of Program Error bit in register = bit [6] = 110b |
| 174h | Status, Control and Configuration Register Map DWORD-8 | 00h | Bits 7:0 = Command used for write access = read only = 00h = Read Only |
| 175h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 176h | | 00h | Bits 23:16 = Address of register where Erase Error is located = 00h |
| 177h | | 95h | Bit 31 = Erase Error bit supported = 1b Bit 30 = Positive polarity Erase Error = 0 means no error, Erase Error = 1 means last erase operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Reserved = 0b Bits 26:24 = Bit location of erase Error bit in register = bit [5] = 101b |
| 178h | Status, Control and Configuration Register Map DWORD-9 | 71h | Bits 7:0 = Command used for write access = 71h |
| 179h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 17Ah | | 03h | Address of register where wait states bits are located = 800003h (Configuration Reg - 2 volatile) |
| 17Bh | | D0h | Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b |

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Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|---|------|--|
| 17Ch | Status, Control and Configuration Register Map DWORD-10 | 71h | Bits 7:0 = Command used for write access = 71h |
| 17Dh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 17Eh | | 03h | Address of register where wait states bits are located = 03h (Configuration Reg - 2 Nonvolatile) |
| 17Fh | | D0h | Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b |
| 180h | Status, Control and Configuration Register Map DWORD-11 | 00h | Bit 31 = 30 dummy cycles supported = 0b Bit 30:26 = Bit pattern used to set 30 dummy cycles = 00000b Bit 25 = 28 dummy cycles supported = 0b Bit 24:20 = Bit pattern used to set 28 dummy cycles = 00000b Bit 19 = 26 dummy cycles supported = 0b Bit 18:14 = Bit pattern used to set 26 dummy cycles = 00000b Bit 13 = 24 dummy cycles supported = 0b Bit 12:8 = Bit pattern used to set 24 dummy cycles = 00000b Bit 7 = 22 dummy cycles supported = 0b Bit 6:2 = Bit pattern used to set 22 dummy cycles = 00000b Bits 1:0 = Reserved = 00b |
| 181h | | 00h | |
| 182h | | 00h | |
| 183h | | 00h | |
| 184h | Status, Control and Configuration Register Map DWORD-12 | B0h | Bit 31 = 20 dummy cycles supported = 0b Bit 30:26 = Bit pattern used to set 20 dummy cycles = 00000b Bit 25 = 18 dummy cycles supported = 0b Bit 24:20 = Bit pattern used to set 18 dummy cycles = 00000b Bit 19 = 16 dummy cycles supported = 0b Bit 18:14 = Bit pattern used to set 16 dummy cycles = 00000b Bit 13 = 14 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 14 dummy cycles = 01110b Bit 7 = 12 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 12 dummy cycles = 01100b Bits 1:0 = Reserved = 00b |
| 185h | | 2Eh | |
| 186h | | 00h | |
| 187h | | 00h | |
| 188h | Status, Control and Configuration Register Map DWORD-13 | 88h | Bit 31 = 10 dummy cycles supported = 1b Bit 30:26 = Bit pattern used to set 10 dummy cycles = 01010b Bit 25 = 8 dummy cycles supported = 1b Bit 24:20 = Bit pattern used to set 8 dummy cycles = 01000b Bit 19 = 6 dummy cycles supported = 1b Bit 18:14 = Bit pattern used to set 6 dummy cycles = 00110b Bit 13 = 4 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 4 dummy cycles = 00100b Bit 7 = 2 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 2 dummy cycles = 00010b Bits 1:0 = Reserved = 00b |
| 189h | | A4h | |
| 18Ah | | 89h | |
| 18Bh | | AAh | |
| 18Ch | Status, Control and Configuration Register Map DWORD-14 | 71h | Bits 7:0 = Command used for write access = 71h |
| 18Dh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 18Eh | | 03h | Address of register where wait states bits are located = 800003h (Configuration Reg - 2 Volatile) |
| 18Fh | | 96h | Bit 31 = QPI Mode Enable Volatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [6] = 110b |
| 190h | Status, Control and Configuration Register Map DWORD-15 | 71h | Bits 7:0 = Command used for write access = 71h |
| 191h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 192h | | 03h | Address of register where wait states bits are located = 03h (Configuration Reg - 2 Nonvolatile) |
| 193h | | 96h | Bit 31 = QPI Mode Enable Nonvolatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [6] = 110b |
| 194h | Status, Control and Configuration Register Map DWORD-16 | 00h | Not Supported |
| 195h | | 00h | |
| 196h | | 00h | |
| 197h | | 00h | |
| 198h | Status, Control and Configuration Register Map DWORD-17 | 00h | |
| 199h | | 00h | |
| 19Ah | | 00h | |
| 19Bh | | 00h | |
| 19Ch | Status, Control and Configuration Register Map DWORD-18 | 00h | |
| 19Dh | | 00h | |
| 19Eh | | 00h | |
| 19Fh | | 00h | |

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Table 86 JEDEC SFDP Rev D parameter table (continued)

| SFDP byte address | SFDP DWORD name | Data | Description |
|-------------------|---|------|--|
| 1A0h | Status, Control and Configuration Register Map DWORD-19 | 00h | Not Supported |
| 1A1h | | 00h | |
| 1A2h | | 00h | |
| 1A3h | | 00h | |
| 1A4h | Status, Control and Configuration Register Map DWORD-20 | 00h | |
| 1A5h | | 00h | |
| 1A6h | | 00h | |
| 1A7h | | 00h | |
| 1A8h | Status, Control and Configuration Register Map DWORD-21 | 00h | |
| 1A9h | | 00h | |
| 1AAh | | 00h | |
| 1ABh | | 00h | |
| 1ACh | Status, Control and Configuration Register Map DWORD-22 | 00h | |
| 1ADh | | 00h | |
| 1AEh | | 00h | |
| 1AFh | | 00h | |
| 1B0h | Status, Control and Configuration Register Map DWORD-23 | 00h | |
| 1B1h | | 00h | |
| 1B2h | | 00h | |
| 1B3h | | 00h | |
| 1B4h | Status, Control and Configuration Register Map DWORD-24 | 00h | |
| 1B5h | | 00h | |
| 1B6h | | 00h | |
| 1B7h | | 00h | |
| 1B8h | Status, Control and Configuration Register Map DWORD-25 | 00h | |
| 1B9h | | 00h | |
| 1BAh | | 00h | |
| 1BBh | | 00h | |
| 1BCh | Status, Control and Configuration Register Map DWORD-26 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1BDh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1BEh | | 05h | Address of register where Output Driver Strength volatile bits are located = 800005h (Configuration Reg - 4 Volatile) |
| 1BFh | | D5h | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b |
| 1C0h | Status, Control and Configuration Register Map DWORD-27 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1C1h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1C2h | | 05h | Address of register where Output Driver Strength volatile bits are located = 05h (Configuration Reg - 4 Nonvolatile) |
| 1C3h | | D5h | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b |
| 1C4h | Status, Control and Configuration Register Map DWORD-28 | 00h | Bits 7:0 = Reserved = 00h |
| 1C5h | | 00h | Bits 15:8 = Reserved = 00h |
| 1C6h | | A0h | Bits 31:29 = Bit pattern to support Driver type 0 = 45 Ohm = 000b Bits 28:26 = Bit pattern to support Driver type 1 = 30 Ohm = 101b Bits 25:23 = Bit pattern to support Driver type 2 = 60 Ohm = 011b Bits 22:20 = Bit pattern to support Driver type 3 = 90 Ohm = 010b Bits 19:17 = Bit pattern to support Driver type 4 = Not supported = 000b Bit 16 = Reserved = 0b |
| 1C7h | | 15h | |

Sector Map Parameter Table Notes

Table 87 provides a means to identify how the device address map is configured and provides a sector map for each supported configuration. This is done by defining a sequence of commands to read out the relevant configuration register bits that affect the selection of an address map. When more than one configuration bit must be read, all the bits are concatenated into an index value that is used to select the current address map.

To identify the sector map configuration in device the following configuration bits are read in the following MSb to LSB order to form the configuration map index value:

- CFR3V[3] - 0 = Hybrid Architecture, 1 = Uniform Architecture
- CFR1V[6] - 0 = 4KB parameter grouped together, 1 = 4KB sectors split between bottom and top
- CFR1V[2] - 0 = 4KB parameter sectors at bottom, 1 = 4KB sectors at top
- The value of some configuration bits may make other configuration bit values not relevant (don't care), hence not all possible combinations of the index value define valid address maps. Only selected configuration bit combinations are supported by the SFDP Sector Map Parameter Table (see **Table 88**). Other combinations must not be used in configuring the sector address map when using this SFDP parameter table to determine the sector map. The following index value combinations are supported.

Table 87 Sector map parameter

| CFR3V[3] | CFR1V[6] | CFR1V[2] | Index value | Description |
|----------|----------|----------|-------------|---|
| 0 | 0 | 0 | 00h | 4KB sectors at bottom with remainder 256KB sectors |
| 0 | 0 | 1 | 01h | 4KB sectors at top with remainder 256KB sectors |
| 0 | 1 | 0 | 02h | 4KB sectors split between top and bottom with remainder 256KB sectors |
| 1 | 0 | 0 | 04h | Uniform 256KB sectors |

Device identification

Table 88 JEDEC SFDP rev D, sector map parameter table

| SFDP | SFDP DWORD name | Data | Description |
|------|---|------|---|
| 1C8h | JEDEC Sector Map Parameter DWORD-1 Config. Detect-1 | FCh | Config. Detect -1 Uniform 256KB Sectors or Hybrid Sectors Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for UNHYSA value 0 = Hybrid map with 4KB parameter sectors 1 = Uniform map Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0 |
| 1C9h | | 65h | |
| 1CAh | | FFh | |
| 1CBh | | 08h | |
| 1CCh | JEDEC Sector Map Parameter DWORD-2 Config. Detect-1 | 04h | Bits 31:0 = Address Value Configuration Register 3 (bit 3) = 00800004h |
| 1CDh | | 00h | |
| 1CEh | | 80h | |
| 1CFh | | 00h | |
| 1D0h | JEDEC Sector Map Parameter DWORD-3 Config. Detect-2 | FCh | Config. Detect-2 4KB Hybrid Sectors Split between Top and Bottom Bits 31:24 = Read data mask = 0100_0000b: Select bit 6 of the data byte for SP4KBS value 0 = 4KB parameter sectors are grouped together 1 = 4KB parameter sectors are split between High and Low Addresses Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0 |
| 1D1h | | 65h | |
| 1D2h | | FFh | |
| 1D3h | | 40h | |
| 1D4h | JEDEC Sector Map Parameter DWORD-4 Config. Detect-2 | 02h | Bits 31:0 = Address Value Configuration Register 1 (bit 6) = 00800002h |
| 1D5h | | 00h | |
| 1D6h | | 80h | |
| 1D7h | | 00h | |
| 1D8h | JEDEC Sector Map Parameter DWORD-5 Config. Detect-3 | FDh | Config Detect-3 4KB Hybrid Sectors on Top or Bottom Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TB4KBS value 0 = 4KB parameter sectors at bottom 1 = 4KB parameter sectors at top Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = End of command descriptor = 1 |
| 1D9h | | 65h | |
| 1DAh | | FFh | |
| 1DBh | | 04h | |
| 1DCh | JEDEC Sector Map Parameter DWORD-6 Config. Detect-3 | 02h | Bits 31:0 = Address Value Configuration Register 1 (bit 2) = 00800002h |
| 1DDh | | 00h | |
| 1DEh | | 80h | |
| 1DFh | | 00h | |
| 1E0h | JEDEC Sector Map Parameter DWORD-7 Config-0 Header | FEh | Configuration Index 00h 4KB sectors at bottom with remainder 256KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions Bits 15:8 = Configuration ID = 00h, 4KB sectors bottom with remainder 256KB Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0 |
| 1E1h | | 00h | |
| 1E2h | | 02h | |
| 1E3h | | FFh | |
| 1E4h | JEDEC Sector Map Parameter DWORD-8 Config-0 Region-0 | F1h | Region 0 of 4KB sectors Bits 31:8 = Region size (thirty-two 4KB) = 0001FFh: Region size as count-1 of 256 Byte units = 32 x 4KB sectors = 128KB Count = 128KB/256 = 512, value = count -1 = 512-1 = 511 = 1FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256KB erase and is not supported in the 4KB sector Bit 2 = Erase Type 3 support = 0b ---Is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4KB erase and is supported in the 4KB sector region |
| 1E5h | | FFh | |
| 1E6h | | 01h | |
| 1E7h | | 00h | |

Device identification

Table 88 JEDEC SFDP rev D, sector map parameter table (continued)

| SFDP | SFDP DWORD name | Data | Description |
|------|---|---|--|
| 1E8h | JEDEC Sector Map Parameter DWORD-9 Config-0 Region-1 | F8h | Region 1 of 128KB sector |
| 1E9h | | FFh | Bits 31:8 = Region size = 0001FFh: Region size as count-1 of 256 Byte units = 1 x 128KB sectors = 128KB Count = 128KB/256 = 512, value = count -1 = 512-1 = 511 = 1FFh |
| 1EAh | | 01h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 128KB sector region |
| 1EBh | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 4KB sector region |
| 1ECh | JEDEC Sector Map Parameter DWORD-10 Config-0 Region-2 | F8h | Region 2 Uniform 256KB sectors |
| 1EDh | | FFh | Bits 31:8 = 256Mb device Region size = 01FBFFh: Region size as count-1 of 128 Byte units = 127 x 256KB sectors = 32,512KB Count = 32,512KB/256 = 130,048 value = count -1 = 130,048-1= 130047=01FBFFh |
| 1EEh | | FBh | Bits 31:8 = 512Mb device Region size = 03FBFFh: Region size as count-1 of 256 Byte units = 255 x 256KB sectors = 65,280KB Count = 65,280KB/256 = 261,120 value = count -1 = 261,120-1= 261119 =03FBFFh |
| 1EFh | | 01h (256Mb) 03h (512Mb) 07h (1Gb) | Bits 31:8 = 1Gb device Region size = 07FBFFh: Region size as count-1 of 256 Byte units = 511 x 256KB sectors = 130,816KB Count = 130,816KB/256 = 523,364, value = count -1 = 523,364-1 = 523263 = 07FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 256KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 256KB sector region |
| 1F0h | JEDEC Sector Map Parameter DWORD-11 Config-3 Header | FEh | Configuration Index 01h 4KB sectors at Top with remainder 256KB |
| 1F1h | | 01h | Bits 31:24 = RFU = FFh |
| 1F2h | | 02h | Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions Bits 15:8 = Configuration ID = 01h: 4KB sectors at top with remainder 256KB sectors |
| 1F3h | | FFh | Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0 |
| 1F4h | JEDEC Sector Map Parameter DWORD-12 Config-3 Region-0 | F8h | Region 0 Uniform 256KB sectors |
| 1F5h | | FFh | Bits 31:8 = 256Mb device Region size = 01FBFFh: Region size as count-1 of 128 Byte units = 127 x 256KB sectors = 32,512KB Count = 32,512KB/256 = 130,048 value = count -1 = 130,048-1= 130047=01FBFFh |
| 1F6h | | FBh | Bits 31:8 = 512Mb device Region size = 03FBFFh: Region size as count-1 of 256 Byte units = 255 x 256KB sectors = 65,280KB Count = 65,280KB/256 = 261,120 value = count -1 = 261,120-1= 261119 =03FBFFh |
| 1F7h | | 01h (256Mb) 03h (512Mb) 07h (1Gb) | Bits 31:8 = 1Gb device Region size = 07FBFFh: Region size as count-1 of 256 Byte units = 511 x 256KB sectors = 130,816KB Count = 130,816KB/256 = 523,264, value = count -1 = 523,364-1 = 523263 = 07FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 256KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 256KB sector region |
| 1F8h | JEDEC Sector Map Parameter DWORD-13 Config-3 Region-1 | F8h | Region 1 of 128KB sector |
| 1F9h | | FFh | Bits 31:8 = Region size = 0001FFh: Region size as count-1 of 256 Byte units = 1 x 128KB sectors = 128KB Count = 128KB/256 = 512, value = count -1 = 512-1 = 511 = 1FFh |
| 1FAh | | 01h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 128KB sector region |
| 1FBh | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 4KB sector region |
| 1FCh | JEDEC Sector Map Parameter DWORD-14 Config-3 Region-2 | F1h | Region 2 of 4KB sectors |
| 1FDh | | FFh | Bits 31:8 = Region size (thirty-two 4KB) = 0001FFh: Region size as count-1 of 256 Byte units = 32 x 4KB sectors = 128KB Count = 128KB/256 = 512, value = count -1 = 512-1 = 511 = 1FFh |
| 1FEh | | 01h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256KB erase and is not supported in the 4KB sector region |
| 1FFh | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4KB erase and is supported in the 4KB sector region |

Device identification

Table 88 JEDEC SFDP rev D, sector map parameter table (continued)

| SFDP | SFDP DWORD name | Data | Description |
|------|---|---|---|
| 200h | JEDEC Sector Map Parameter DWORD-15 Config-1 Header | FEh | Configuration Index 02h 4KB sectors split between Bottom and Top with remainder 256KB |
| 201h | | 02h | Bits 31:24 = RFU = FFh |
| 202h | | 04h | Bits 23:16 = Region count (DWORDs -1) = 04h: Five regions |
| 203h | | FFh | Bits 15:8 = Configuration ID = 02h: 4KB sectors split between bottom and top with remainder 256KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0 |
| 204h | JEDEC Sector Map Parameter DWORD-16 Config-1 Region-0 | F1h | Region 0 of 4KB sectors |
| 205h | | FFh | Bits 31:8 = Region size (16 x 4KB) = 0000FFh: Region size as count-1 of 256 Byte units = 16 x 4KB sectors = 64KB Count = 64KB/256 = 256, value = count -1 = 256-1 = 255 = FFh |
| 206h | | 00h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256KB erase and is not supported in the 4KB sector region |
| 207h | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4KB erase and is supported in the 4KB sector region |
| 208h | JEDEC Sector Map Parameter DWORD-17 Config-1 Region-1 | F8h | Region 1 of 192KB sector |
| 209h | | FFh | Bits 31:8 = Region size = 0002FFh: Region size as count-1 of 256 Byte units = 1 x 192KB sectors = 192KB Count = 192KB/256 = 768, value = count -1 = 768-1 = 767 = 2FFh |
| 20Ah | | 02h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 192KB sector region |
| 20Bh | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 4KB sector region |
| 20Ch | JEDEC Sector Map Parameter DWORD-18 Config-1 Region-2 | F8h | Region 2 Uniform 256KB sectors |
| 20Dh | | FFh | Bits 31:8 = 256Mb device Region size = 01F7FFh: Region size as count-1 of 128 Byte units = 126 x 256KB sectors = 32,256KB Count = 32,256KB/256 = 129,024 value = count -1 = 129,024-1= 129,023=01F7FFh |
| 20Eh | | F7h | Bits 31:8 = 512Mb device Region size = 03F7FFh: Region size as count-1 of 256 Byte units = 254 x 256KB sectors = 65,024KB Count = 65,024KB/256 = 260,096 value = count -1 = 260,096-1 = 260,095 = 03F7FFh |
| 20Fh | | 01h (256Mb) 03h (512Mb) 07h (1Gb) | Bits 31:8 = 1Gb device Region size = 07F7FFh: Region size as count-1 of 256 Byte units = 510 x 256KB sectors = 130,560KB Count = 130,560KB/256 = 522,240, value = count -1 = 522,240-1 = 522,239 = 7F7FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 256KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 256KB sector region |
| 210h | JEDEC Sector Map Parameter DWORD-19 Config-1 Region-3 | F8h | Region 3 of 192KB sector |
| 211h | | FFh | Bits 31:8 = Region size = 000FFh: Region size as count-1 of 256 Byte units = 1 x 192KB sectors = 192KB Count = 192KB/256 = 768, value = count -1 = 768-1 = 767 = 2FFh |
| 212h | | 02h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 192KB sector region |
| 213h | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 22 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 4KB sector region |
| 214h | JEDEC Sector Map Parameter DWORD-20 Config-1 Region-5 | F1h | Region 5 of 4KB sectors |
| 215h | | FFh | Bits 31:8 = Region size (16 x 4KB) = 0000FFh: Region size as count-1 of 256 Byte units = 16 x 4KB sectors = 64KB Count = 64KB/256 = 256, value = count -1 = 256-1 = 255 = FFh |
| 216h | | 00h | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined |
| 217h | | 00h | Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256KB erase and is not supported in the 4KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4KB erase and is supported in the 4KB sector region |
| 218h | JEDEC Sector Map Parameter DWORD-21 Config-4 Header | FFh | Configuration Index 04h Uniform 256KB sectors |
| 219h | | 04h | Bits 31:24 = RFU = FFh |
| 21Ah | | 00h | Bits 23:16 = Region count (DWORDs -1) = 00h: One region |
| 21Bh | | FFh | Bits 15:8 = Configuration ID = 04h: Uniform 256KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = End of map descriptor = 1 |

Device identification

Table 88 JEDEC SFDP rev D, sector map parameter table (continued)

| SFDP | SFDP DWORD name | Data | Description |
|------|---|---|---|
| 21Ch | JEDEC Sector Map Parameter DWORD-22 Config-4 Region-0 | F8h | Region 0 Uniform 256KB sectors |
| 21Dh | | FFh | Bits 31:8 = 256Mb device Region size = 01FFFFh: Region size as count-1 of 128 Byte units = 128 x 256KB sectors = 32,768KB Count = 32,768KB/256 = 131,072 value = count -1 = 131,072-1= 131,071=01FFFFh |
| 21Eh | | FFh | Bits 31:8 = 512Mb device Region size = 03FFFFh: Region size as count-1 of 256 Byte units = 256 x 256KB sectors = 65,536KB Count = 65,536KB/256 = 262,144 value = count -1 = 262,144-1 = 262,143 = 3FFFFh |
| 21Fh | | 01h (256Mb) 03h (512Mb) 07h (1Gb) | Bits 31:8 = 1Gb device Region size = 07FFFFh: Region size as count-1 of 256 Byte units = 512 x 256KB sectors = 131,072KB Count = 131,072KB/256 = 524,288, value = count -1 = 524,288-1 = 524,287 = 7FFFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256KB erase and is supported in the 256KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 256KB sector region |

9.2 Manufacturer and device ID

Table 89 Manufacturer and device ID

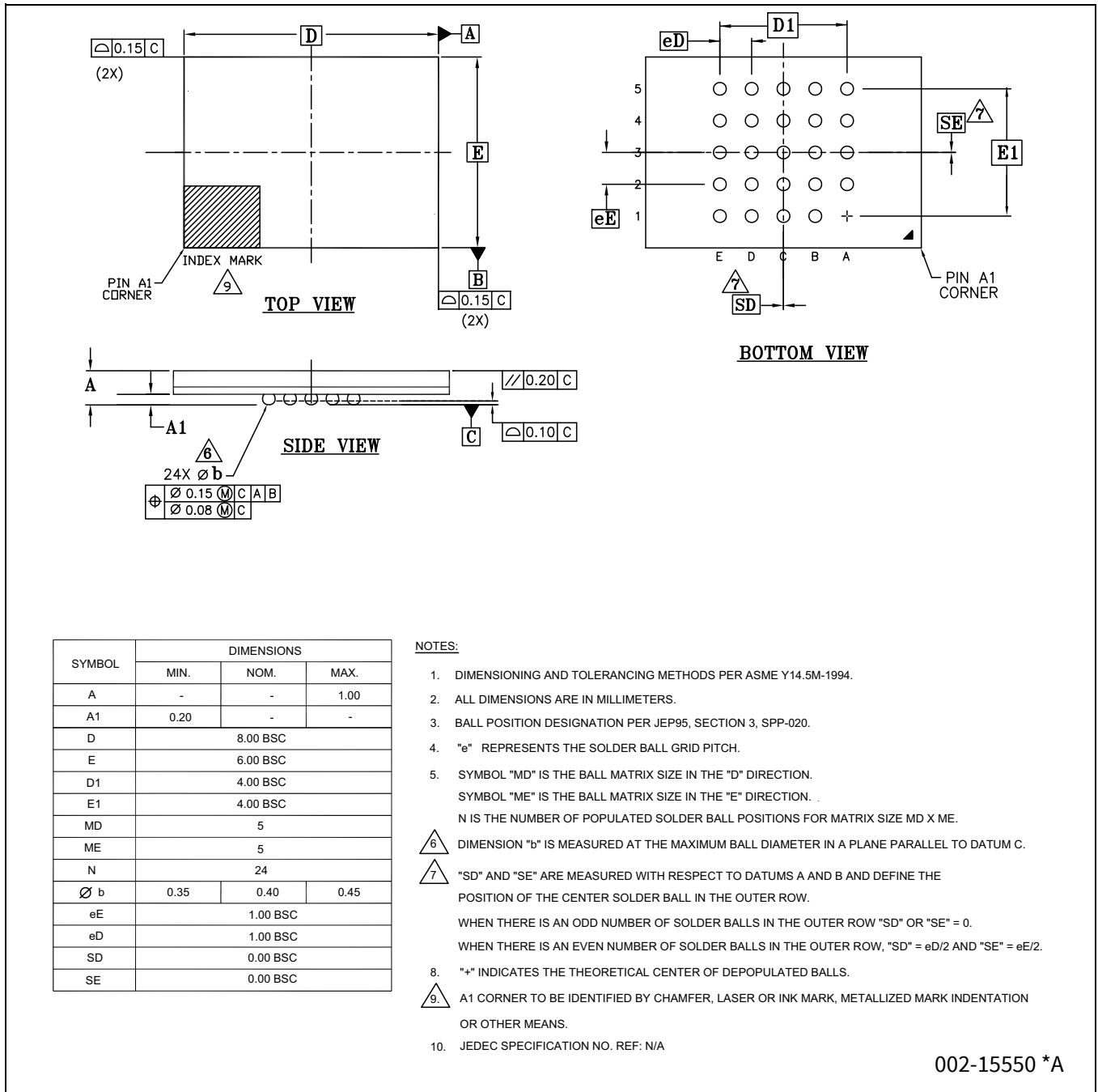
| Byte address | Data | Description |
|--------------|---------------------------------------|---|
| 00h | 34h | Manufacturer ID for CYPRESS™ |
| 01h | 2Ah (HL-T) / 2Bh (HS-T) | Device ID MSB - Memory Interface Type |
| 02h | 19h (256Mb) / 1Ah (512Mb) / 1Bh (1Gb) | Device ID LSB - Density |
| 03h | 0Fh | ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map. |
| 04h | 03h (Default Configuration) | Physical Sector Architecture The HS/L-T family may be configured with or without 4KB parameter sectors in addition to the uniform sectors. 03h = Uniform 256KB with thirty-two 4KB Parameter Sectors) |
| 05h | 90h (HL-T/HS-T Family) | Family ID |

9.3 Unique device ID

Table 90 Unique device ID

| Byte address | Data | Description |
|--------------|-------------------------|-------------------------|
| 00h to 07h | 8-Byte Unique Device ID | 64-bit unique ID number |

10 Package diagrams



002-15550 *A

Figure 85 Ball grid array 24-ball 6 x 8 mm (VAA024)

Package diagrams

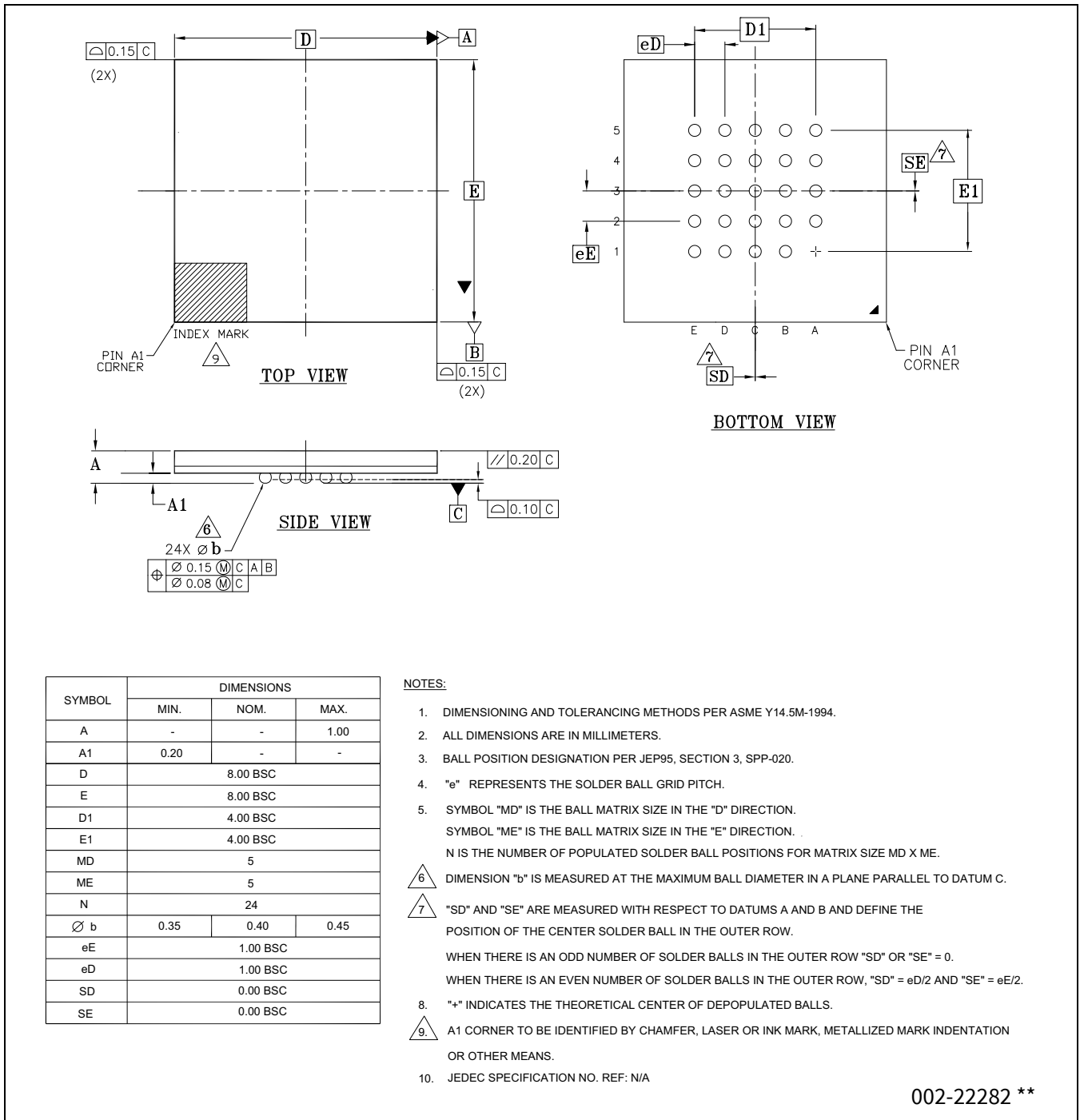
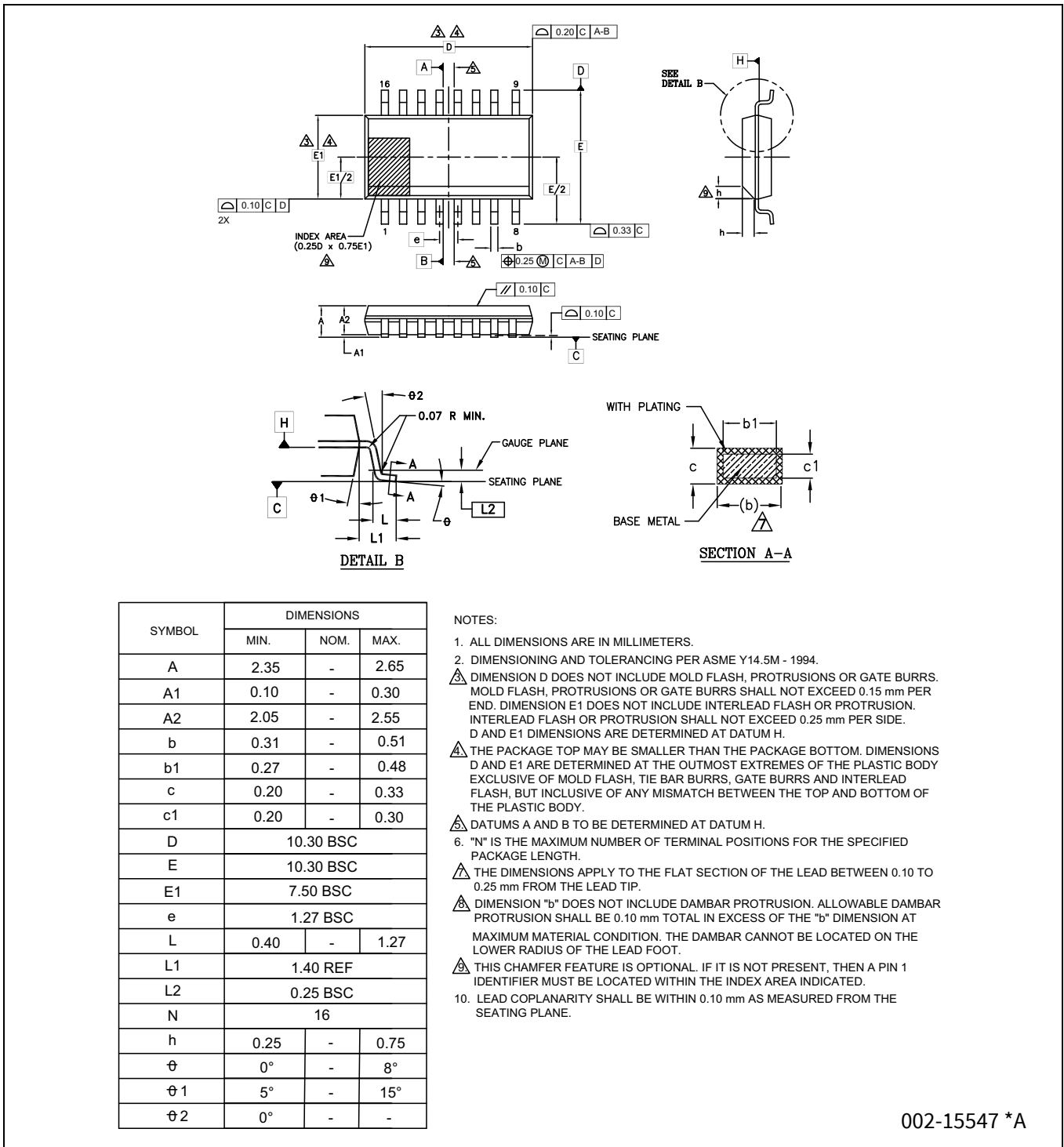


Figure 86 Ball grid array 24-ball 8 x 8 mm (VAC024)

Package diagrams



002-15547 *A

Figure 87 SOIC 16-lead, 300-mil body width (S03016)

Package diagrams

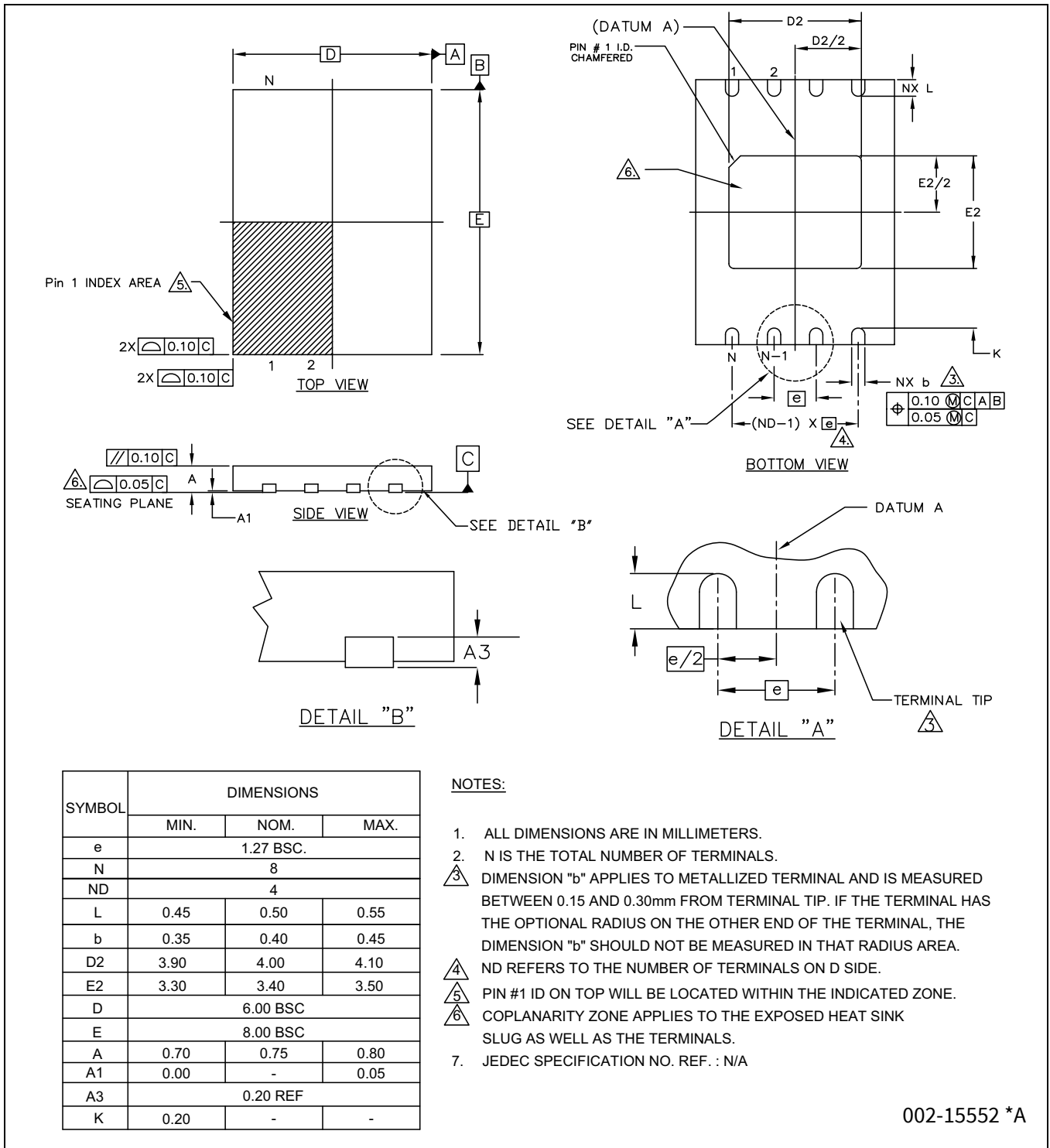
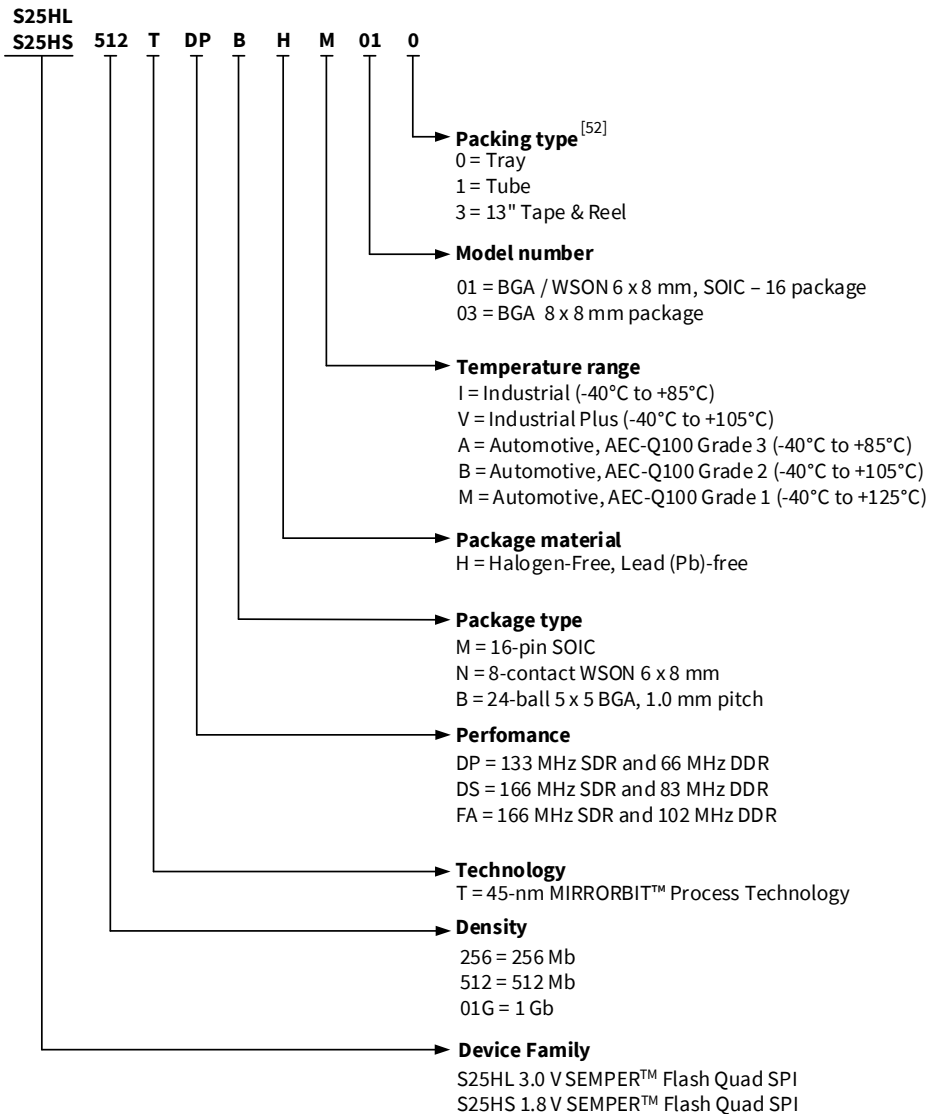


Figure 88 WSON 8-contact 6 × 8 mm leadless (WNH008)

11 Ordering information

The ordering part number is formed by a valid combination of the following:



Note
 52. See Packing and Packaging Handbook on www.cypress.com for further information.

11.1 Valid combinations – Standard grade

Table 91 lists configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 91 Valid combinations – Standard grade

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = Packing Type) | Package marking | |
|---------------------------|--------------|-----------------------|-------------------|--------------|-------------------|---|-------------------|--------------|
| S25HL512T | DP | BH | I, V | 01 | 0, 3 | S25HL512TDPBHI01x | 25HL512TPI01 | |
| | | | | | | S25HL512TDPBHV01x | 25HL512TPV01 | |
| | | MH | I, V | 01 | 0, 1, 3 | S25HL512TDPMHI01x | 25HL512TPI01 | |
| | | | | | | S25HL512TDPMHV01x | 25HL512TPV01 | |
| | | NH | I, V | 01 | 0, 1, 3 | S25HL512TDPNHI01x | 2HL512TPI01 | |
| | | | | | | S25HL512TDPNHV01x | 2HL512TPV01 | |
| | FA | BH | I, V | 01 | 0, 3 | S25HL512TFABHI01x | 25HL512TFI01 | |
| | | | | | | S25HL512TFABHV01x | 25HL512TFV01 | |
| | | MH | I, V | 01 | 0, 1, 3 | S25HL512TFAMHI01x | 25HL512TFI01 | |
| | | | | | | S25HL512TFAMHV01x | 25HL512TFV01 | |
| | | NH | I, V | 01 | 0, 1, 3 | S25HL512TFANHI01x | 2HL512TFI01 | |
| | | | | | | S25HL512TFANHV01x | 2HL512TFV01 | |
| S25HS512T | DP | BH | I, V | 01 | 0, 3 | S25HS512TDPBHI01x | 25HS512TPI01 | |
| | | | | | | S25HS512TDPBHV01x | 25HS512TPV01 | |
| | | MH | I, V | 01 | 0, 1, 3 | S25HS512TDPMHI01x | 25HS512TPI01 | |
| | | | | | | S25HS512TDPMHV01x | 25HS512TPV01 | |
| | | NH | I, V | 01 | 0, 1, 3 | S25HS512TDPNHI01x | 2HS512TPI01 | |
| | | | | | | S25HS512TDPNHV01x | 2HS512TPV01 | |
| | DS | BH | V | 01 | 0, 3 | S25HS512TDSBHV01x | 25HS512TSV01 | |
| | | | | | | S25HS512TDSMHV01x | 25HS512TSV01 | |
| | FA | BH | I, V | 01 | 0, 3 | S25HS512TFABHI01x | 25HS512TFI01 | |
| | | | | | | S25HS512TFABHV01x | 25HS512TFV01 | |
| | | MH | I, V | 01 | 0, 1, 3 | S25HS512TFAMHI01x | 25HS512TFI01 | |
| | | | | | | S25HS512TFAMHV01x | 25HS512TFV01 | |
| | | NH | I, V | 01 | 0, 1, 3 | S25HS512TFANHI01x | 2HS512TFI01 | |
| | | | | | | S25HS512TFANHV01x | 2HS512TFV01 | |
| | S25HL01GT | DP | BH | I, V | 03 | 0, 3 | S25HL01GTDPBHV03x | 25HL01GTPV03 |
| | | | | | | | S25HL01GTDPBHI03x | 25HL01GTPI03 |
| | | | MH | I, V | 01 | 0, 1, 3 | S25HL01GTDPMHV01x | 25HL01GTPV01 |
| | | | | | | | S25HL01GTDPMHI01x | 25HL01GTPI01 |
| FA | | BH | I, V | 03 | 0, 3 | S25HL01GTFABHV03x | 25HL01GTFV03 | |
| | | | | | | S25HL01GTFABHI03x | 25HL01GTFI03 | |
| | | MH | I, V | 01 | 0, 1, 3 | S25HL01GTFAMHI01x | 25HL01GTFI01 | |
| | | | | | | S25HL01GTFAMHV01x | 25HL01GTFV01 | |
| S25HS01GT | | DP | BH | I, V | 03 | 0, 3 | S25HS01GTDPBHI03x | 25HS01GTPI03 |
| | | | | | | | S25HS01GTDPBHV03x | 25HS01GTPV03 |
| | | MH | I, V | 01 | 0, 1, 3 | S25HS01GTDPMHI01x | 25HS01GTPI01 | |
| | | | | | | S25HS01GTDPMHV01x | 25HS01GTPV01 | |
| S25HS01GT | FA | BH | I, V | 03 | 0, 3 | S25HS01GTFABHI03x | 25HS01GTFI03 | |
| | | | | | | S25HS01GTFABHV03x | 25HS01GTFV03 | |
| | MH | I, V | 01 | 0, 1, 3 | S25HS01GTFAMHI01x | 25HS01GTFI01 | | |
| | | | | | S25HS01GTFAMHV01x | 25HS01GTFV01 | | |

11.2 Valid combinations – Automotive grade / AEC-Q100

Table 92 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non-AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 92 Valid combinations – Automotive grade / AEC-Q100

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = packing type) | Package marking |
|---------------------------|--------------|-----------------------|-------------------|--------------|--------------|---|-----------------|
| S25HL512T | DP | BH | A, B, M | 01 | 0, 3 | S25HL512TDPBHA01x | 25HL512TPA01 |
| | | | | | | S25HL512TDPBHB01x | 25HL512TPB01 |
| | | | | | | S25HL512TDPBHM01x | 25HL512TPM01 |
| | | MH | A, B, M | 01 | 0, 1, 3 | S25HL512TDPMHA01x | 25HL512TPA01 |
| | | | | | | S25HL512TDPMHB01x | 25HL512TPB01 |
| | | | | | | S25HL512TDPMHM01x | 25HL512TPM01 |
| | | NH | A, B, M | 01 | 0, 1, 3 | S25HL512TDPNHA01x | 2HL512TPA01 |
| | | | | | | S25HL512TDPNHB01x | 2HL512TPB01 |
| | | | | | | S25HL512TDPNHM01x | 2HL512TPM01 |
| | FA | BH | A, B, M | 01 | 0, 3 | S25HL512TFABHA01x | 25HL512TFA01 |
| | | | | | | S25HL512TFABHB01x | 25HL512TFB01 |
| | | | | | | S25HL512TFABHM01x | 25HL512TFM01 |
| | | MH | A, B, M | 01 | 0, 1, 3 | S25HL512TFAMHA01x | 25HL512TFA01 |
| | | | | | | S25HL512TFAMHB01x | 25HL512TFB01 |
| | | | | | | S25HL512TFAMHM01x | 25HL512TFM01 |
| | | NH | A, B, M | 01 | 0, 1, 3 | S25HL512TFANHA01x | 2HL512TFA01 |
| | | | | | | S25HL512TFANHB01x | 2HL512TFB01 |
| | | | | | | S25HL512TFANHM01x | 2HL512TFM01 |
| S25HS512T | DP | BH | A, B, M | 01 | 0, 3 | S25HS512TDPBHA01x | 25HS512TPA01 |
| | | | | | | S25HS512TDPBHB01x | 25HS512TPB01 |
| | | | | | | S25HS512TDPBHM01x | 25HS512TPM01 |
| | | MH | A, B, M | 01 | 0, 1, 3 | S25HS512TDPMHA01x | 25HS512TPA01 |
| | | | | | | S25HS512TDPMHB01x | 25HS512TPB01 |
| | | | | | | S25HS512TDPMHM01x | 25HS512TPM01 |
| | | NH | A, B, M | 01 | 0, 1, 3 | S25HS512TDPNHA01x | 2HS512TPA01 |
| | | | | | | S25HS512TDPNHB01x | 2HS512TPB01 |
| | | | | | | S25HS512TDPNHM01x | 2HS512TPM01 |
| | FA | BH | A, B, M | 01 | 0, 3 | S25HS512TFABHA01x | 25HS512TFA01 |
| | | | | | | S25HS512TFABHB01x | 25HS512TFB01 |
| | | | | | | S25HS512TFABHM01x | 25HS512TFM01 |

Ordering information

Table 92 Valid combinations – Automotive grade / AEC-Q100 (continued)

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = packing type) | Package marking | |
|---------------------------|--------------|-----------------------|-------------------|--------------|--------------|---|-------------------|--------------|
| S25HS512T | FA | MH | A, B, M | 01 | 0, 1, 3 | S25HS512TFAMHA01x | 25HS512TFA01 | |
| | | | | | | S25HS512TFAMHB01x | 25HS512TFB01 | |
| | | | | | | S25HS512TFAMHM01x | 25HS512TFM01 | |
| | | NH | A, B, M | 01 | 0, 1, 3 | 0, 1, 3 | S25HS512TFANHA01x | 2HS512TFA01 |
| | | | | | | | S25HS512TFANHB01x | 2HS512TFB01 |
| | | | | | | | S25HS512TFANHM01x | 2HS512TFM01 |
| S25HL01GT | DP | BH | A, B, M | 03 | 0, 3 | S25HL01GTDPBHA03x | 25HL01GTPA03 | |
| | | | | | | S25HL01GTDPBHB03x | 25HL01GTPB03 | |
| | | | | | | S25HL01GTDPBHM03x | 25HL01GTPM03 | |
| | | MH | A, B, M | 01 | 0, 1, 3 | 0, 1, 3 | S25HL01GTDPMHA01x | 25HL01GTPA01 |
| | | | | | | | S25HL01GTDPMHB01x | 25HL01GTPB01 |
| | | | | | | | S25HL01GTDPMHM01x | 25HL01GTPM01 |
| | FA | BH | A, B, M | 03 | 0, 3 | 0, 3 | S25HL01GTFABHA03x | 25HL01GTFA03 |
| | | | | | | | S25HL01GTFABHB03x | 25HL01GTFB03 |
| | | | | | | | S25HL01GTFABHM03x | 25HL01GTFM03 |
| | | MH | A, B, M | 01 | 0, 1, 3 | 0, 1, 3 | S25HL01GTFAMHA01x | 25HL01GTFA01 |
| | | | | | | | S25HL01GTFAMHB01x | 25HL01GTFB01 |
| | | | | | | | S25HL01GTFAMHM01x | 25HL01GTFM01 |
| S25HS01GT | DP | BH | A, B, M | 03 | 0, 3 | S25HS01GTDPBHA03x | 25HS01GTPA03 | |
| | | | | | | S25HS01GTDPBHB03x | 25HS01GTPB03 | |
| | | | | | | S25HS01GTDPBHM03x | 25HS01GTPM03 | |
| | | MH | A, B, M | 01 | 0, 1, 3 | 0, 1, 3 | S25HS01GTDPMHA01x | 25HS01GTPA01 |
| | | | | | | | S25HS01GTDPMHB01x | 25HS01GTPB01 |
| | | | | | | | S25HS01GTDPMHM01x | 25HS01GTPM01 |
| | FA | BH | A, B, M | 03 | 0, 3 | 0, 3 | S25HS01GTFABHA03x | 25HS01GTFA03 |
| | | | | | | | S25HS01GTFABHB03x | 25HS01GTFB03 |
| | | | | | | | S25HS01GTFABHM03x | 25HS01GTFM03 |
| | | MH | A, B, M | 01 | 0, 1, 3 | 0, 1, 3 | S25HS01GTFAMHA01x | 25HS01GTFA01 |
| | | | | | | | S25HS01GTFAMHB01x | 25HS01GTFB01 |
| | | | | | | | S25HS01GTFAMHM01x | 25HS01GTFM01 |

Revision history

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|---|
| *P | 2019-06-04 | Finalizing document for S25HS512T devices. |
| *Q | 2019-06-21 | Finalizing document for S25HL512T devices. Updated t_{VR} parameter. Introduced t_{VF} parameter. |
| *R | 2019-07-03 | Finalizing document for S25HL01GT devices. Updated I_{CC1} parameters. Updated Valid Combinations. |
| *S | 2019-09-13 | Updated Transaction table. Updated Ordering Information. |
| *T | 2019-11-26 | Finalizing document for S25HS01GT devices. |
| *U | 2019-12-20 | Updated Table 17 , Table 85 , and Table 87 (Product Information Notification). |
| *V | 2019-01-29 | Updated Table 73 . Updated Sales information and Copyright year. |
| *W | 2020-03-23 | Updated Table 81 based on Final Characterization results. |
| *X | 2020-04-22 | Updated Table 9 , Table 48 , and Table 55 . Updated Table 85 and Table 87 (Product Information Notification). |
| *Y | 2020-12-01 | Updated text in Read QPI SDR and DDR transaction and Read QPI SDR and DDR transaction . Updated Related SPI Transaction for Configuration Register 4 to RDAY1_4_0 in Table 29 . Updated text in Data learning pattern (DLP) . Updated selection options for CFR3N[7:6], CFR3V[7:6] in Table 50 . Added note in Table 56 . Updated description and note for ASPO[2] in Table 58 . Updated CFR3N[3], CFR1N[6], and CFR1N[2] to CFR3V[3], CFR1V[6], and CFR1V[2] in Sector Map Parameter Table Notes . Updated Sector Map Parameters in Table 86 . Updated SFDP DWORD, Data, and Description in Table 87 . |
| *Z | 2021-10-18 | Updated to Infineon template. Updated Table 79 : Added Theta JB and JC and 256Mb packages. Updated Table 82 : Added 256Mb specifications. Updated Table 84 : Added 256Mb specifications. Updated Table 86 : Added 256Mb specifications. |
| AA | 2022-01-18 | Updated Table 6 : Changed JESD216C to JESD216D Changed CFR3V[1:0] to CFR3V[7:6] in Read device identification transaction Updated Table 84 : Removed 256T / 512T / 01GT and updated max value for t_{PEDS} Updated Table 86 : Updated data and description for 12Dh, 12Eh, and 12Fh byte addresses |

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Edition 2022-01-18
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
002-12345 Rev. AA

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