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NXH80T120L2Q0S2G/S2TG, NXH80T120L2Q0P2G

Q0PACK Module

The NXH80T120L2Q0S2/P2G is a power module containing a T−type neutral point clamped (NPC) three level inverter stage. The integrated field stop trench IGBTs and fast recovery diodes provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Low Switching Loss
- Low V_{CESAT}
- Compact 65.9 mm x 32.5 mm x 12 mm Package
- Thermistor
- Options with pre−applied thermal interface material (TIM) and without pre−applied TIM
- Options with solderable pins and press−fit pins

Typical Applications

- Solar Inverter
- Uninterruptable Power Supplies

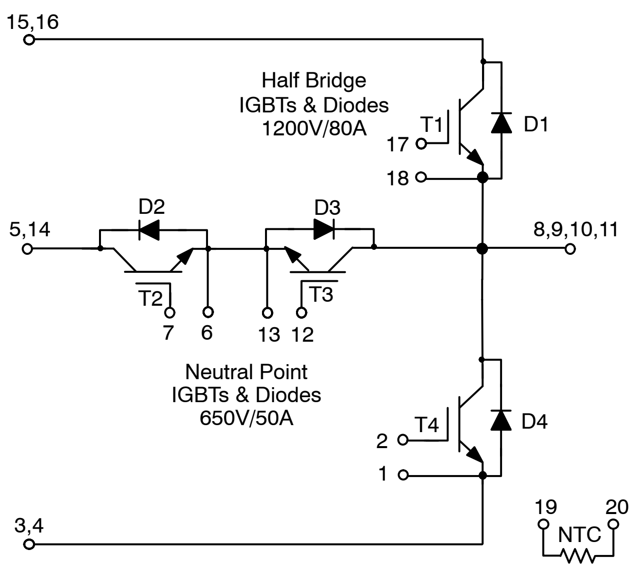

Figure 1. Schematic Diagram

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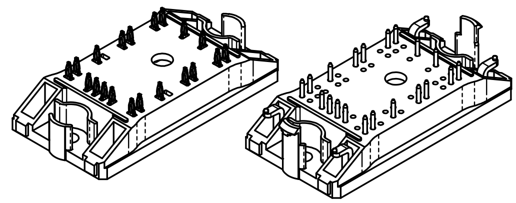
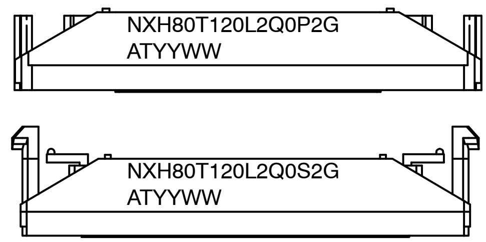


Q0PACK
CASE 180AA
PRESS−FIT PINS

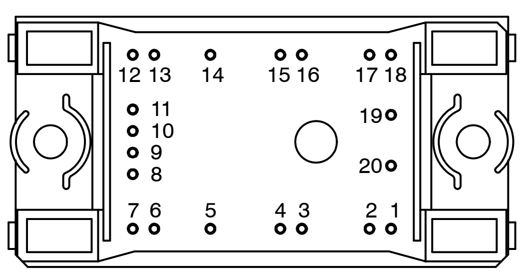
Q0PACK
CASE 180AB
SOLDERABLE PINS

MARKING DIAGRAMS



NXH80T120L2Q0S2G = Specific Device Code
G = Pb−free Package
A = Assembly Site Code
T = Test Site Code
YYWW = Year and Work Week Code

PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 13 of this data sheet.

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HALF BRIDGE IGBT			
Collector−Emitter Voltage	V_{CES}	1200	V
Gate−Emitter Voltage	V_{GE}	±20	V
Continuous Collector Current @ T_h = 80°C (T_J = 175°C)	I_C	67	A
Pulsed Collector Current (T_J = 175°C)	I_{Cpulse}	201	A
Maximum Power Dissipation @ T_h = 80°C (T_J = 175°C)	P_{tot}	158	W
Short Circuit Withstand Time @ V_{GE} = 15 V, V_{CE} = 600 V, $T_J \leq$ 150°C	T_{sc}	5	μs
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
NEUTRAL POINT IGBT			
Collector−Emitter Voltage	V_{CES}	600	V
Gate−Emitter Voltage	V_{GE}	±20	V
Continuous Collector Current @ T_h = 80°C (T_J = 175°C)	I_C	49	A
Pulsed Collector Current (T_J = 175°C)	I_{Cpulse}	147	A
Maximum Power Dissipation @ T_h = 80°C (T_J = 175°C)	P_{tot}	86	W
Short Circuit Withstand Time @ V_{GE} = 15 V, V_{CE} = 400 V, $T_J \leq$ 150°C	T_{sc}	5	μs
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
HALF BRIDGE DIODE			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ T_h = 80°C (T_J = 175°C)	I_F	28	A
Repetitive Peak Forward Current (T_J = 175°C, t_p limited by T_{Jmax})	I_{FRM}	84	A
Maximum Power Dissipation @ T_h = 80°C (T_J = 175°C)	P_{tot}	73	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
NEUTRAL POINT DIODE			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Continuous Forward Current @ T_h = 80°C (T_J = 175°C)	I_F	33	A
Repetitive Peak Forward Current (T_J = 175°C, t_p limited by T_{Jmax})	I_{FRM}	99	A
Maximum Power Dissipation @ T_h = 80°C (T_J = 175°C)	P_{tot}	63	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
THERMAL PROPERTIES			
Storage Temperature range	T_{stg}	−40 to 125	°C
INSULATION PROPERTIES			
Isolation test voltage, t = 1 sec, 60 Hz	V_{is}	3000	V_{RMS}
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

Table 2. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
HALF BRIDGE IGBT CHARACTERISTICS						
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 1200 V	I_{CES}	–	–	300	μA
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 80 A, T_J = 25°C	$V_{CE(sat)}$	–	2.05	2.85	V
	V_{GE} = 15 V, I_C = 80 A, T_J = 150°C		–	2.10	–	
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 1.5 mA	$V_{GE(TH)}$	–	5.45	6.4	V
Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	300	nA
Turn−on Delay Time	T_J = 25°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15V, R_G = 4.7 Ω	$t_{d(on)}$	–	61	–	ns
Rise Time		t_r	–	28	–	
Turn−off Delay Time		$t_{d(off)}$	–	205	–	
Fall Time		t_f	–	41	–	
Turn−on Switching Loss per Pulse		E_{on}	–	550	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	1100	–	
Turn−on Delay Time	T_J = 125°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	$t_{d(on)}$	–	58	–	ns
Rise Time		t_r	–	30	–	
Turn−off Delay Time		$t_{d(off)}$	–	230	–	
Fall Time		t_f	–	63	–	
Turn−on Switching Loss per Pulse		E_{on}	–	720	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	1700	–	
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	19400	–	pF
Output Capacitance		C_{oes}	–	400	–	
Reverse Transfer Capacitance		C_{res}	–	340	–	
Total Gate Charge	V_{CE} = 600 V, I_C = 80 A, V_{GE} = +15 V	Q_g	–	800	–	nC
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 76 μm ±2%, λ = 2.9 W/mK	R_{thJH}	–	0.60	–	°C/W
NEUTRAL POINT DIODE CHARACTERISTICS						
Diode Forward Voltage	I_F = 60 A, T_J = 25°C	V_F	–	1.7	2.2	V
	I_F = 60 A, T_J = 150°C		–	1.6	–	
Reverse Recovery Time	T_J = 25°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	t_{rr}	–	39	–	ns
Reverse Recovery Charge		Q_{rr}	–	1.1	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	48	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	3400	–	A/μs
Reverse Recovery Energy		E_{rr}	–	400	–	μJ
Reverse Recovery Time	T_J = 125°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	t_{rr}	–	78	–	ns
Reverse Recovery Charge		Q_{rr}	–	2.0	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	59	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1600	–	A/μs
Reverse Recovery Energy		E_{rr}	–	550	–	μJ
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 76 μm ±2%, λ = 2.9 W/mK	R_{thJH}	–	1.50	–	°C/W
NEUTRAL POINT IGBT CHARACTERISTICS						
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 600 V	I_{CES}	–	–	250	μA
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 50 A, T_J = 25°C	$V_{CE(sat)}$	–	1.40	1.75	V
	V_{GE} = 15 V, I_C = 50 A, T_J = 150°C		–	1.50	–	
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 1.2 mA	$V_{GE(TH)}$	–	5.45	6.4	V
Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	200	nA

Table 3. ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
NEUTRAL POINT IGBT CHARACTERISTICS						
Turn−on Delay Time	T_J = 25°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	$t_{d(on)}$	–	30	–	ns
Rise Time		t_r	–	19	–	
Turn−off Delay Time		$t_{d(off)}$	–	110	–	
Fall Time		t_f	–	23	–	
Turn−on Switching Loss per Pulse		E_{on}	–	800	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	480	–	
Turn−on Delay Time	T_J = 125°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	$t_{d(on)}$	–	32	–	ns
Rise Time		t_r	–	18	–	
Turn−off Delay Time		$t_{d(off)}$	–	120	–	
Fall Time		t_f	–	35	–	
Turn−on Switching Loss per Pulse		E_{on}	–	1100	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	880	–	
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	9400	–	pF
Output Capacitance		C_{oes}	–	280	–	
Reverse Transfer Capacitance		C_{res}	–	250	–	
Total Gate Charge	V_{CE} = 480 V, I_C = 50 A, V_{GE} = +15 V	Q_g	–	395	–	nC
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 76 μm ±2%, λ = 2.9 W/mK	R_{thJH}	–	1.10	–	°C/W
HALF BRIDGE DIODE CHARACTERISTICS						
Diode Forward Voltage	I_F = 40 A, T_J = 25°C	V_F	–	2.11	3.10	V
	I_F = 40 A, T_J = 150°C		–	1.50	–	
Reverse recovery time	T_J = 25°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	t_{rr}	–	45	–	ns
Reverse recovery charge		Q_{rr}	–	2.7	–	μC
Peak reverse recovery current		I_{RRM}	–	110	–	A
Peak rate of fall of recovery current		di/dt	–	7100	–	A/μs
Reverse recovery energy		E_{rr}	–	1000	–	μJ
Reverse recovery time	T_J = 125°C V_{CE} = 350 V, I_C = 60 A V_{GE} = ±15 V, R_G = 4.7 Ω	t_{rr}	–	185	–	ns
Reverse recovery charge		Q_{rr}	–	6	–	μC
Peak reverse recovery current		I_{RRM}	–	150	–	A
Peak rate of fall of recovery current		di/dt	–	5900	–	A/μs
Reverse recovery energy		E_{rr}	–	1900	–	μJ
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 76 μm ±2%, λ = 2.9 W/mK	R_{thJH}	–	1.30	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal resistance	T = 25°C	R_{25}	–	22	–	kΩ
Nominal resistance	T = 100°C	R_{100}	–	1486	–	Ω
Deviation of R25		ΔR/R	−5	–	5	%
Power dissipation		P_D	–	200	–	mW
Power dissipation constant			–	2	–	mW/K
B−value	B(25/50), tolerance ±3%		–	3950	–	K
B−value	B(25/100), tolerance ±3%		–	3998	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – Half Bridge IGBT and Neutral Point Diode

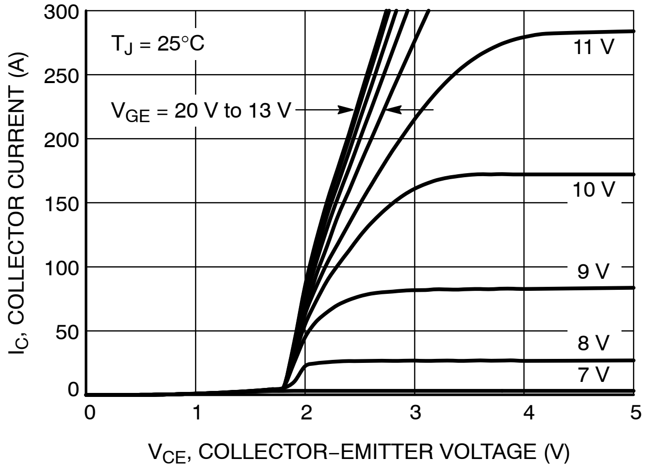


Figure 2. Typical Output Characteristics

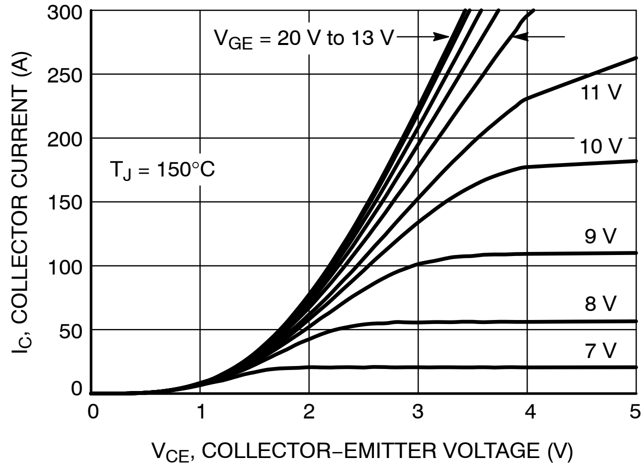


Figure 3. Typical Output Characteristics

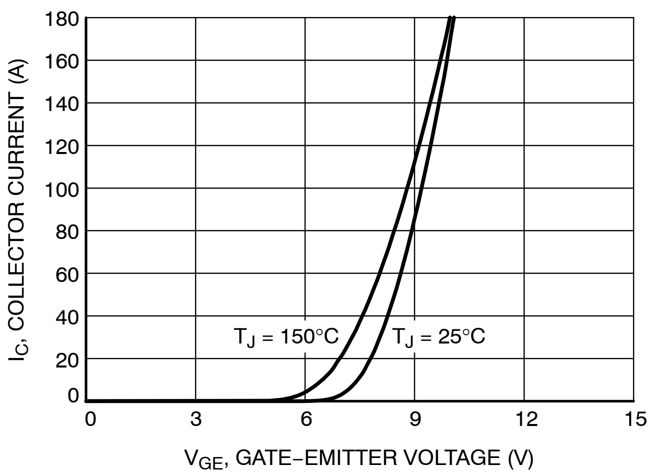


Figure 4. Typical Transfer Characteristics

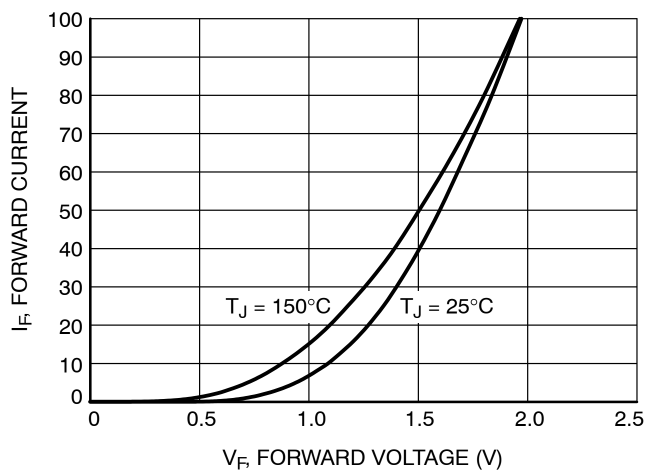


Figure 5. Diode Forward Characteristics

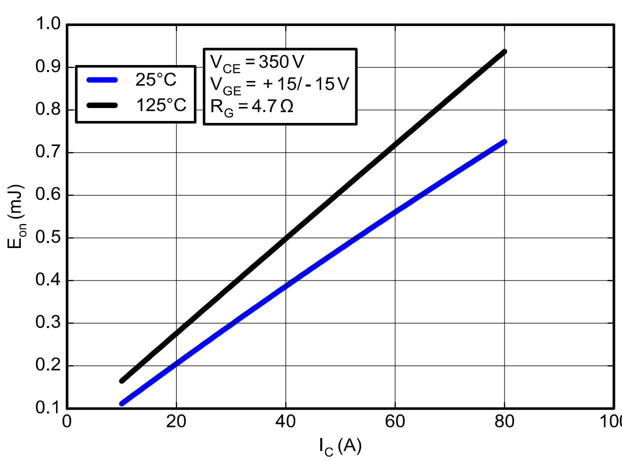


Figure 6. Typical Turn On Loss vs. IC

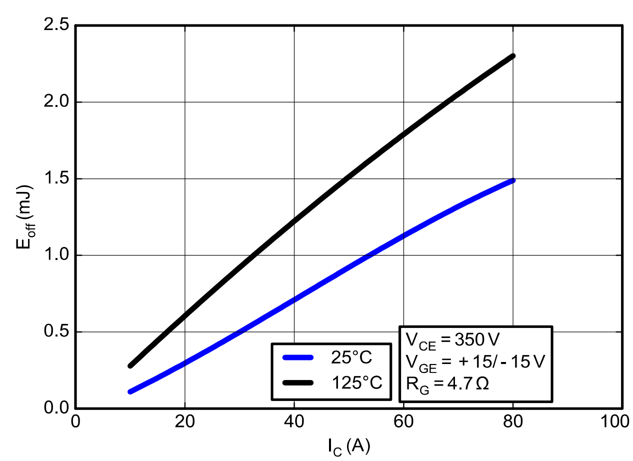


Figure 7. Typical Turn Off Loss vs. IC

TYPICAL CHARACTERISTICS – Half Bridge IGBT and Neutral Point Diode

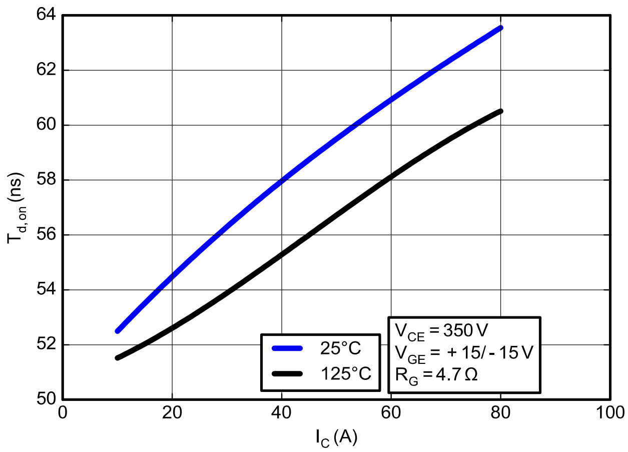


Figure 8. Typical On Switching Times vs. IC

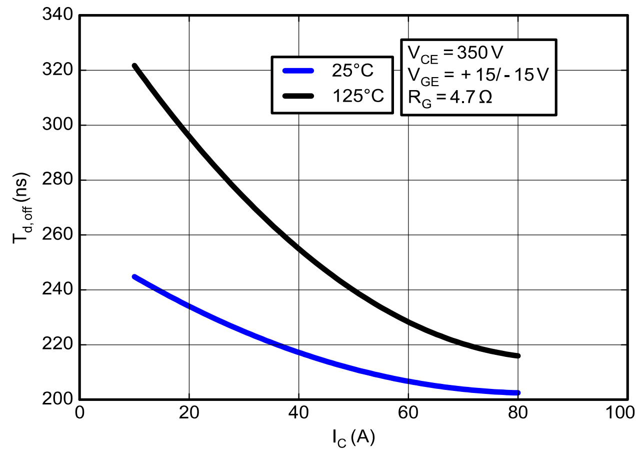


Figure 9. Typical Off Switching Times vs. IC

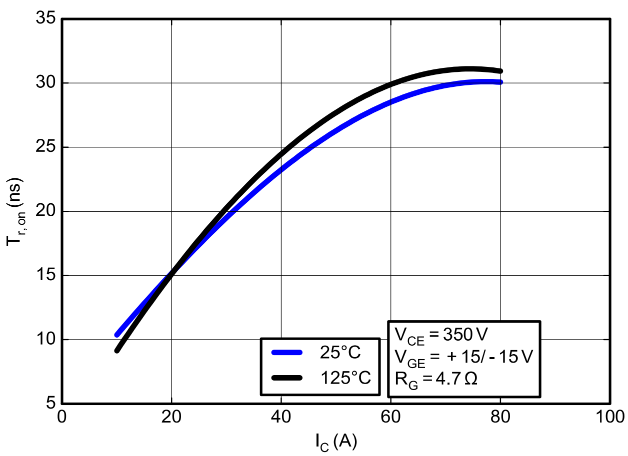


Figure 10. Typical On Rise Times vs. IC

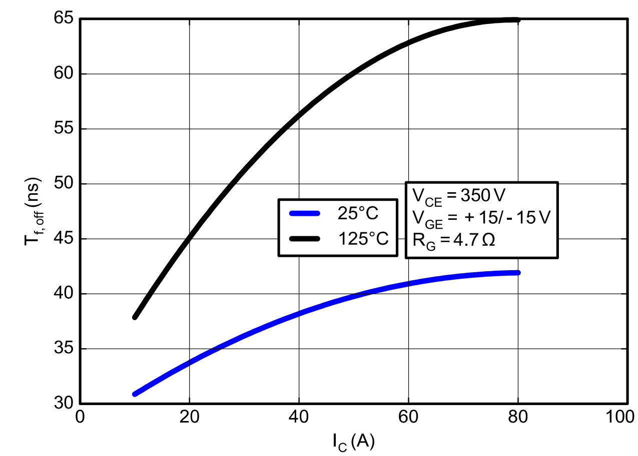


Figure 11. Typical Off Fall Times vs. IC

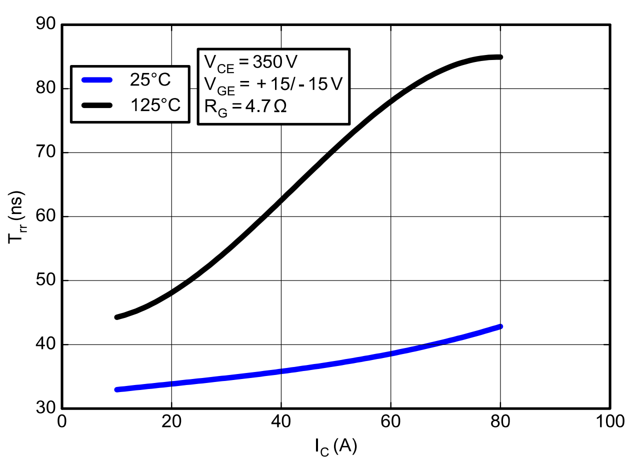


Figure 12. Typical Reverse Recovery Time vs. IC

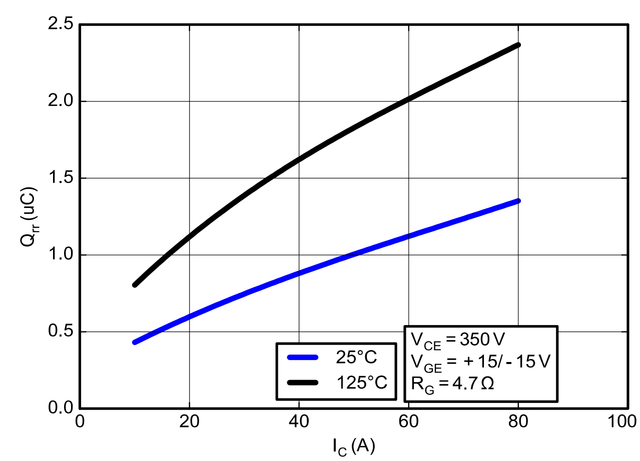


Figure 13. Typical Reverse Recovery Charge vs. IC

TYPICAL CHARACTERISTICS – Half Bridge IGBT and Neutral Point Diode

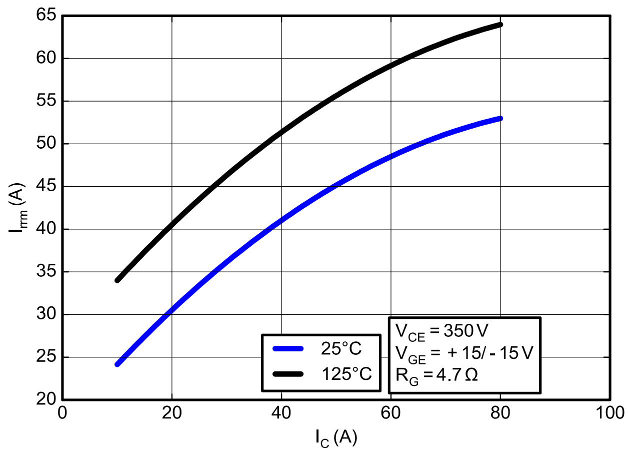


Figure 14. Typical Reverse Recovery Peak Current vs. IC

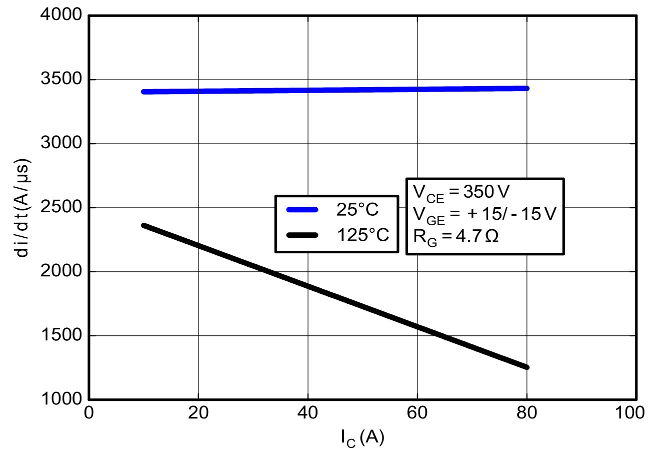


Figure 15. Typical Diode Current Slope vs. IC

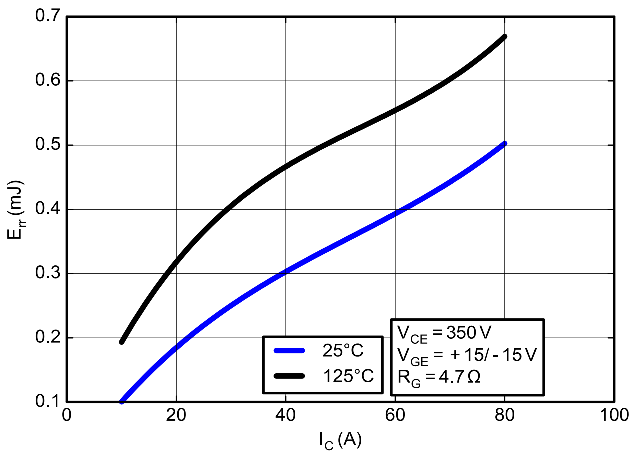


Figure 16. Typical Reverse Recovery Energy vs. IC

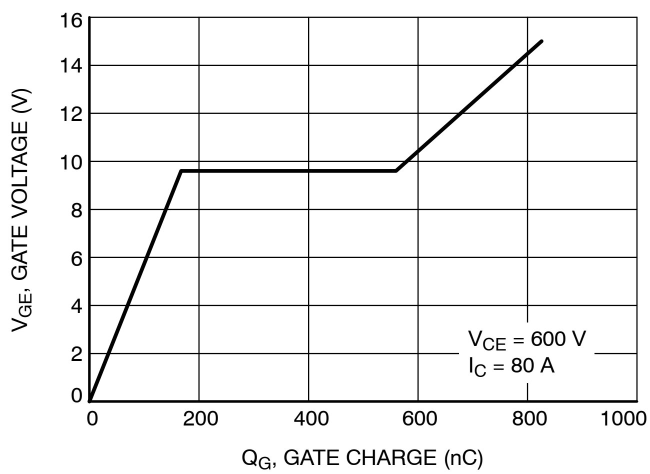


Figure 17. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – Half Bridge IGBT and Neutral Point Diode

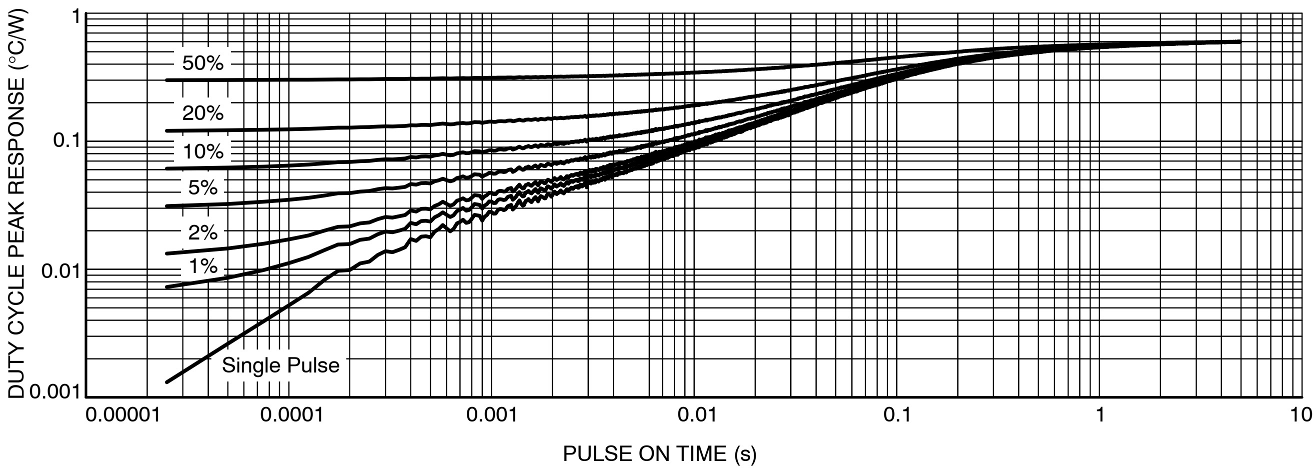


Figure 18. IGBT Transient Thermal Impedance

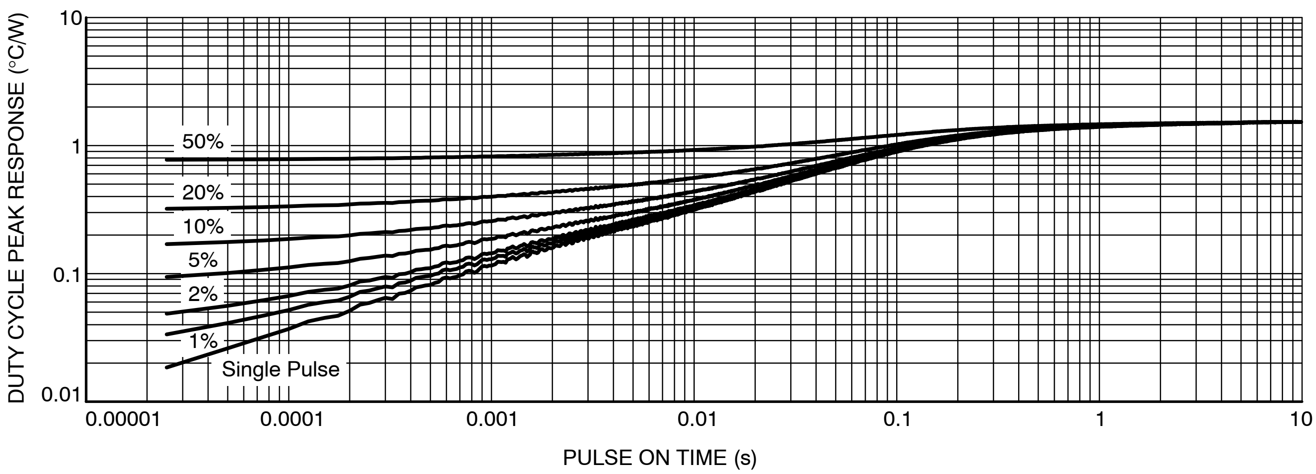


Figure 19. Diode Transient Thermal Impedance

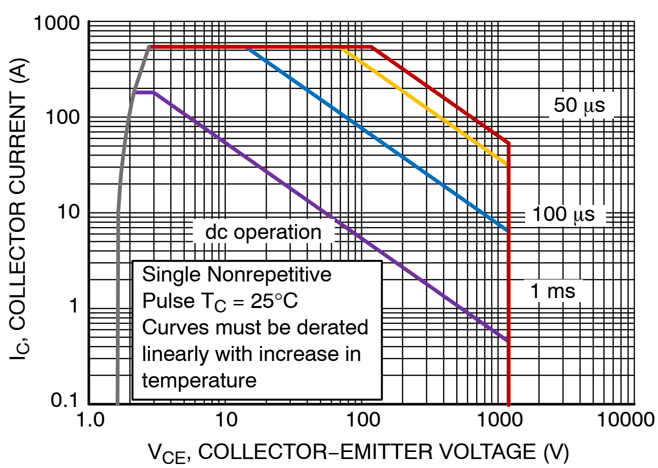


Figure 20. T1 & T4 FBSOA

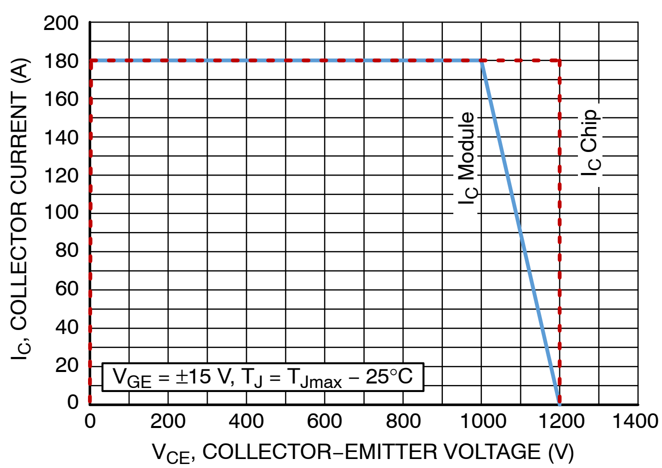


Figure 21. T1 & T4 RBSOA

TYPICAL CHARACTERISTICS – Neutral Point IGBT and Half Bridge Diode

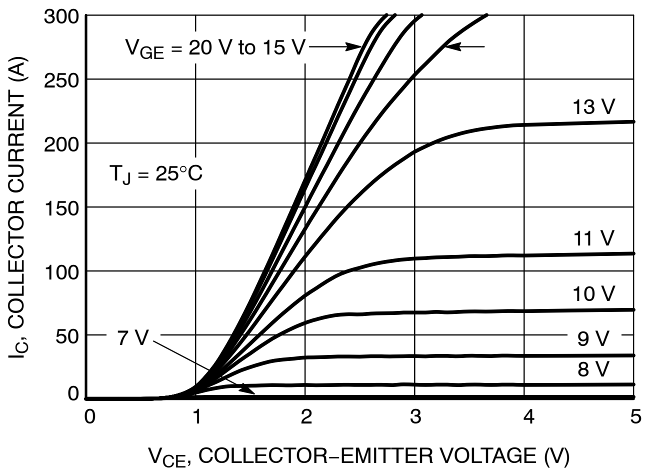


Figure 22. Typical Output Characteristics

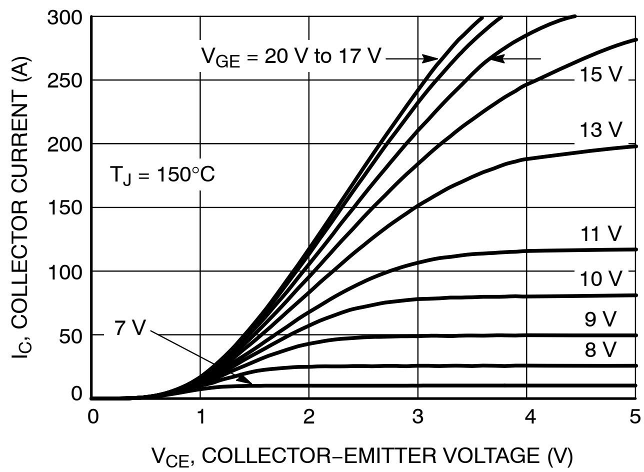


Figure 23. Typical Output Characteristics

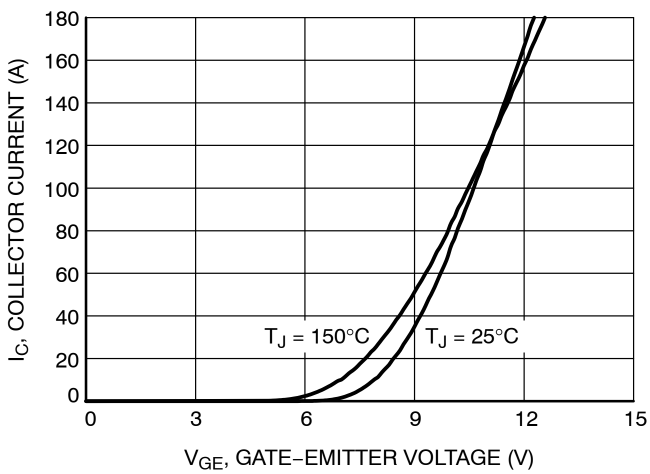


Figure 24. Typical Transfer Characteristics

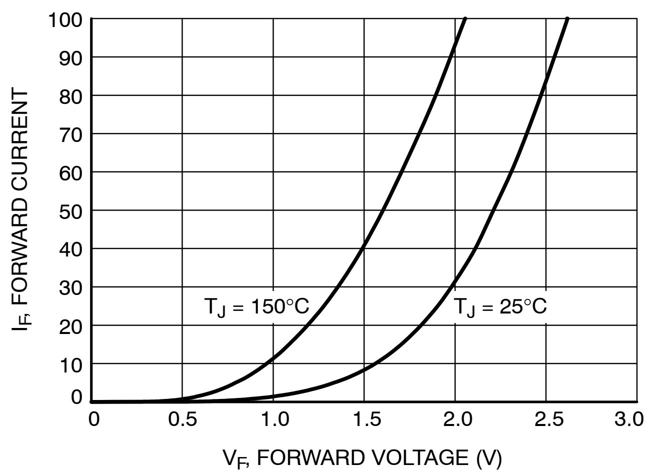


Figure 25. Diode Forward Characteristics

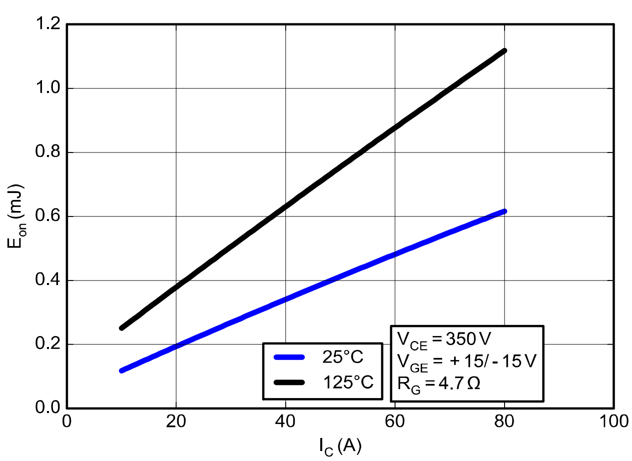


Figure 26. Typical Turn On Loss vs. IC

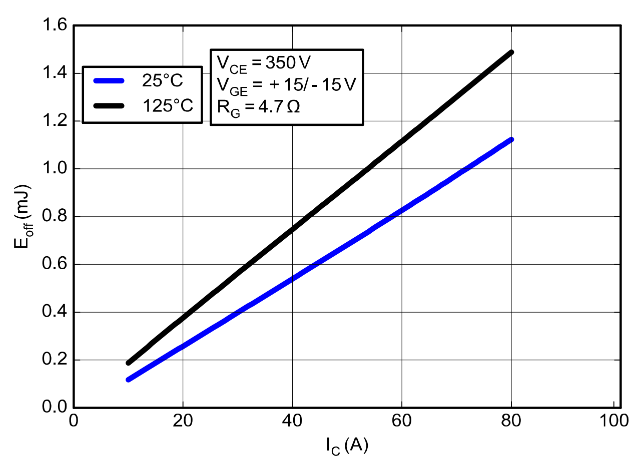


Figure 27. Typical Turn Off Loss vs. IC

TYPICAL CHARACTERISTICS – Neutral Point IGBT and Half Bridge Diode

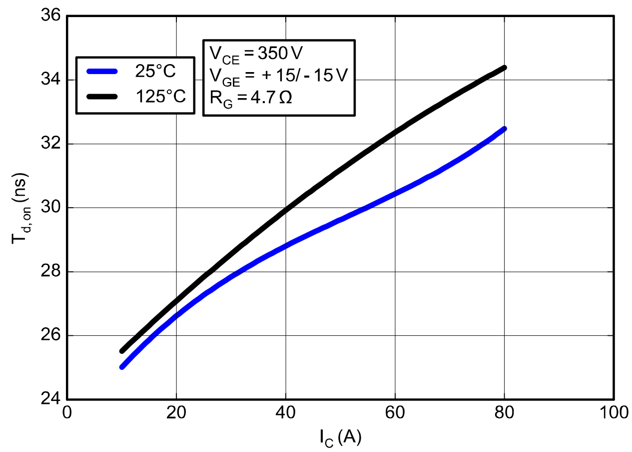


Figure 28. Typical On Switching Times vs. IC

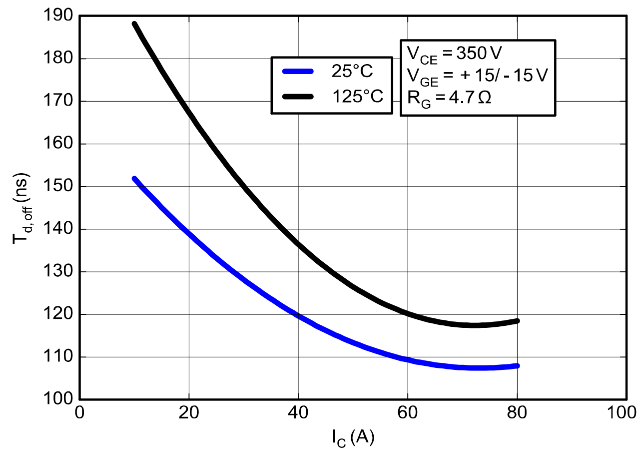


Figure 29. Typical Off Switching Times vs. IC

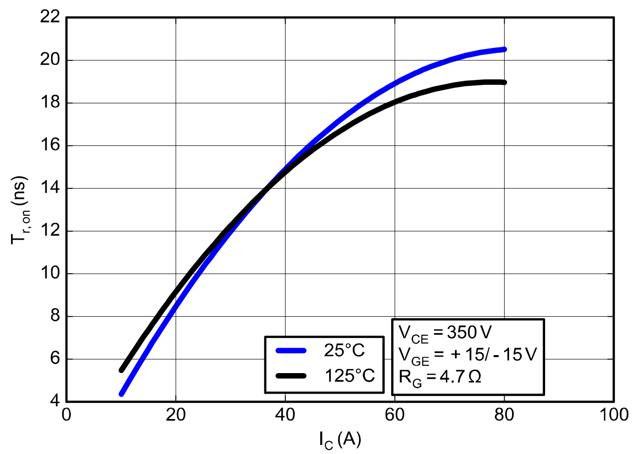


Figure 30. Typical On Rise Times vs. IC

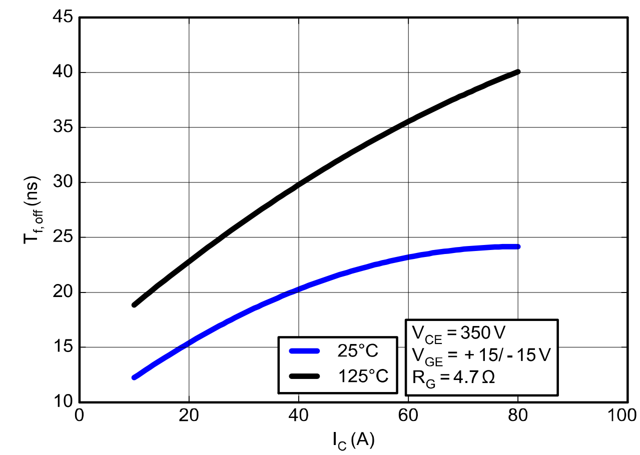


Figure 31. Typical Off Fall Times vs. IC

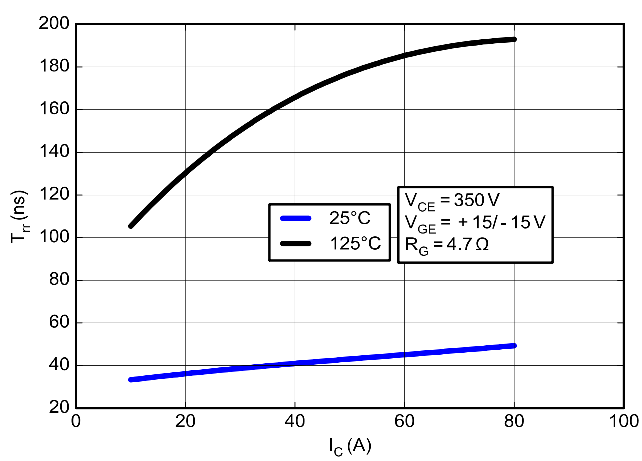


Figure 32. Typical Reverse Recovery Time vs. IC

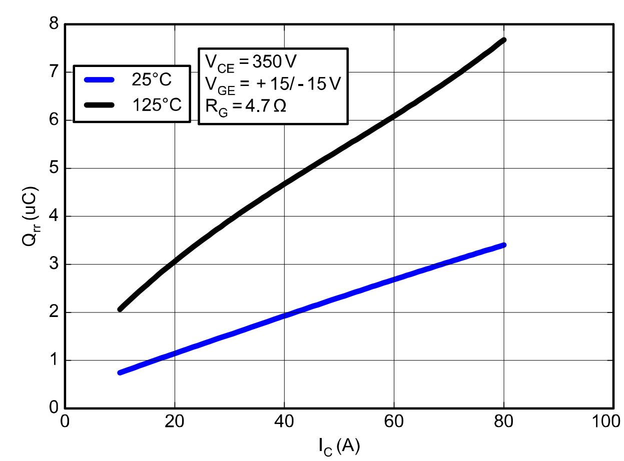


Figure 33. Typical Reverse Recovery Charge vs. IC

TYPICAL CHARACTERISTICS – Neutral Point IGBT and Half Bridge Diode

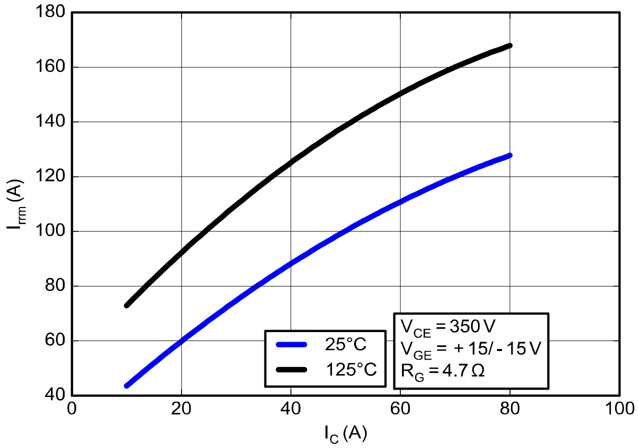


Figure 34. Typical Reverse Recovery Peak Current vs. IC

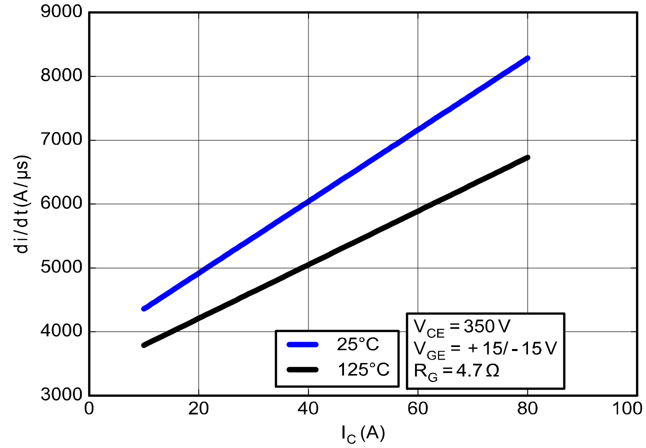


Figure 35. Typical Diode Current Slope vs. IC

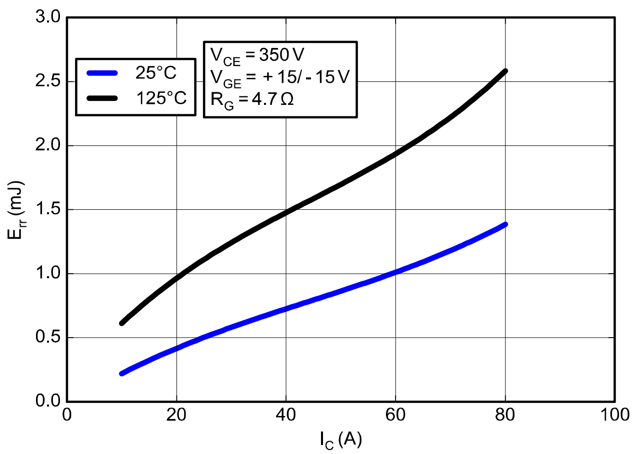


Figure 36. Typical Reverse Recovery Energy vs. IC

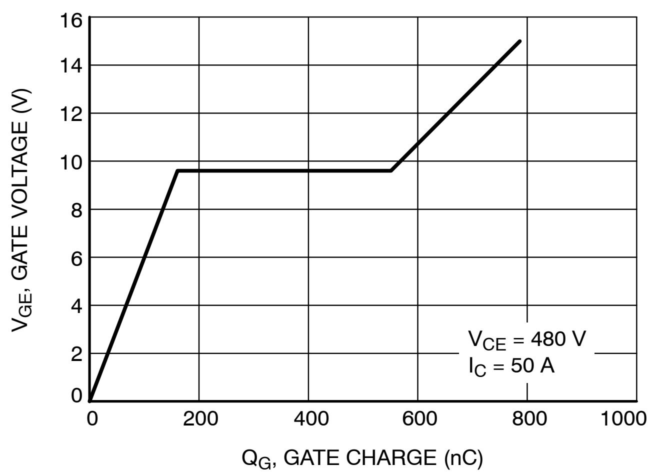


Figure 37. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – Neutral Point IGBT and Half Bridge Diode

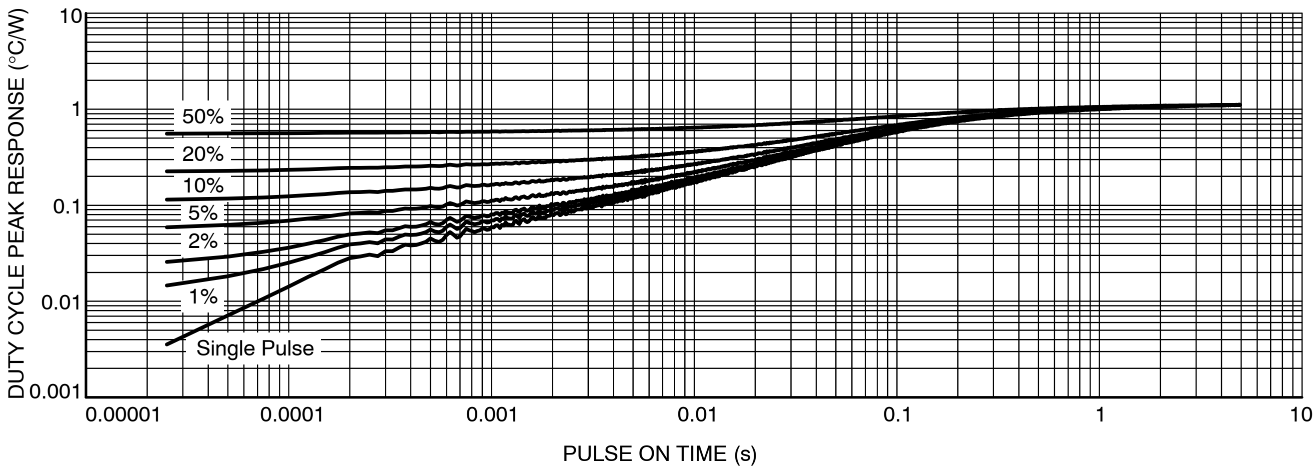


Figure 38. IGBT Transient Thermal Impedance

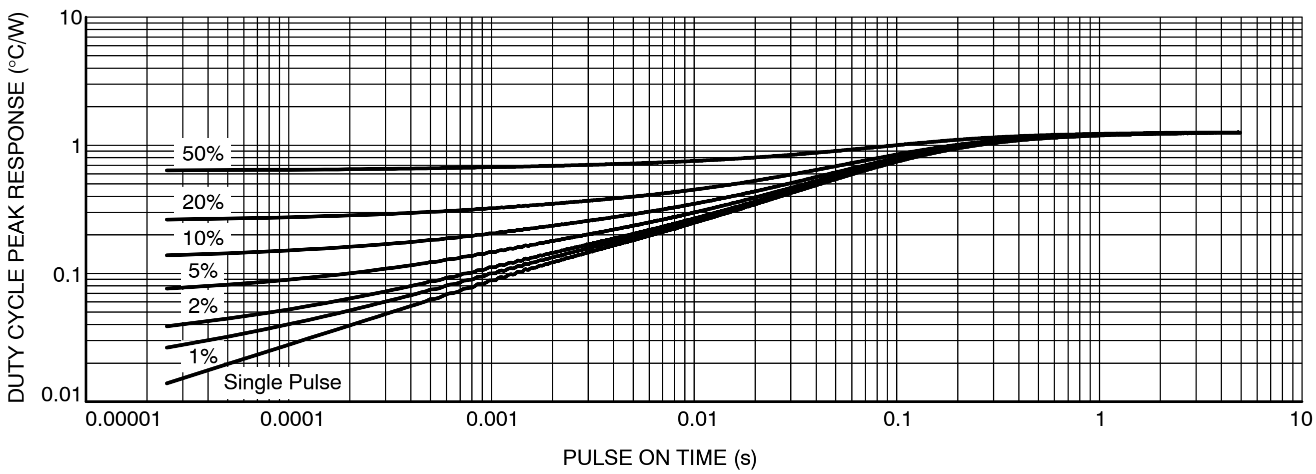


Figure 39. Diode Transient Thermal Impedance

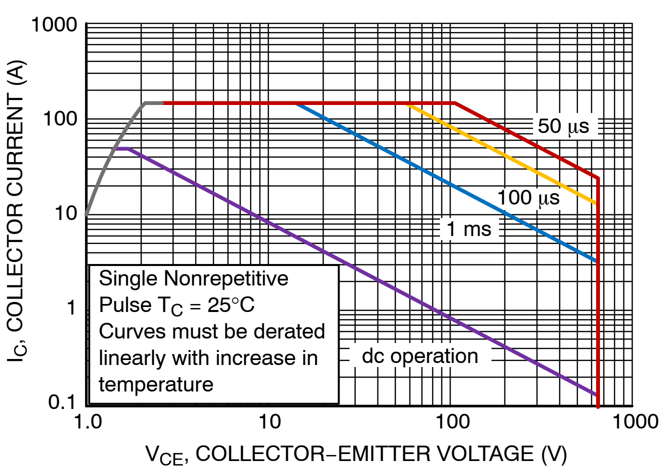


Figure 40. T2 & T3 FBSOA

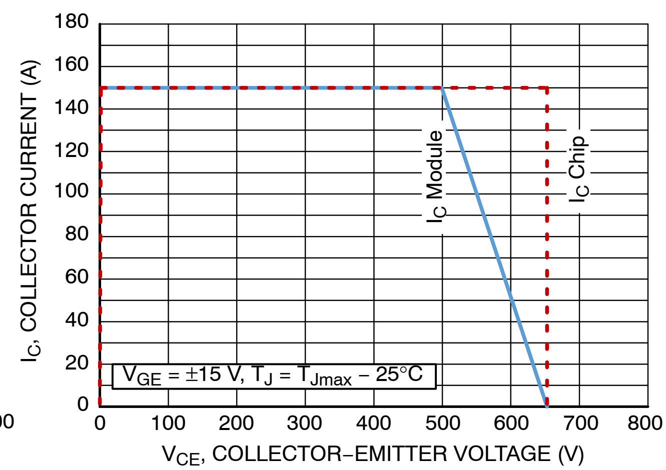


Figure 41. T2 & T3 RBSOA

TYPICAL CHARACTERISTICS − Thermistor

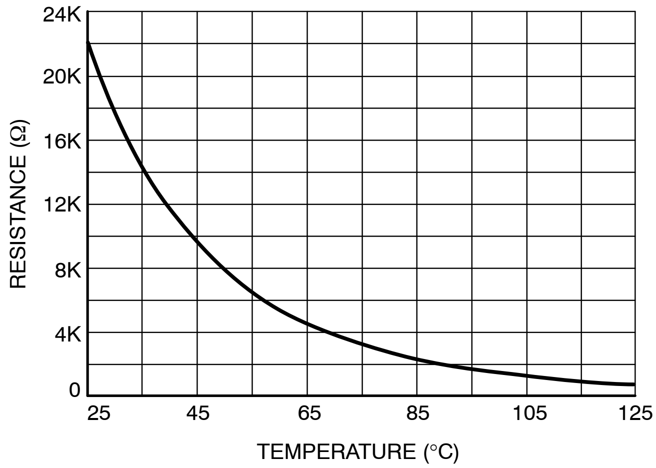


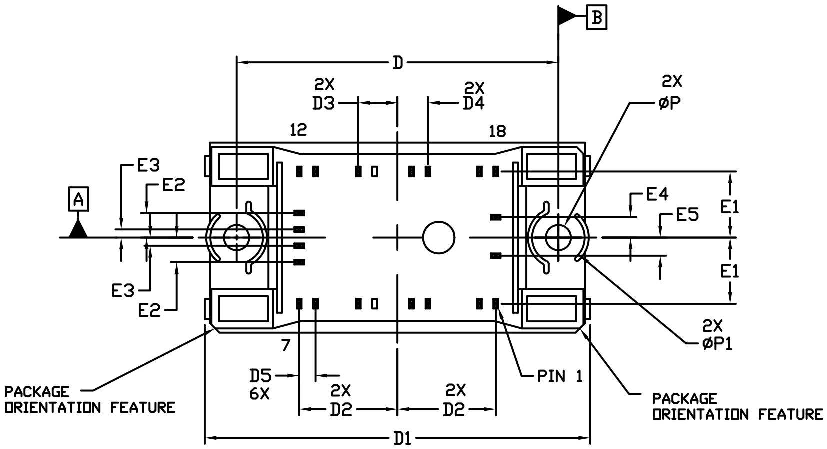
Figure 42. Thermistor Characteristics

ORDERING INFORMATION

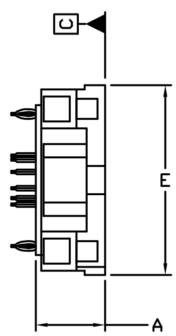
Orderable Part Number	Marking	Package	Shipping
NXH80T120L2Q0P2G	NXH80T120L2Q0P2G	Q0PACK − Case 180AA (Pb−Free and Halide−Free)	24 Units / Blister Tray
NXH80T120L2Q0S2G	NXH80T120L2Q0S2G	Q0PACK − Case 180AB (Pb−Free and Halide−Free)	24 Units / Blister Tray
NXH80T120L2Q0S2TG	NXH80T120L2Q0S2TG	Q0PACK − Case 180AB with pre−applied thermal interface material (TIM) (Pb−Free and Halide−Free)	24 Units / Blister Tray

PACKAGE DIMENSIONS

PIM20, 55x32.5 / Q0PACK
CASE 180AA
ISSUE D

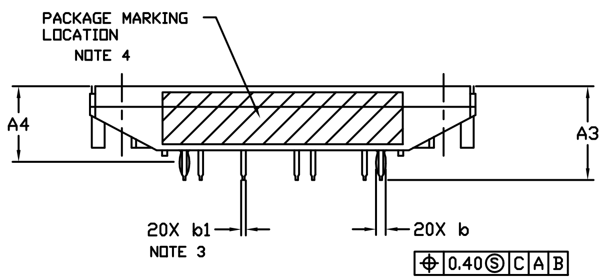


TOP VIEW

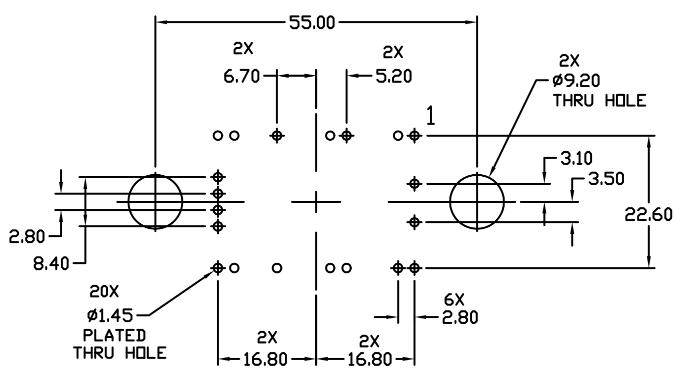


END VIEW

DIM	MILLIMETERS MIN.	NOM.	MAX.
A	11.33	11.83	12.33
A3	15.50	16.00	16.50
A4	12.88 BSC		
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	54.80	55.00	55.20
D1	65.70	67.90	70.10
D2	16.80 BSC		
D3	6.70 BSC		
D4	5.20 BSC		
D5	2.80 BSC		
E	32.30	32.50	32.70
E1	11.30 BSC		
E2	4.20 BSC		
E3	1.40 BSC		
E4	3.50 BSC		
E5	3.10 BSC		
P	4.10	4.30	4.50
P1	8.50	9.00	9.50



SIDE VIEW



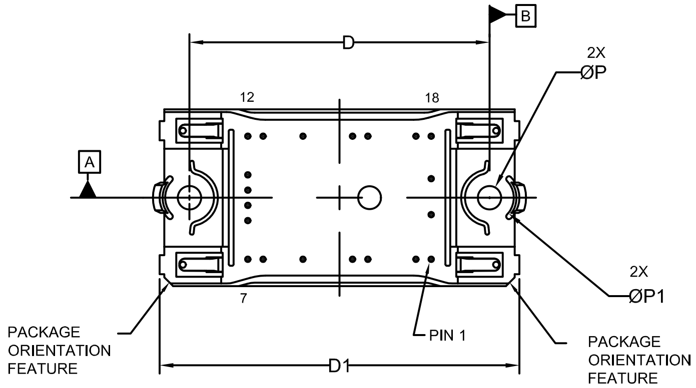
RECOMMENDED
MOUNTING PATTERN

NOTES:

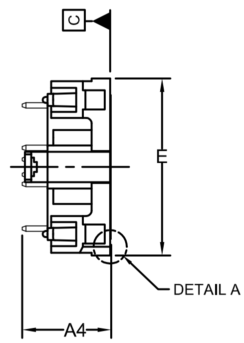
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
4. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

PACKAGE DIMENSIONS

PIM20, 55x32.5 / Q0PACK
CASE 180AB
ISSUE D

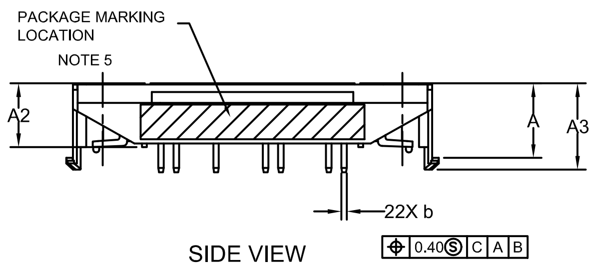


TOP VIEW

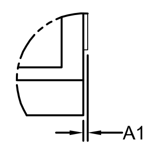


END VIEW

DIM	MILLIMETERS	
	MIN.	NOM.
A	13.50	13.90
A1	0.10	0.30
A2	11.50	11.90
A3	15.65	16.05
A4	16.35 REF	
b	0.95	1.05
D	54.80	55.20
D1	65.60	66.20
E	32.20	32.80
P	4.20	4.40
P1	8.90	9.10



SIDE VIEW



DETAIL A

NOTE 4

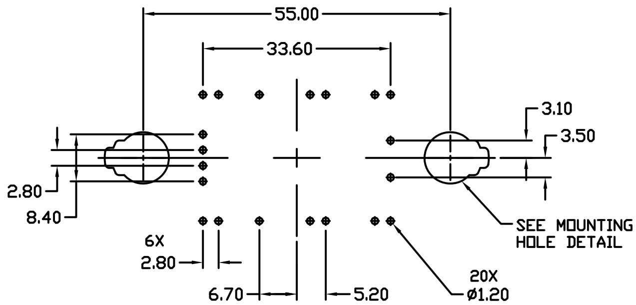
PIN	PIN POSITION X	PIN POSITION Y	PIN	PIN POSITION X	PIN POSITION Y
1	16.80	-11.30	11	-16.80	4.20
2	14.00	-11.30	12	-16.80	11.30
3	5.20	-11.30	13	-14.00	11.30
4	2.40	-11.30	14	-6.70	11.30
5	-6.70	-11.30	15	2.40	11.30
6	-14.00	-11.30	16	5.20	11.30
7	-16.80	-11.30	17	14.00	11.30
8	-16.80	-4.20	18	16.80	11.30
9	-16.80	-1.40	19	16.80	3.50
10	-16.80	1.40	20	16.80	-3.10

NOTES:

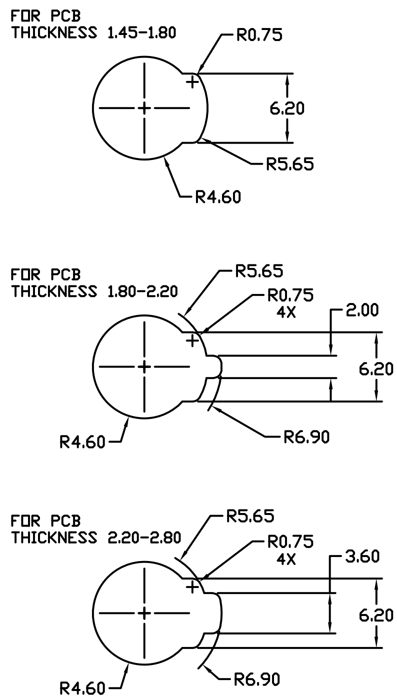
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

PACKAGE DIMENSIONS

PIM20, 55x32.5 / Q0PACK
CASE 180AB
ISSUE D



RECOMMENDED
MOUNTING PATTERN



MOUNTING HOLE DETAIL

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