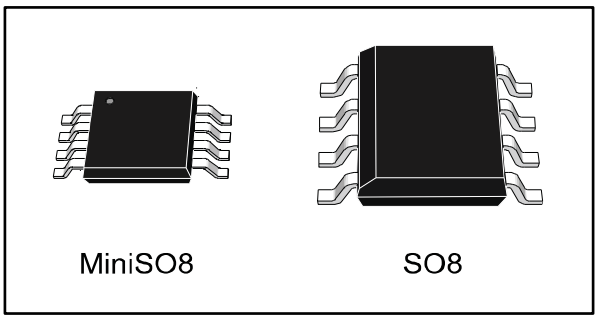
TSX7192

Low-power, precision, rail-to-rail, 9.0 MHz, 16 V operational amplifiers

Datasheet - production data



Features

- Low input offset voltage: 200 µV max.
- Rail-to-rail input and output
- Low current consumption: 850 µA max.
- Gain bandwidth product: 9 MHz
- Low supply voltage: 2.7 to 16 V
- Stable when used with Gain ≥ 10
- Low input bias current: 50 pA max.
- High ESD tolerance: 4 kV HBM
- Extended temp. range: -40 °C to 125 °C
- Automotive qualification

Related products

- See the TSX7191 for single op amp version
- See the TSX712 for lower speeds with similar precision
- See the TSX562 for low-power features
- See the TSX632 for micro-power features
- See the TSX922 for higher speeds

Applications

- Battery-powered instrumentation
- Instrumentation amplifier
- Active filtering
- High-impedance sensor interface
- Current sensing (high and low side)

Description

The TSX7192 dual, operational amplifier (op amp) offers high precision functioning with low input offset voltage down to a maximum of 200 µV at 25 °C. In addition, its rail-to-rail input and output functionality allows this product to be used on full range input and output without limitation. This is particularly useful for a low-voltage supply such as 2.7 V that the TSX7192 is able to operate with.

Thus, the TSX7192 has the great advantage of offering a large span of supply voltages, ranging from 2.7 V to 16 V. It can be used in multiple applications with a unique reference.

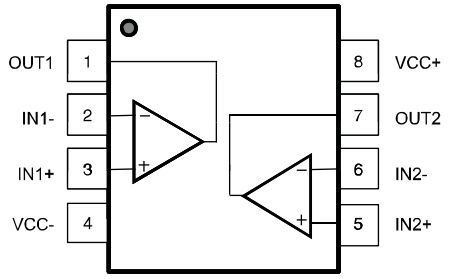
Low input bias current performance makes the TSX7192 perfect when used for signal conditioning in sensor interface applications. In addition, low-side and high-side current measurements can be easily made thanks to rail-to-rail functionality. The TSX7192 is a decompensated amplifier and must be used with a gain greater than 10 to ensure stability.

High ESD tolerance (4 kV HBM) and a wide temperature range are also good arguments to use the TSX7192 in the automotive market segment.

Contents

1 Package pin connections

Figure 1: Pin connections (top view)



MiniSO8 and SO8

2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	18	V
V_{id}	Differential input voltage (2)	$\pm V_{CC}$	mV
V_{in}	Input voltage	(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current (3)	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Maximum junction temperature	150	
ESD	HBM: human body model (4)	4000	V
	MM: machine model (5)	100	
	CDM: charged device model (6)	1500	
	Latch-up immunity	200	mA

Notes:

(1)All voltage values, except the differential voltage are with respect to the network ground terminal.

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. See *Section 4.7* for precautions to follow when using the TSX7192 with high differential input voltage.

(3)Input current must be limited by a resistor in series with the inputs.

(4)According to JEDEC standard JESD22-A114F.

(5)According to JEDEC standard JESD22-A115A.

(6)According to ANSI/ESD STM5.3.1.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{oper}	Operating free air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3: Electrical characteristics at VCC+ = 4 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 ° C, and RL > 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	T = 25 °C			200	µV
		$T_{min} < T_{op} < 85$ °C			365	
		$T_{min} < T_{op} < 125$ °C			450	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		1		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	$V_{out} = V_{CC}/2$		1	50	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current (1)	$V_{out} = V_{CC}/2$		1	50	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 4.1 V, $V_{out} = V_{CC}/2$	80	98		dB
		$T_{min} < T_{op} < T_{max}$	78			
		V_{icm} = -0.1 to 2 V, $V_{out} = V_{CC}/2$	91	103		
		$T_{min} < T_{op} < T_{max}$	86			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 to 3.7 V	110	136		
		$T_{min} < T_{op} < T_{max}$	96			
		R_L= 10 kΩ, V_{out} = 0.2 to 3.8 V	110	140		
		$T_{min} < T_{op} < T_{max}$	96			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L= 2 kΩ to $V_{CC}/2$		28	50	mV
		$T_{min} < T_{op} < T_{max}$			60	
		R_L= 10 kΩ to $V_{CC}/2$		6	15	
		$T_{min} < T_{op} < T_{max}$			20	
V_{OL}	Low level output voltage	R_L= 2 kΩ to $V_{CC}/2$		23	50	
		$T_{min} < T_{op} < T_{max}$			60	
		R_L= 10 kΩ to $V_{CC}/2$		5	15	
		$T_{min} < T_{op} < T_{max}$			20	
I_{out}	I_{sink}	$V_{out} = V_{CC}$	25	37		mA
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	35	45		
		$T_{min} < T_{op} < T_{max}$	20			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}/2$		570	800	µA
		$T_{min} < T_{op} < T_{max}$			900	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	5	7.7		MHz
ϕm	Phase margin	Gain = 10, R_L = 10 kΩ, C_L = 100 pF		42		Degrees
SRn	Negative slew rate	Av = 10, V_{out} = 3 V_{PP}, 10 % to 90 %	1.3	2.3		V/µs
		T_{min} < T_{op} < T_{max}	1.0			
SRp	Positive slew rate	Av = 10, V_{out} = 3 V_{PP}, 10 % to 90 %	1.5	2.5		
		T_{min} < T_{op} < T_{max}	1.1			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f =1 kHz, Av = 10, R_L= 10 kΩ, BW = 22 kHz, V_{out} = 3V_{PP}		0.003		%

Notes:

(1)Maximum values are guaranteed by design.

(2)Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 4.6*).

Table 4: Electrical characteristics at VCC+ = 10 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL > 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	T = 25 °C			200	µV
		T_{min} < T_{op} < 85 °C			365	
		T_{min} < T_{op} < 125 °C			450	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		25		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	V_{out} = V_{CC}/2		1	50	pA
		T_{min} < T_{op} < T_{max}			200	
I_{io}	Input offset current (1)	V_{out} = V_{CC}/2		1	50	
		T_{min} < T_{op} < T_{max}			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 10.1 V, V_{out} = V_{CC}/2	88	100		dB
		T_{min} < T_{op} < T_{max}	84			
		V_{icm} = -0.1 to 8 V, V_{out} = V_{CC}/2	98	106		
		T_{min} < T_{op} < T_{max}	92			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 to 9.7 V	110	140		
		T_{min} < T_{op} < T_{max}	100			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.2 to 9.8 V	110			dB
		$T_{min} < T_{op} < T_{max}$	100			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L= 2 kΩ to V_{CC}/2		45	70	mV
		$T_{min} < T_{op} < T_{max}$			80	
		R_L= 10 kΩ to V_{CC}/2		10	30	
		$T_{min} < T_{op} < T_{max}$			40	
V_{OL}	Low level output voltage	R_L= 2 kΩ to V_{CC}/2		42	70	
		$T_{min} < T_{op} < T_{max}$			80	
		R_L= 10 kΩ to V_{CC}/2		9	30	
		$T_{min} < T_{op} < T_{max}$			40	
I_{out}	I_{sink}	$V_{out} = V_{CC}$	30	39		mA
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	50	69		
		$T_{min} < T_{op} < T_{max}$	40			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}/2$		630	850	µA
		$T_{min} < T_{op} < T_{max}$			1000	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	5	9		MHz
ϕm	Phase margin	G = 10, R_L = 10 kΩ, C_L = 100 pF		48		Degrees
SRn	Negative slew rate	Av = 10, V_{out} = 8 V_{PP}, 10 % to 90 %	1.3	2.3		V/µs
		$T_{min} < T_{op} < T_{max}$	1.0			
SRp	Positive slew rate	Av = 10, V_{out} = 8 V_{PP}, 10 % to 90 %	1.5	2.5		
		$T_{min} < T_{op} < T_{max}$	1.1			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 10, R_L= 10 kΩ, BW = 22 kHz, V_{out} = 9 V_{PP}		0.0001		%

Notes:

(1)Maximum values are guaranteed by design.

(2)Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 4.6*).

Table 5: Electrical characteristics at VCC+ = 16 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL > 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	T = 25 °C			200	µV
		$T_{min} < T_{op} < 85$ °C			365	
		$T_{min} < T_{op} < 125$ °C			450	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		500		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	$V_{out} = V_{CC}/2$		1	50	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current (1)	$V_{out} = V_{CC}/2$		1	50	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = -0.1 to 16.1 V, $V_{out} = V_{CC}/2$	94	107		dB
		$T_{min} < T_{op} < T_{max}$	90			
		V_{icm} = -0.1 to 14 V, $V_{out} = V_{CC}/2$	100	107		
		$T_{min} < T_{op} < T_{max}$	90			
SVRR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 4 to 16 V	100	131		
		$T_{min} < T_{op} < T_{max}$	90			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 to 15.7 V	110	146		
		$T_{min} < T_{op} < T_{max}$	100			
		R_L= 10 kΩ, V_{out} = 0.2 to 15.8 V	110	149		
		$T_{min} < T_{op} < T_{max}$	100			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L= 2 kΩ		100	130	mV
		$T_{min} < T_{op} < T_{max}$			150	
		R_L= 10 kΩ		16	40	
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low level output voltage	R_L= 2 kΩ		70	130	
		$T_{min} < T_{op} < T_{max}$			150	
		R_L= 10 kΩ		15	40	
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	$V_{out} = V_{CC}$	30	40		mA
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	50	68		
		$T_{min} < T_{op} < T_{max}$	45			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}/2$		660	900	µA
		$T_{min} < T_{op} < T_{max}$			1000	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	5	8.5		MHz
ϕm	Phase margin	G = 10, R_L = 10 kΩ, C_L = 100 pF		51		Degrees
SRn	Negative slew rate	Av = 10, V_{out} = 10 V_{PP}, 10 % to 90 %	1.5	2.4		V/µs
		T_{min} < T_{op} < T_{max}	1.1			
SRp	Positive slew rate	Av = 10, V_{out} = 10 V_{PP}, 10 % to 90 %	1.5	2.5		
		T_{min} < T_{op} < T_{max}	1.1			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + Noise	f = 1 kHz, Av = 10, R_L= 10 kΩ, BW = 22 kHz, V_{out} = 10 V_{PP}		0.0001		%

Notes:

(1)Maximum values are guaranteed by design.

(2)Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 4.6*).

Figure 2: Supply current vs. supply voltage

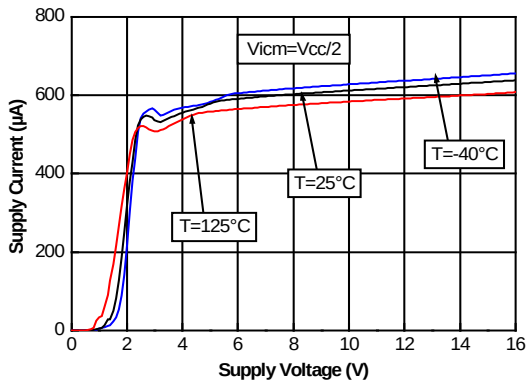


Figure 3: Input offset voltage distribution at VCC = 16 V

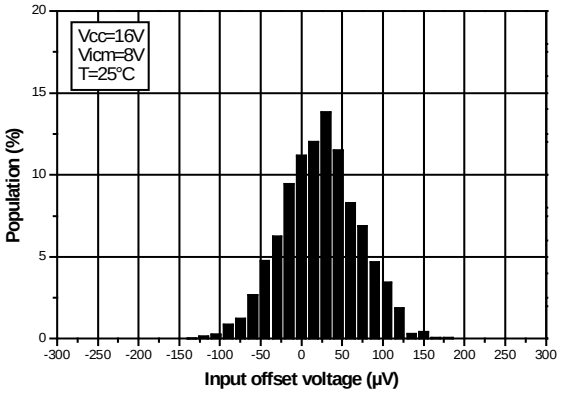


Figure 4: Input offset voltage distribution at VCC = 4 V

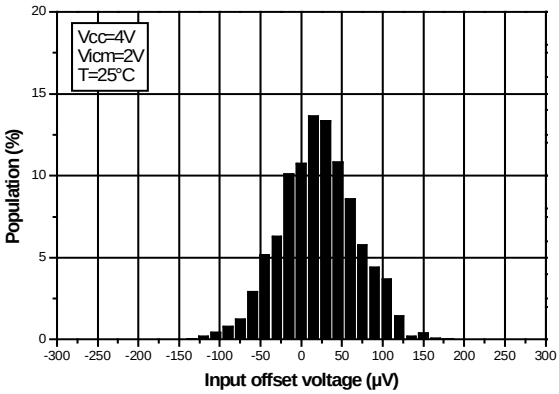


Figure 5: Input offset voltage vs. temperature at VCC = 16 V

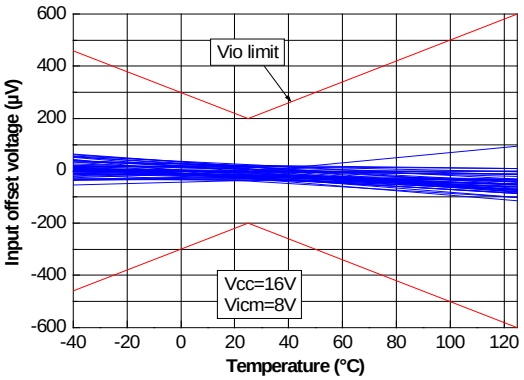


Figure 6: Input offset voltage drift population

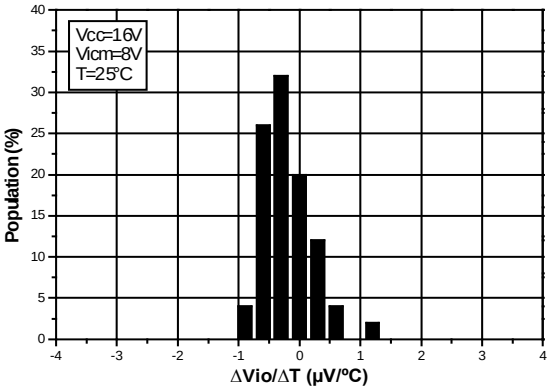


Figure 7: Input offset voltage vs. supply voltage at VICM = 0 V

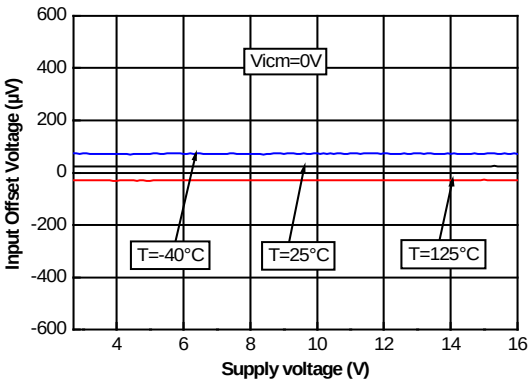


Figure 8: Input offset voltage vs. common mode voltage at VCC = 2.7 V

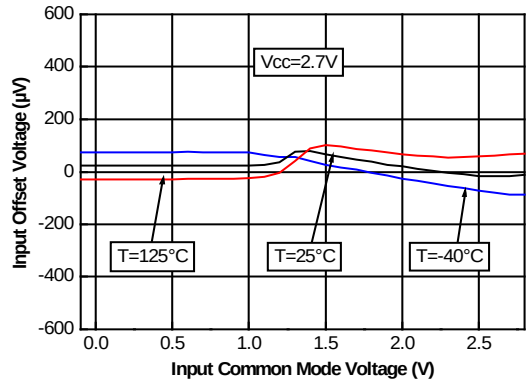


Figure 9: Input offset voltage vs. common mode voltage at VCC = 16 V

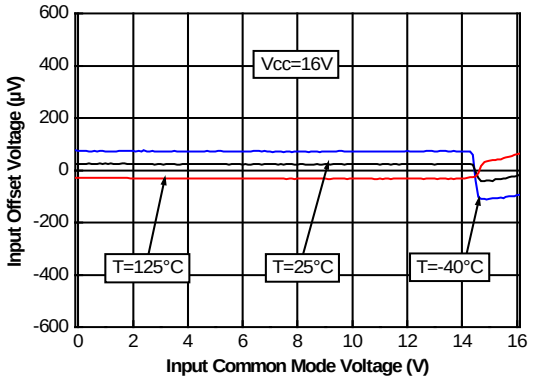


Figure 10: Output current vs. output voltage at VCC = 2.7 V

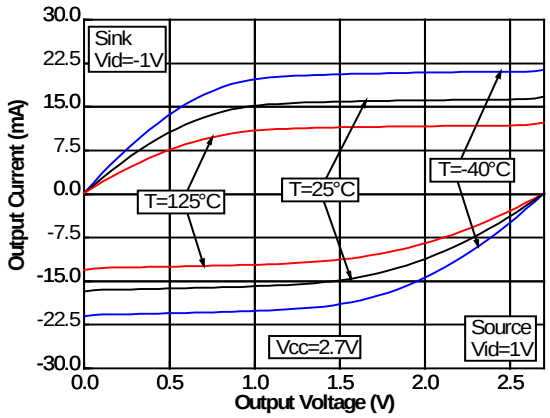


Figure 11: Output current vs. output voltage at VCC = 16 V

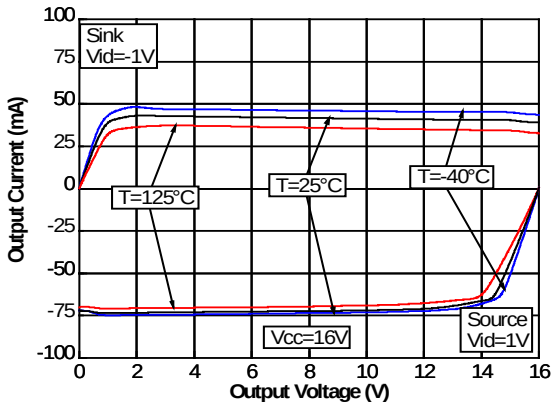


Figure 12: Output low voltage vs. supply voltage

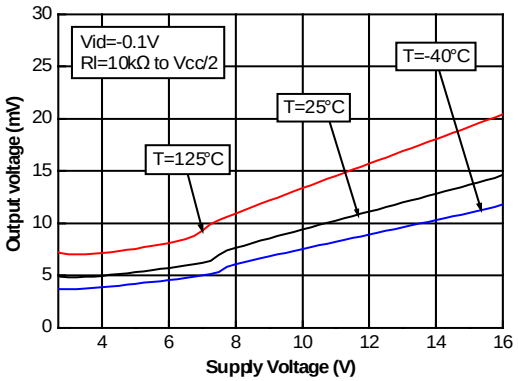


Figure 13: Output high voltage (drop from VCC+) vs. supply voltage

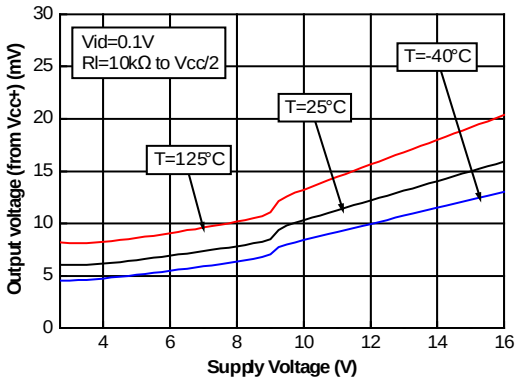


Figure 14: Output voltage vs. input voltage close to the rail at VCC = 16 V

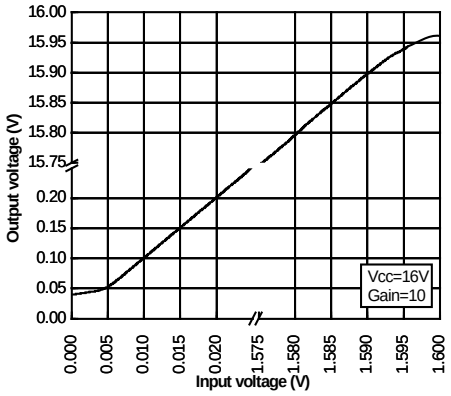


Figure 15: Slew rate vs. supply voltage

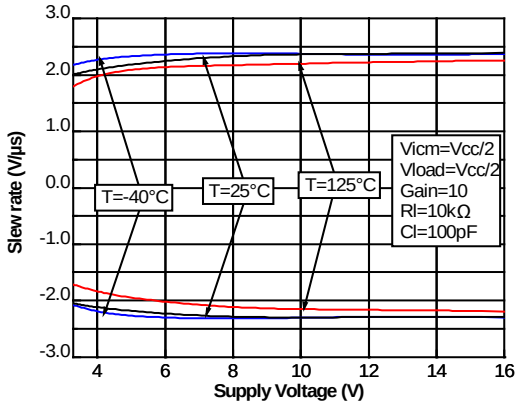


Figure 16: Negative slew rate at VCC = 16 V

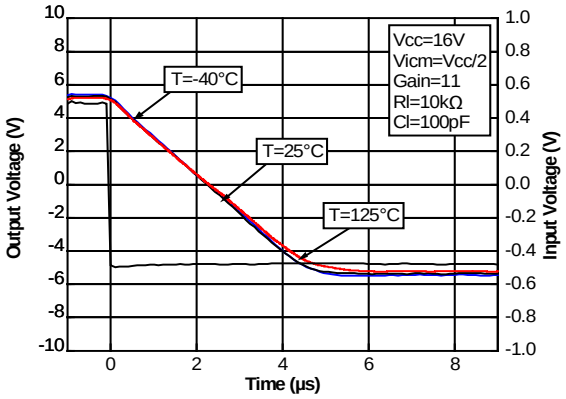


Figure 17: Positive slew rate at VCC = 16 V

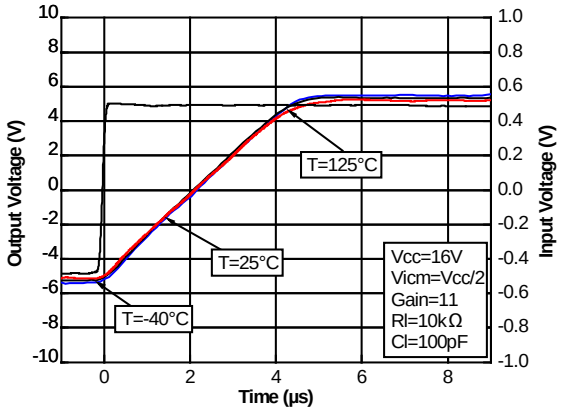


Figure 18: Response to a small input voltage step

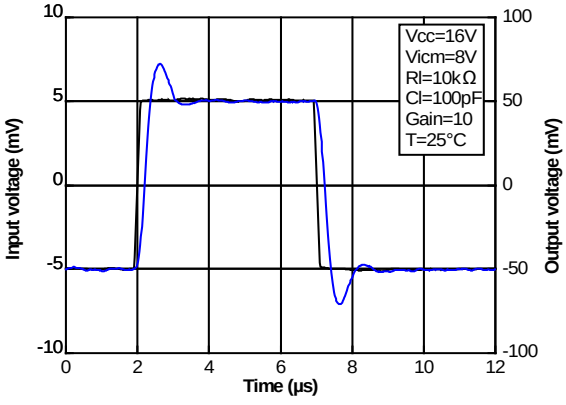


Figure 19: Recovery behavior after a negative step on the input

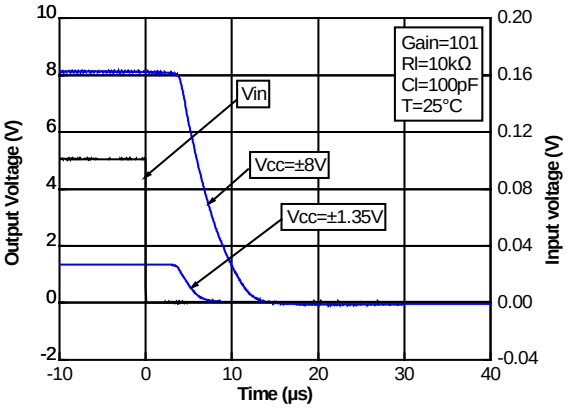


Figure 20: Recovery behavior after a positive step on the input

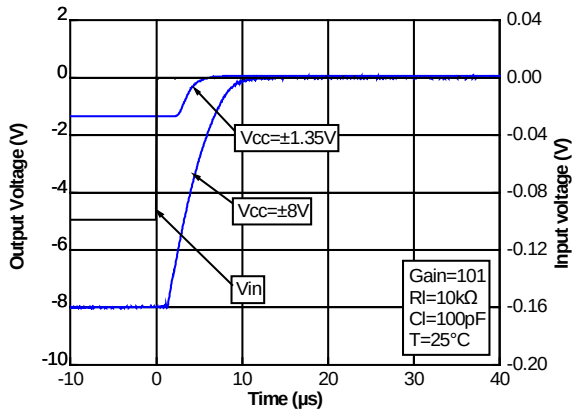


Figure 21: Bode diagram at VCC = 2.7 V

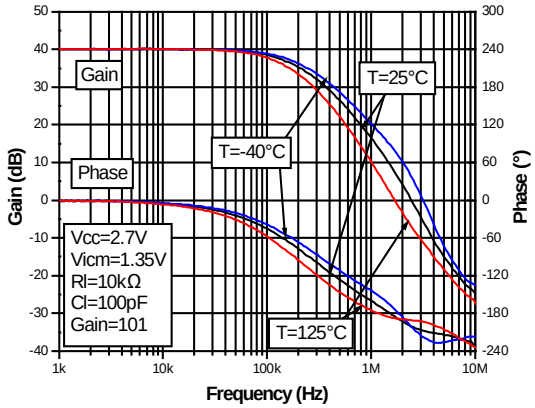


Figure 22: Bode diagram at VCC = 16 V

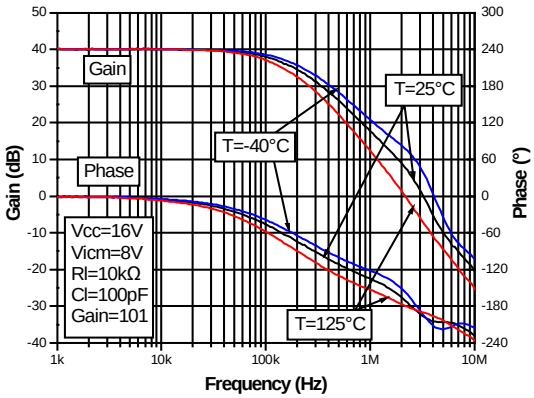


Figure 23: Power supply rejection ratio (PSRR) vs. frequency

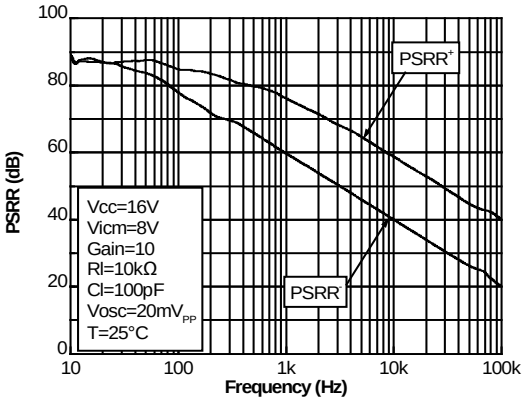


Figure 24: Output overshoot vs. capacitive load

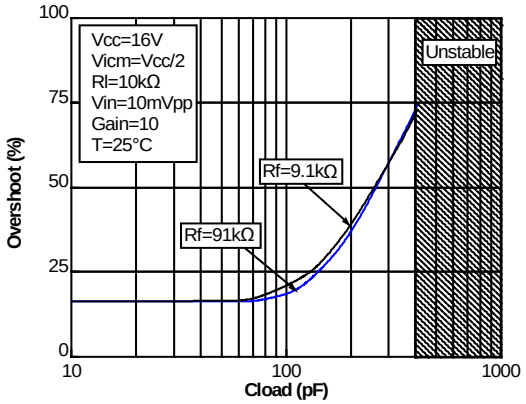


Figure 25: Output impedance vs. frequency in closed loop configuration

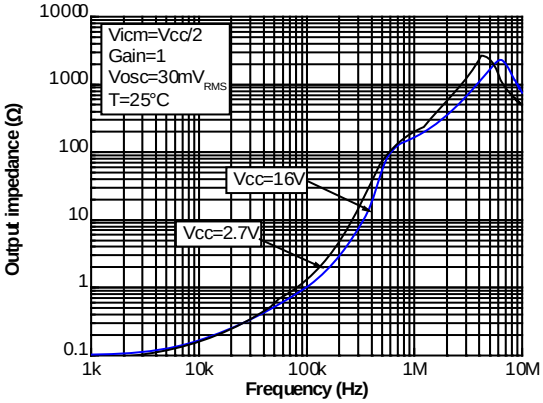


Figure 26: THD + N vs. frequency

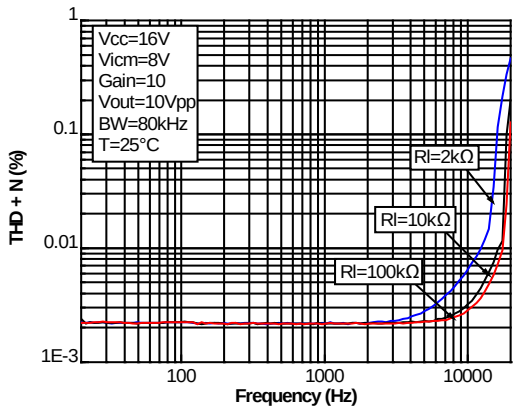


Figure 27: THD + N vs. output voltage

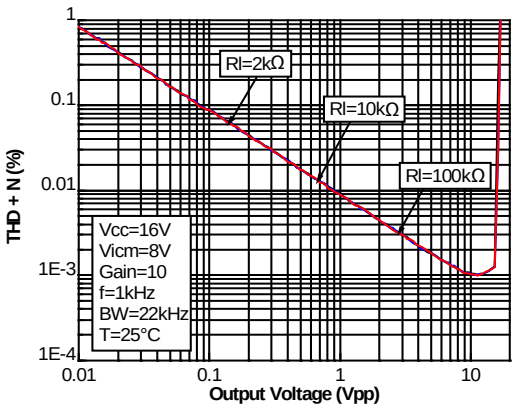


Figure 28: Noise vs. frequency

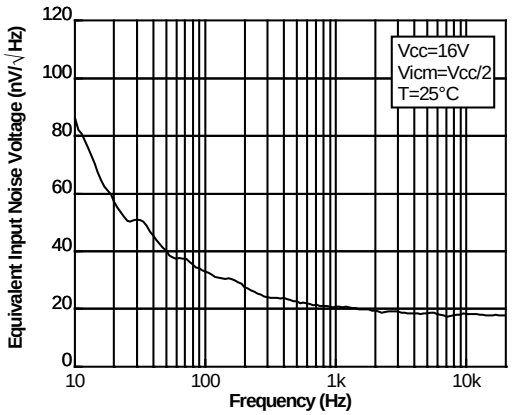
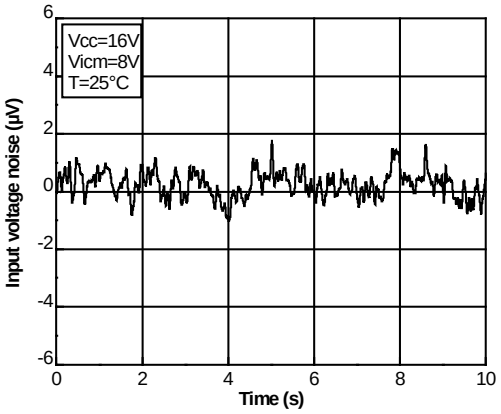


Figure 29: 0.1 to 10Hz noise



4 Application information

4.1 Operating voltages

The TSX7192 device can operate from 2.7 to 16 V. The parameters are fully specified for 4 V, 10 V, and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 °C.

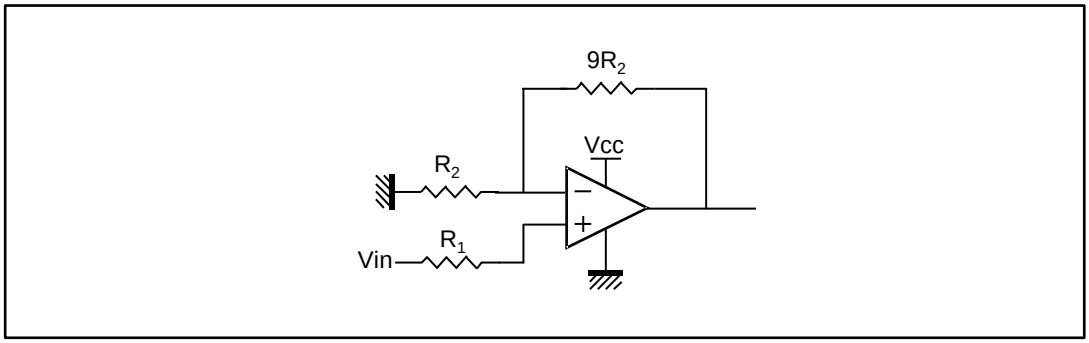
4.2 Input pin voltage ranges

The TSX7192 device has internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this over current can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as described in *Figure 30*.

Figure 30: Input current limitation



4.3 Rail-to-rail input

The TSX7192 device has a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V.

4.4 Rail-to-rail output

The operational amplifier output levels can go close to the rails: to a maximum of 40 mV above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

4.5 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 125 °C.

The TSX7192 datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

4.6 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\,\text{h} \times 12\ \text{months} / (24\,\text{h} \times 365.25\ \text{days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.7 High values of input differential voltage

In a closed loop configuration, which represents the typical use of an op amp, the input differential voltage is low (close to V_{io}). However, some specific conditions can lead to higher input differential values, such as:

- operation in an output saturation state
- operation at speeds higher than the device bandwidth, with output voltage dynamics limited by slew rate.
- use of the amplifier in a comparator configuration, hence in open loop

Use of the TSX7191 in comparator configuration, especially combined with high temperature and long duration can create a permanent drift of V_{io}.

4.8 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, the unity gain configuration is the worst case for stability and the ability to drive large capacitive loads.

Figure 31 shows the serial resistor that must be added to the output, to make a system stable. *Figure 32* shows the test configuration using an isolation resistor, Riso.

Figure 31: Stability criteria with a serial resistor at different supply voltages

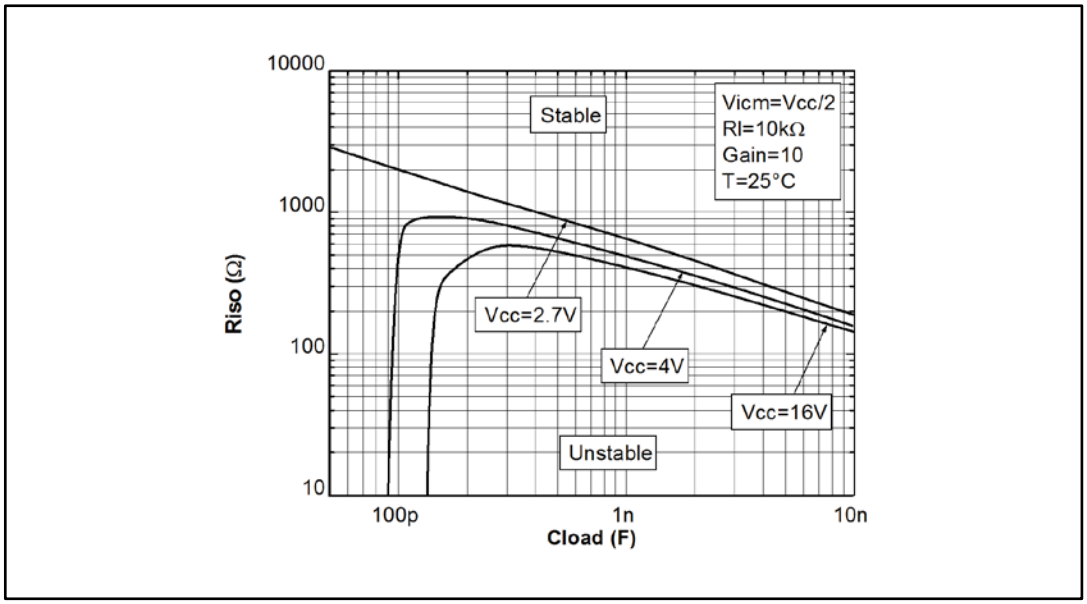
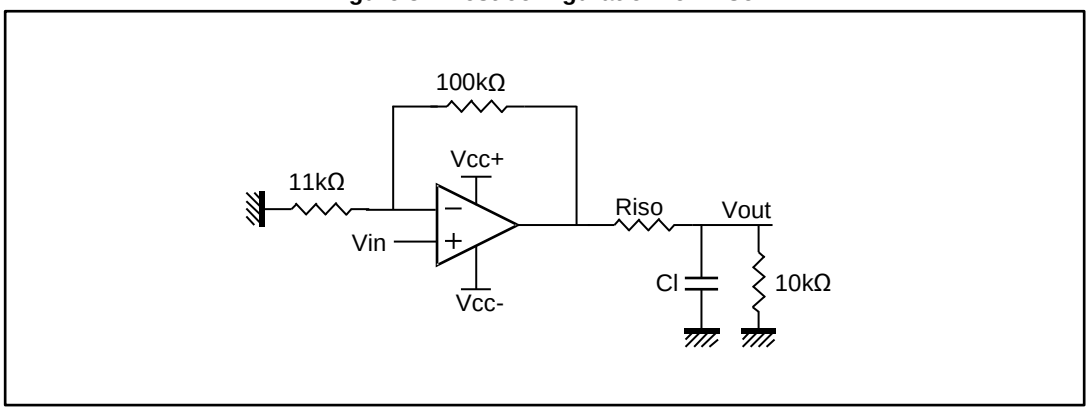


Figure 32: Test configuration for Riso



4.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB, tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

4.10 Optimized application recommendation

It is recommended to place a 22 nF capacitor as close as possible to the supply pin. A good decoupling will help to reduce electromagnetic interference impact.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 MiniSO8 package information

Figure 33: MiniSO8 package outline

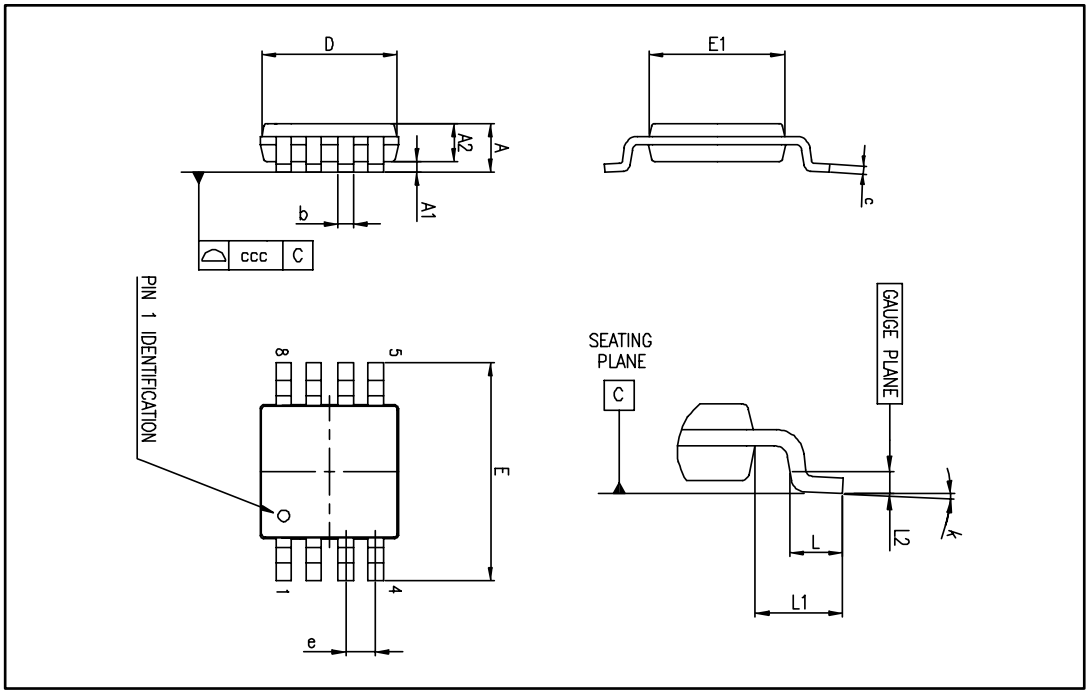


Table 6: MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.2 SO8 package information

Figure 34: SO8 package outline

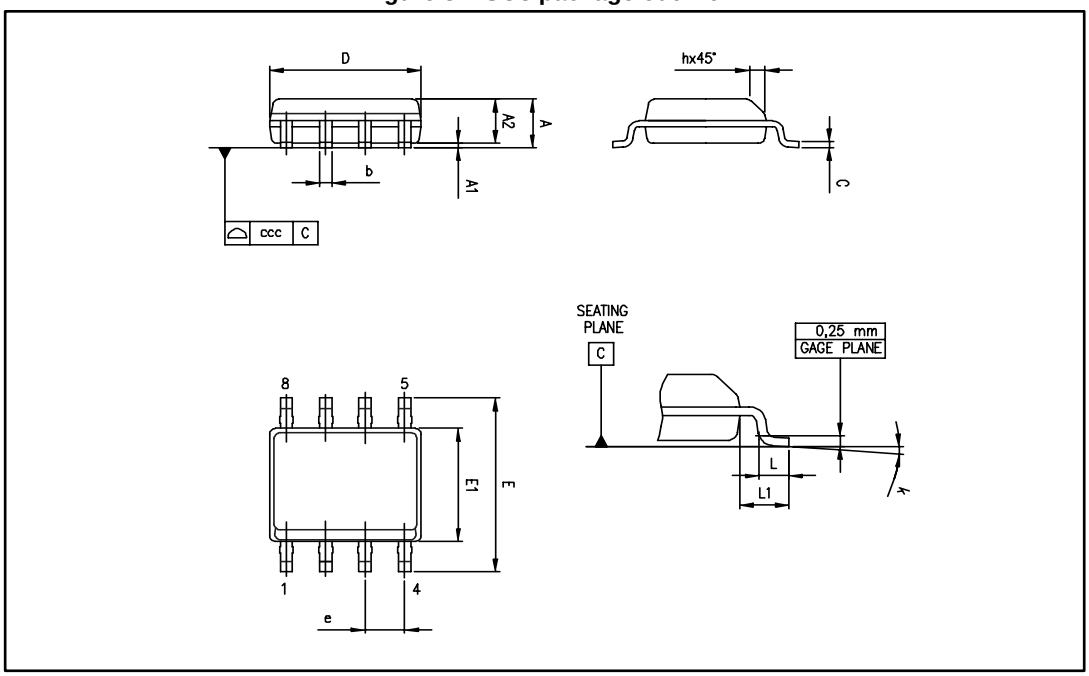


Table 7: SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

6 Ordering information

Table 8: Order codes

Order code	Temperature range	Package	Packaging	Marking
TSX7192IDT	-40 to +125 °C	SO8	Tape and reel	TSX7192
TSX7192IST		MiniSO8		K210
TSX7192IYDT (1)	-40 to +125 °C, automotive grade	SO8		TSX7192Y
TSX7192IYST (1)		MiniSO8		K213

Notes:

(1)Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

7 Revision history

Table 9: Document revision history

Date	Revision	Changes
06-Mar-2015	1	Initial release

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