

MC74AC74, MC74ACT74

Dual D-Type Positive Edge-Triggered Flip-Flop

The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

Features

- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs
- These are Pb-Free Devices

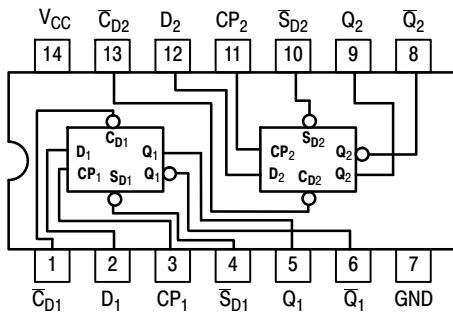


Figure 1. Pinout: 14-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

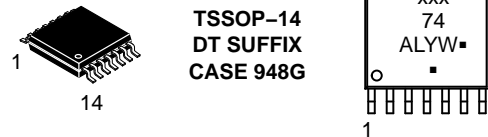
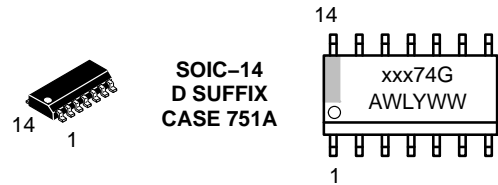
| PIN | FUNCTION |
|---|---------------------|
| D ₁ , D ₂ | Data Inputs |
| CP ₁ , CP ₂ | Clock Pulse Inputs |
| \bar{C}_D1 , \bar{C}_D2 | Direct Clear Inputs |
| \bar{S}_D1 , \bar{S}_D2 | Direct Set Inputs |
| Q ₁ , \bar{Q}_1 , Q ₂ , \bar{Q}_2 | Outputs |



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MARKING DIAGRAMS



xxx = AC or ACT
 A = Assembly Location
 WL or L = Wafer Lot
 Y = Year
 WW or W = Work Week
 G or ■ = Pb-Free Package



(Note: Microdot may be in either location)


ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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TRUTH TABLE (Each Half)

| Inputs | | | | Outputs | |
|-------------|-------------|---|---|---------|-------------|
| \bar{S}_D | \bar{C}_D | CP | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H |  | H | H | L |
| H | H |  | L | L | H |
| H | H | L | X | Q_0 | \bar{Q}_0 |

NOTE: H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial;
 = LOW-to-HIGH Clock Transition
 $Q_0(\bar{Q}_0)$ = Previous Q(\bar{Q}) before LOW-to-HIGH Transition of Clock

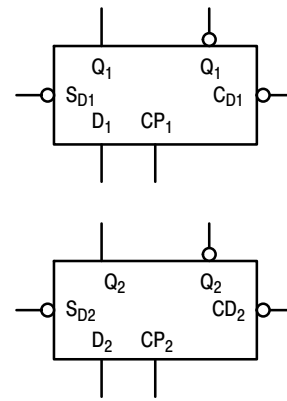
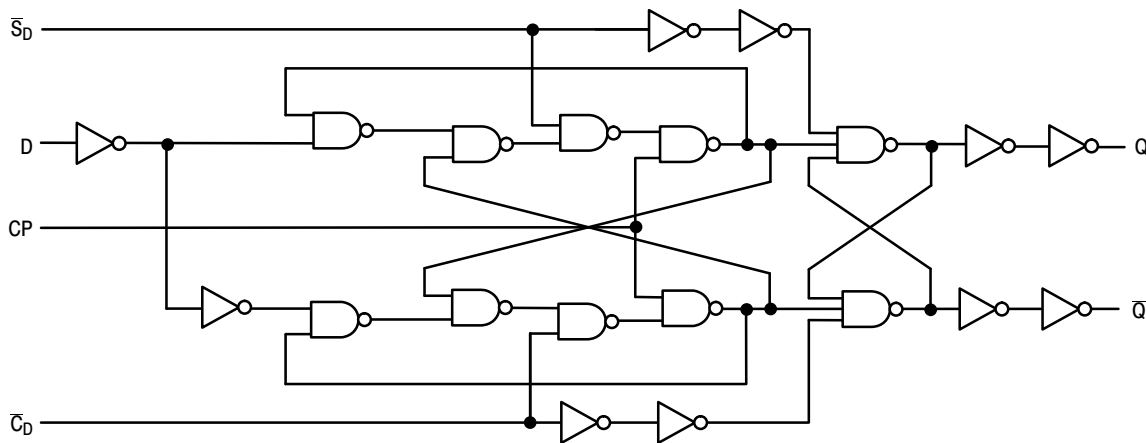


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MC74AC74, MC74ACT74

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|---|---|------------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _I | DC Input Voltage | -0.5 ≤ V _I ≤ V _{CC} + 0.5 | V |
| V _O | DC Output Voltage (Note 1) | -0.5 ≤ V _O ≤ V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | ±20 | mA |
| I _{OK} | DC Output Diode Current | ±50 | mA |
| I _O | DC Output Sink/Source Current | ±50 | mA |
| I _{CC} | DC Supply Current per Output Pin | ±50 | mA |
| I _{GND} | DC Ground Current per Output Pin | ±50 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction temperature under Bias | +150 | °C |
| θ _{JA} | Thermal Resistance (Note 2) | SOIC TSSOP 125 170 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C | SOIC TSSOP 125 170 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) > 2000 > 200 > 1000 | V |
| I _{Latch-Up} | Latch-Up Performance | Above V _{CC} and Below GND at 85°C (Note 6) | ±100 mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit | |
|------------------------------------|--|-------------------------|-----|-----------------|------|------|
| V _{CC} | Supply Voltage | 'AC | 2.0 | 5.0 | 6.0 | V |
| | | 'ACT | 4.5 | 5.0 | 5.5 | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Ref. to GND) | 0 | - | V _{CC} | V | |
| t _r , t _f | Input Rise and Fall Time (Note) 'AC Devices except Schmitt Inputs | V _{CC} @ 3.0 V | - | 150 | - | ns/V |
| | | V _{CC} @ 4.5 V | - | 40 | - | |
| | | V _{CC} @ 5.5 V | - | 25 | - | |
| t _r , t _f | Input Rise and Fall Time (Note) 'ACT Devices except Schmitt Inputs | V _{CC} @ 4.5 V | - | 10 | - | ns/V |
| | | V _{CC} @ 5.5 V | - | 8.0 | - | |
| T _J | Junction Temperature (PDIP) | - | - | 140 | °C | |
| T _A | Operating Ambient Temperature Range | -40 | 25 | 85 | °C | |
| I _{OH} | Output Current – High | - | - | -24 | mA | |
| I _{OL} | Output Current – Low | - | - | 24 | mA | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | 74AC | | 74AC | | Unit | Conditions |
|------------------|-----------------------------------|---------------------|------------------------|-------------------|---------------------------------|----|---|------------|
| | | | T _A = +25°C | | T _A = -40°C to +85°C | | | |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | I _{OUT} = -50 μA | |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | - | 2.56 | 2.46 | V | *V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA | |
| | | 4.5 | - | 3.86 | 3.76 | | | |
| | | 5.5 | - | 4.86 | 4.76 | | | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | I _{OUT} = 50 μA | |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | - | 0.36 | 0.44 | V | *V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA | |
| | | 4.5 | - | 0.36 | 0.44 | | | |
| | | 5.5 | - | 0.36 | 0.44 | | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | - | ±0.1 | ±1.0 | μA | V _I = V _{CC} , GND | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | - | - | 75 | mA | V _{OLD} = 1.65 V Max | |
| I _{OHD} | | 5.5 | - | - | -75 | mA | V _{OHD} = 3.85 V Min | |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | - | 4.0 | 40 | μA | V _{IN} = V _{CC} or GND | |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

| Symbol | Parameter | V _{CC} * (V) | 74AC | | | 74AC | | Unit | Fig. No. |
|------------------|---|-----------------------|--|------|------|---|------|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 | 100 | 125 | - | 95 | - | MHz | 3-3 |
| | | 5.0 | 140 | 160 | - | 125 | - | | |
| t _{PLH} | Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n | 3.3 | 5.0 | 8.0 | 12.5 | 4.0 | 13.0 | ns | 3-6 |
| | | 5.0 | 3.5 | 6.0 | 9.0 | 3.0 | 10.0 | | |
| t _{PHL} | Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n | 3.3 | 4.0 | 10.5 | 12.0 | 3.5 | 13.5 | ns | 3-6 |
| | | 5.0 | 3.0 | 8.0 | 9.5 | 2.5 | 10.5 | | |
| t _{PLH} | Propagation Delay C _{Pn} to Q _n or Q _n | 3.3 | 4.5 | 8.0 | 13.5 | 4.0 | 16.0 | ns | 3-6 |
| | | 5.0 | 3.5 | 6.0 | 10.0 | 3.0 | 10.5 | | |
| t _{PHL} | Propagation Delay C _{Pn} to Q _n or Q _n | 3.3 | 3.5 | 8.0 | 14.0 | 3.5 | 14.5 | ns | 3-6 |
| | | 5.0 | 2.5 | 6.0 | 10.0 | 2.5 | 10.5 | | |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

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AC OPERATING REQUIREMENTS

| Symbol | Parameter | V _{CC} * (V) | 74AC | | 74AC | | Unit | Fig. No. |
|------------------|--|--------------------------|--|--------------------|--|----|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _s | Set-up Time, HIGH or LOW D _n to CP _n | 3.3 | 1.5 | 4.0 | 4.5 | ns | 3-9 | |
| | | 5.0 | 1.0 | 3.0 | 3.0 | | | |
| t _h | Hold Time, HIGH or LOW D _n to CP _n | 3.3 | -2.0 | 0.5 | 0.5 | ns | 3-9 | |
| | | 5.0 | -1.5 | 0.5 | 0.5 | | | |
| t _w | C _{Pn} or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width | 3.3 | 3.0 | 5.5 | 7.0 | ns | 3-6 | |
| | | 5.0 | 2.5 | 4.5 | 5.0 | | | |
| t _{rec} | Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP | 3.3 | -2.5 | 0 | 0 | ns | 3-9 | |
| | | 5.0 | -2.0 | 0 | 0 | | | |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC74, MC74ACT74

DC CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | 74ACT | | 74ACT | | Unit | Conditions |
|-------------------|--|------------------------|------------------------|-------------------|---------------------------------------|----|---|------------|
| | | | T _A = +25°C | | T _A = -40°C to +85°C | | | |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | I _{OUT} = -50 μA | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | - | 3.86 | 3.76 | V | *V _{IN} = V _{IL} or V _{IH} -24 mA | |
| | | 5.5 | - | 4.86 | 4.76 | | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | I _{OUT} = 50 μA | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | - | 0.36 | 0.44 | V | *V _{IN} = V _{IL} or V _{IH} 24 mA | |
| | | 5.5 | - | 0.36 | 0.44 | | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | - | ±0.1 | ±1.0 | μA | V _I = V _{CC} , GND | |
| ΔI _{CCT} | Additional Max. I _{CC} /Input | 5.5 | 0.6 | - | 1.5 | mA | V _I = V _{CC} - 2.1 V | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | - | - | 75 | mA | V _{OLD} = 1.65 V Max | |
| I _{OHD} | | 5.5 | - | - | -75 | mA | V _{OHD} = 3.85 V Min | |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | - | 4.0 | 40 | μA | V _{IN} = V _{CC} or GND | |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | | 74ACT | | Unit | Fig. No. |
|------------------|---|--------------------------|--|-----|------|--|------|------|-------------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 145 | 210 | - | 125 | - | MHz | 3-3 |
| t _{PLH} | Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n | 5.0 | 3.0 | 5.5 | 9.5 | 2.5 | 10.5 | ns | 3-6 |
| t _{PHL} | Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n | 5.0 | 3.0 | 6.0 | 10.0 | 3.0 | 11.5 | ns | 3-6 |
| t _{PLH} | Propagation Delay C _{Pn} to Q _n or Q _n | 5.0 | 4.0 | 7.5 | 11.0 | 4.0 | 13.0 | ns | 3-6 |
| t _{PHL} | Propagation Delay C _{Pn} to Q _n or Q _n | 5.0 | 3.5 | 6.0 | 10.0 | 3.0 | 11.5 | ns | 3-6 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC74, MC74ACT74

AC OPERATING REQUIREMENTS

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | 74ACT | | Unit | Fig. No. |
|------------------|--|--------------------------|--|--------------------|--|----|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _s | Set-up Time, HIGH or LOW D _n to CP _n | 5.0 | 1.0 | 3.0 | 3.5 | ns | 3-9 | |
| t _h | Hold Time, HIGH or LOW D _n to CP _n | 5.0 | -0.5 | 1.0 | 1.0 | ns | 3-9 | |
| t _w | C _{Pn} or C _{Dn} or S _{Dn} Pulse Width | 5.0 | 3.0 | 5.0 | 6.0 | ns | 3-6 | |
| t _{rec} | Recovery Time C _{Dn} or S _{Dn} to CP | 5.0 | -2.5 | 0 | 0 | ns | 3-9 | |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

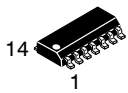
| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|-----------------|-------------------------------|--------------|------|-------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0 V |
| C _{PD} | Power Dissipation Capacitance | 35 | pF | V _{CC} = 5.0 V |

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-----------------------|------------------|
| MC74AC74DG | SOIC-14 (Pb-Free) | 55 Units/Rail |
| MC74AC74DR2G | SOIC-14 (Pb-Free) | 2500/Tape & Reel |
| MC74AC74DTR2G | TSSOP-14 (Pb-Free) | 2500/Tape & Reel |
| MC74ACT74DG | SOIC-14 (Pb-Free) | 55 Units/Rail |
| MC74ACT74DR2G | SOIC-14 (Pb-Free) | 2500/Tape & Reel |
| MC74ACT74DTR2G | TSSOP-14 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

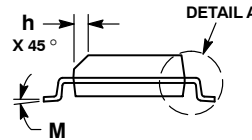
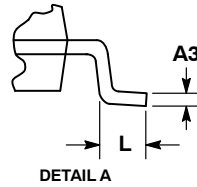
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

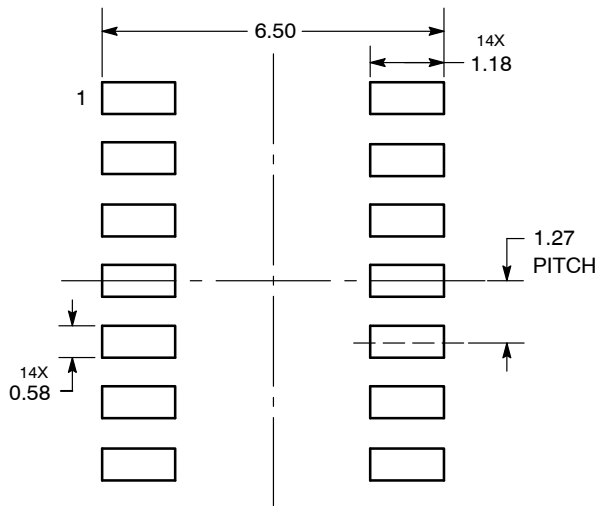
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

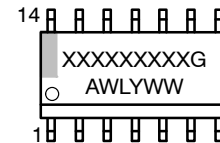
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

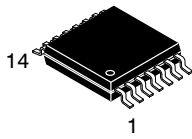
STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

| | | |
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| DESCRIPTION: | SOIC-14 NB | PAGE 2 OF 2 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

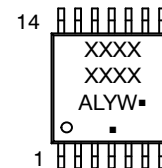


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

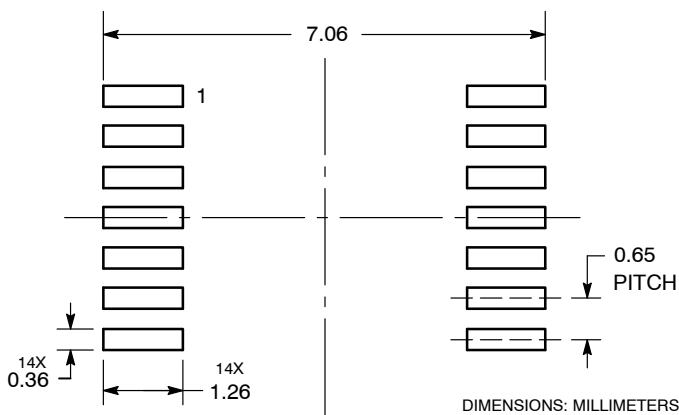


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



| | | |
|-------------------------|--------------------|--|
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