HARRIS SEMICONDUCTOR
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IH5009-5012, 5014, 5016-5020, 5022, 5024
Virtual Ground Analog Switch

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from TTL open collector logic (15 volts) while the even numbered devices are driven directly from low level TTL logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

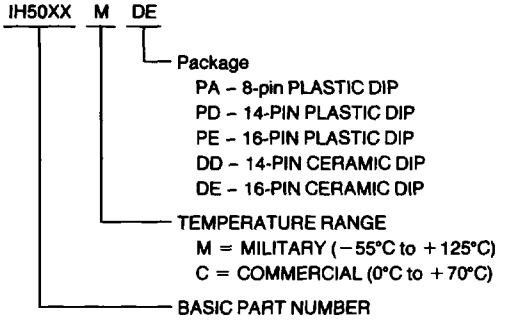
FEATURES

- **Switches Analog Signals Up to 20 Volts Peak-to-Peak**
- **Each Channel Complete – Interfaces With Most Integrated Logic**
- **Switching Speeds Less Than 0.5μs**
- **$I_{D(OFF)}$ Less Than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ – 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

ORDERING INFORMATION

Basic Part Number	Channels	Logic Level	Packages
IH5009	4	+15	DD,PD
IH5010	4	+5	DD,PD
IH5011	4	+15	DE,PE
IH5012	4	+5	DE,PE
IH5014	3	+5	DD,PD
IH5016	3	+5	DE,PE
IH5017	2	+15	DD,PA
IH5018	2	+5	DD,PA
IH5019	2	+15	DE,PA
IH5020	2	+5	DE,PA
IH5022	1	+5	DD,PA
IH5024	1	+5	DE,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.



NOTE: All typical values have been characterized but are not tested.

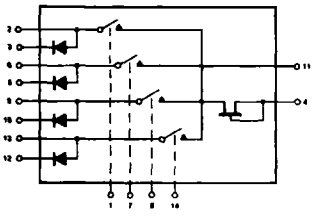
ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage ..... −15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Operating Temperature
5009C Series ..... 0°C to +70°C
5009M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

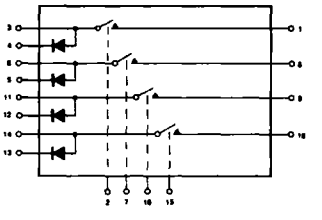
NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

IH5009 ($r_{DS(ON)} \leq 100\Omega$) IH5010 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PD, JD)



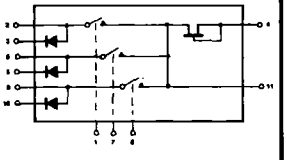
0284-1

IH5011 ($r_{DS(ON)} \leq 100\Omega$) IH5012 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



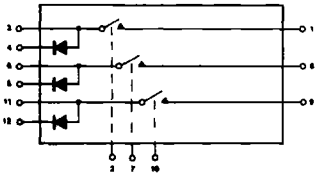
0284-2

IH5014 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PE, JE)



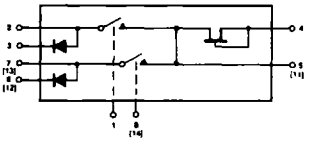
0284-3

IH5016 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



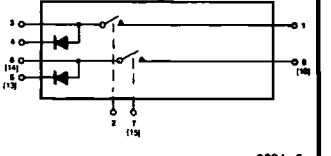
0284-4

IH5017 ($r_{DS(ON)} \leq 100\Omega$) IH5018 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



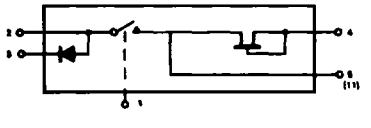
0284-5

IH5019 ($r_{DS(ON)} \leq 100\Omega$) IH5020 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA, JE)



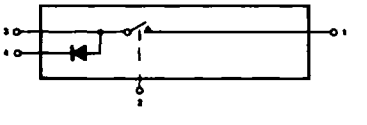
0284-6

IH5022 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



0284-7

IH5024 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA, JE)



0284-8

(Note: Numbers in brackets refer to CERDIP packages.)

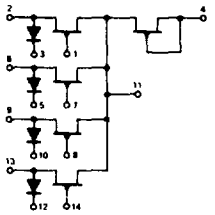
Figure 1: Pin Connections

NOTE: All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

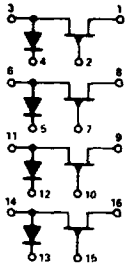
FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



0284-9

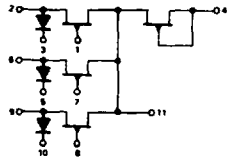
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



0284-10

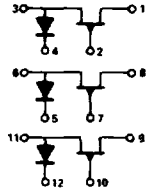
THREE CHANNEL

IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



0284-11

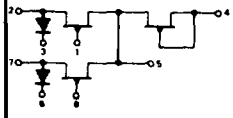
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



0284-12

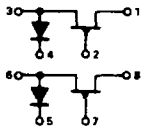
TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-13

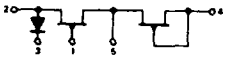
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-14

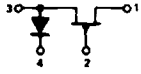
SINGLE CHANNEL

IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-15

IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-16

Figure 2: Device Schematics and Pin Connections

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (per channel)

Symbol (Note 1)	Characteristic	Type (Note 4)	TEST Conditions (Note 2)	Specification Limit				Units
				−55°C (M) 0°C (C)	25°C		+125°C (M) +70°C (C)	
				Min/Max	Typ	Min/Max	Min/Max	
$I_{IN(ON)}$	Input Current-ON	ALL	V_{IN} = 0V, I_D = 2mA		0.01	±0.5	100	µA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V		0.04	±0.5	20	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V		0.04	±0.5	20	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 7, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 8, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 6, Note 3			4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 8, Note 3			11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V		0.02	±0.5	20	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V		0.02	±0.5	20	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 1mA		0.30	±1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 1mA		0.10	±0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 2mA			1.0	10	µA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 2mA			2.0	100	µA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	I_D = 2mA, V_{IN} = 0.5V	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	I_D = 2mA, V_{IN} = 1.5V	100	80	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 5 & 6		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 5 & 6		300	500		ns
CT	Cross Talk	All	f = 100Hz		120			dB

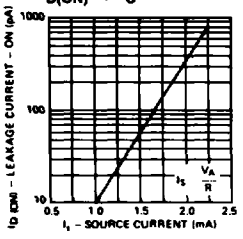
NOTES: 1. (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
2. Refer to Figure 2 for definition of terms.
3. $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of $r_{DS(ON)}$ and $I_{D(OFF)}$ respectively.
4. "5V Logic CKTS" applies to even-numbered devices. "15V Logic CKTS" applies to odd-numbered devices.

NOTE. All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

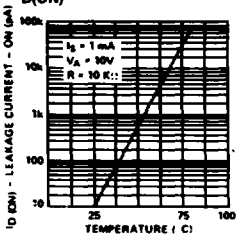
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

$I_{D(ON)}$ vs. I_S AT 25°C



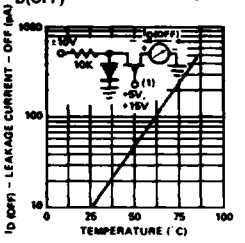
0284-17

$I_{D(ON)}$ vs. TEMPERATURE



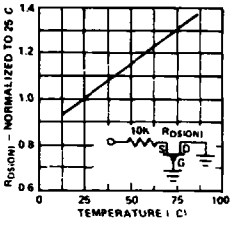
0284-18

$I_{D(OFF)}$ vs. TEMPERATURE



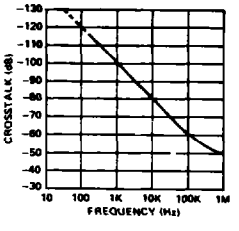
0284-19

$R_{DS(ON)}$ vs. TEMPERATURE (NORMALIZED TO 25°C VALUE)



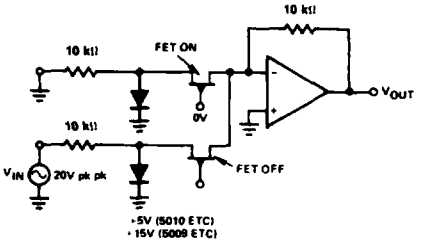
0284-20

CROSSTALK AS A FUNCTION OF FREQUENCY



0284-21

CROSSTALK MEASUREMENT CIRCUIT



0284-22

DETAILED DESCRIPTION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS}=0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by:

$$GAIN=\frac{10k\Omega + r_{DS(ON)}(compensator)}{10k\Omega + r_{DS(switch)}}.$$

NOTE: All typical values have been characterized but are not tested.

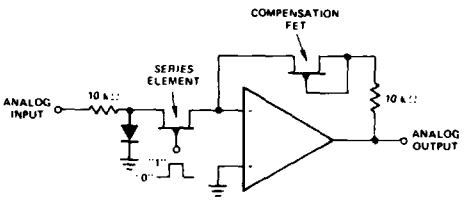


Figure 3: Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

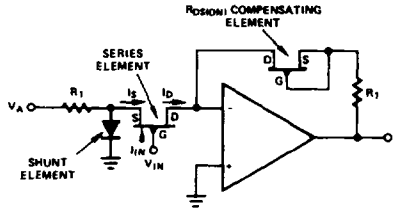


Figure 4.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by TTL open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

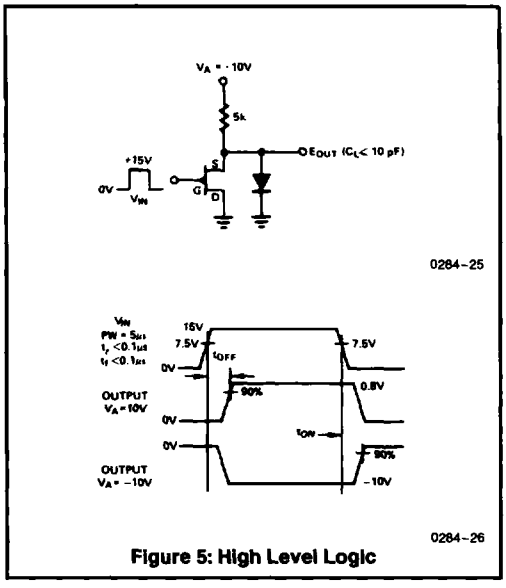


Figure 5: High Level Logic

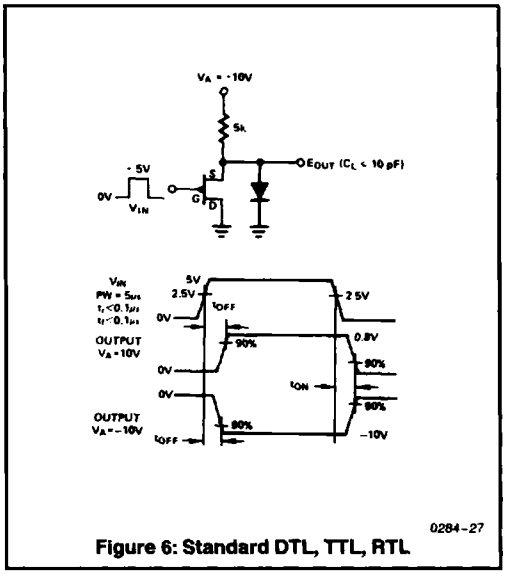


Figure 6: Standard DTL, TTL, RTL

NOTE. All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

LOGIC INTERFACE CIRCUITS

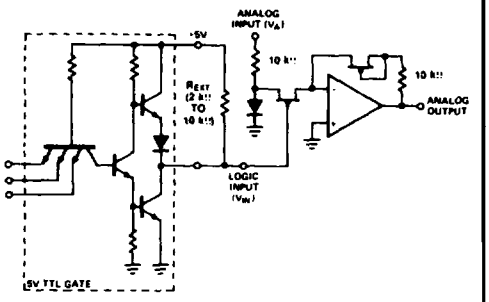


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Figure 7: Interfacing with +5V Logic

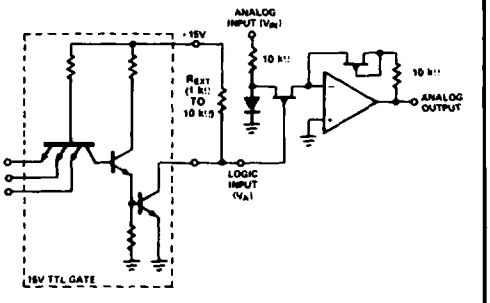

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Figure 8: Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)

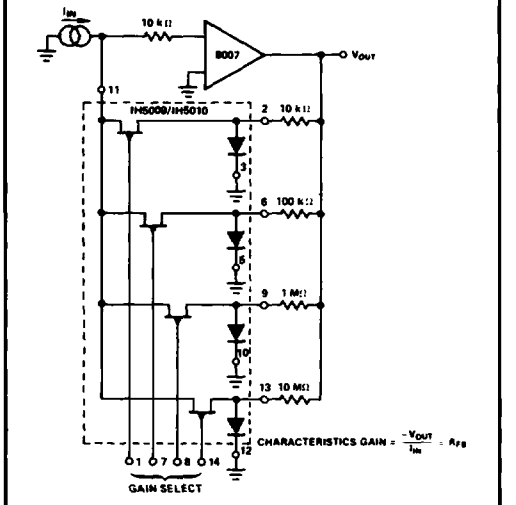

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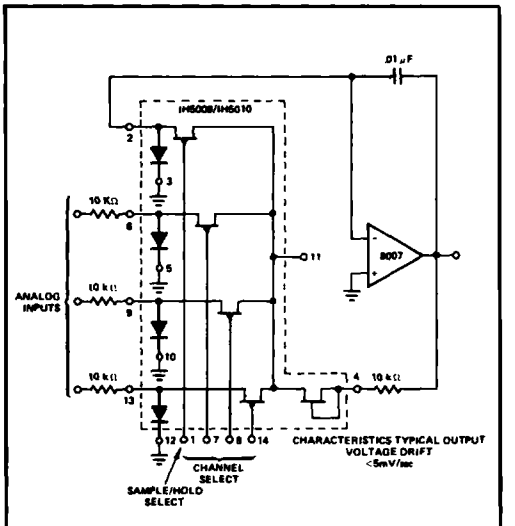
Figure 9



0284-31

Figure 10

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches".

NOTE: All typical values have been characterized but are not tested.