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National Semiconductor

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LMH6682/6683
190MHz Single Supply, Dual and Triple Operational Amplifiers

General Description

The LMH6682 and LMH6683 are high speed operational amplifiers designed for use in modern video systems. These single supply monolithic amplifiers extend National's feature-rich, high value video portfolio to include a dual and a triple version. The important video specifications of differential gain (± 0.01% typ.) and differential phase (±0.08 degrees) combined with an output drive current in each amplifier of 85mA make the LMH6682 and LMH6683 excellent choices for a full range of video applications.

Voltage feedback topology in operational amplifiers assures maximum flexibility and ease of use in high speed amplifier designs. The LMH6682/83 is fabricated in National Semiconductor's VIP10 process. This advanced process provides a superior ratio of speed to quiescient current consumption and assures the user of high-value amplifier designs. Advanced technology and circuit design enables in these amplifiers a –3db bandwidth of 190MHz, a slew rate of 940V/µsec, and stability for gains of less than –1 and greater than +2.

The input stage design of the LM6682/83 enables an input signal range that extends below the negative rail. The output stage voltage range reaches to within 0.8V of either rail when driving a 2kΩ load. Other attractive features include fast settling and low distortion. Other applications for these amplifiers include servo control designs. These applications are sensitive to amplifiers that exhibit phase reversal when the inputs exceed the rated voltage range. The LMH6682/83 amplifiers are designed to be immune to phase reversal when the specified input range is exceeded. See applications section. This feature makes for design simplicity and flexibility in many industrial applications.

The LMH6682 dual operational amplifier is offered in miniature surface mount packages, SOIC-8, and MSOP-8. The LMH6683 triple amplifier is offered in SOIC-14 and TSSOP-14.

Features

V_S = ±5V, T_A = 25˚C, R_L = 100Ω, A = +2 (Typical values unless specified)

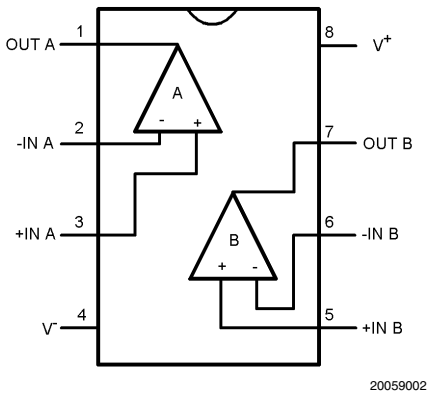
- DG error 0.01%
- DP error 0.08˚
- –3dB BW (A = +2) 190MHz
- Slew rate (V_S = ±5V) 940V/µs
- Supply current 6.5mA/amp
- Output current +80/–90mA
- Input common mode voltage 0.5V beyond V^-, 1.7V from V^+
- Output voltage swing (R_L = 2kΩ) 0.8V from rails
- Input voltage noise (100KHz) 12nV/$\sqrt{Hz}$

Applications

- CD/DVD ROM
- ADC buffer amp
- Portable video
- Current sense buffer
- Portable communications

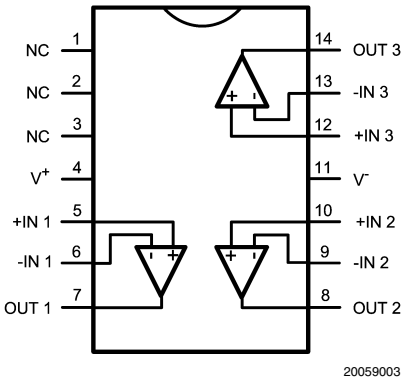
Connection Diagrams

SOIC-8/MSOP-8 (LMH6682)



Top View

SOIC-14/TSSOP-14 (LMH6683)



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2KV(Note 2)
Machine Model	200V (Note 3)
V_{IN} Differential	±2.5V
Output Short Circuit Duration	(Note 4), (Note 6)
Input Current	±10mA
Supply Voltage (V^+ - V^-)	12.6V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 7)	+150˚C

Operating Ratings (Note 1)

Supply Voltage (V^+ − V^-)	3V to 12V
Operating Temperature Range (Note 7)	−40˚C to +85˚C
Package Thermal Resistance (Note 7)	
SOIC-8	190˚C/W
MSOP-8	235˚C/W
SOIC-14	145˚C/W
TSSOP-14	155˚C/W

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L = 100Ω to $V^+/2$, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
SSBW	−3dB BW	A = +2, V_{OUT} = 200mV$_{PP}$	140	180		MHz
		A = −1, V_{OUT} = 200mV$_{PP}$		180		
GFP	Gain Flatness Peaking	A = +2, V_{OUT} = 200mV$_{PP}$ DC to 100MHz		2.1		dB
GFR	Gain Flatness Rolloff	A = +2, V_{OUT} = 200mV$_{PP}$ DC to 100MHz		0.1		dB
LPD 1˚	1˚ Linear Phase Deviation	A = +2, V_{OUT} = 200mV$_{PP}$, ±1˚		40		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	A = +2, ±0.1dB, V_{OUT} = 200mV$_{PP}$		25		MHz
FPBW	Full Power −1dB Bandwidth	A = +2, V_{OUT} = 2V$_{PP}$		110		MHz
DG	Differential Gain NTSC 3.58MHz	A = +2, R_L = 150Ω to $V^+/2$ Pos video only V_{CM} = 2V		0.03		%
DP	Differential Phase NTSC 3.58MHz	A = +2, R_L = 150Ω to $V^+/2$ Pos video only V_{CM} = 2V		0.05		deg
Time Domain Response						
T_r/T_f	Rise and Fall Time	20-80%, V_O = 1V$_{PP}$, A_V = +2		2.1		ns
		20-80%, V_O = 1V$_{PP}$, A_V = −1		2		
OS	Overshoot	A = +2, V_O = 100mV$_{PP}$		22		%
T_s	Settling Time	V_O = 2V$_{PP}$, ±0.1%, A_V = +2		49		ns
SR	Slew Rate (Note 11)	A = +2, V_{OUT} = 3V$_{PP}$		520		V/µs
		A = −1, V_{OUT} = 3V$_{PP}$		500		
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A = +2, R_L = 2kΩ		−60		dBc
		f = 5MHz, V_O = 2V$_{PP}$, A = +2, R_L = 100Ω		−61		
HD3	3rd Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A = +2, R_L = 2kΩ		−77		dBc
		f = 5MHz, V_O = 2V$_{PP}$, A = +2, R_L = 100Ω		−54		

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L = 100Ω to $V^+/2$, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Distortion and Noise Response						
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 2kΩ		−60		dBc
		f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 100Ω		−53		
e_n	Input Referred Voltage Noise	f = 1kHz		17		nV/ $\sqrt{Hz}$
		f = 100kHz		12		
i_n	Input Referred Current Noise	f = 1kHz		8		pA/ $\sqrt{Hz}$
		f = 100kHz		3		
CT	Cross-Talk Rejection (Amplifier)	f = 5MHz, A = +2, SND: R_L = 100Ω RCV: R_F = R_G = 510Ω		−77		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = 1.25V to 3.75V, R_L = 2kΩ to $V^+/2$	85	95		dB
		V_O = 1.5V to 3.5V, R_L = 150Ω to $V^+/2$	75	85		
		V_O = 2V to 3V, R_L = 50Ω to $V^+/2$	70	80		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−0.2 **−0.1**	−0.5		V
			3.0 **2.8**	3.3		
V_{OS}	Input Offset Voltage			±1.1	±5 **±7**	mV
TC V_{OS}	Input Offset Voltage Average Drift	(Note 12)		±2		µV/˚C
I_B	Input Bias Current	(Note 10)		−5	−20 **−30**	µA
TC $_{IB}$	Input Bias Current Drift			0.01		nA/˚C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.0V	72	82		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5V to 5.5V, V_{CM} = 1V	70	76		dB
I_S	Supply Current (per channel)	No load		6.5	9 **11**	mA

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L = 100Ω to $V^+/2$, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Miscellaneous Performance						
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$	4.10 **3.8**	4.25		V
		R_L = 150Ω to $V^+/2$	3.90 **3.70**	4.19		
		R_L = 75Ω to $V^+/2$	3.75 **3.50**	4.15		
	Output Swing Low	R_L = 2kΩ to $V^+/2$		800	920 **1100**	mV
		R_L = 150Ω to $V^+/2$		870	970 **1200**	
		R_L = 75Ω to $V^+/2$		885	1100 **1250**	
I_{OUT}	Output Current	V_O = 1V from either supply rail	±40	+80/–75		mA
I_{SC}	Output Short Circuit Current (Note 5), (Note 6), (Note 10)	Sourcing to $V^+/2$	–100 **–80**	–155		mA
		Sinking from $V^+/2$	100 **80**	220		
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			1.6		pF
R_{OUT}	Output Resistance Closed Loop	f = 1kHz, A = +2, R_L = 50Ω		0.02		Ω
		f = 1MHz, A = +2, R_L = 50Ω		0.12		

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = –5V, $V_O = V_{CM}$ = 0V, and R_L = 100Ω to 0V, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
SSBW	–3dB BW	A = +2, V_{OUT} = 200mV$_{PP}$	150	190		MHz
		A = –1, V_{OUT} = 200mV$_{PP}$		190		
GFP	Gain Flatness Peaking	A = +2, V_{OUT} = 200mV$_{PP}$ DC to 100MHz		1.7		dB
GFR	Gain Flatness Rolloff	A = +2, V_{OUT} = 200mV$_{PP}$ DC to 100MHz		0.1		dB
LPD 1˚	1˚ Linear Phase Deviation	A = +2, V_{OUT} = 200mV$_{PP}$, ±1˚		40		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	A = +2, ±0.1dB, V_{OUT} = 200mV$_{PP}$		25		MHz
FPBW	Full Power –1dB Bandwidth	A = +2, V_{OUT} = 2V$_{PP}$		120		MHz
DG	Differential Gain NTSC 3.58MHz	A = +2, R_L = 150Ω to 0V		0.01		%
DP	Differential Phase NTSC 3.58MHz	A = +2, R_L = 150Ω to 0V		0.08		deg
Time Domain Response						
T_r/T_f	Rise and Fall Time	20-80%, V_O = 1V$_{PP}$, A = +2		1.9		ns
		20-80%, V_O = 1V$_{PP}$, A = –1		2		
OS	Overshoot	A = +2, V_O = 100mV$_{PP}$		19		%
T_s	Settling Time	V_O = 2V$_{PP}$, ±0.1%, A = +2		42		ns

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = −5V, V_O = V_{CM} = 0V, and R_L = 100Ω to 0V, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Time Domain Response						
SR	Slew Rate (Note 11)	A = +2, V_{OUT} = $6V_{PP}$		940		V/µs
		A = −1, V_{OUT} = $6V_{PP}$		900		
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 2kΩ		−63		dBc
		f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 100Ω		−66		
HD3	3rd Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 2kΩ		−82		dBc
		f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 100Ω		−54		
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 2kΩ		−63		dBc
		f = 5MHz, V_O = $2V_{PP}$, A = +2, R_L = 100Ω		−54		
e_n	Input Referred Voltage Noise	f = 1kHz		18		nV/ $\sqrt{Hz}$
		f = 100kHz		12		
i_n	Input Referred Current Noise	f = 1kHz		6		pA/ $\sqrt{Hz}$
		f = 100kHz		3		
CT	Cross-Talk Rejection (Amplifier)	f = 5MHz, A = +2, SND: R_L = 100Ω RCV: R_F = R_G = 510Ω		−78		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = −3.75V to 3.75V, R_L = 2kΩ to $V^+/2$	87	100		dB
		V_O = −3.5V to 3.5V, R_L = 150Ω to $V^+/2$	80	90		
		V_O = −3V to 3V, R_L = 50Ω to $V^+/2$	75	85		
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50dB	−5.2 **−5.1**	−5.5		V
			3.0 **2.8**	3.3		
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Voltage Average Drift	(Note 12)		±2		µV/˚C
I_B	Input Bias Current	(Note 10)		−5	−20 **−30**	µA
TC $_{IB}$	Input Bias Current Drift			0.01		nA/˚C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.0V	75	84		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 8.5V to 9.5V, V^- = −1V	75	82		dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −4.5V to −5.5V, V^+ = 5V	78	85		dB

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = –5V, V_O = V_{CM} = 0V, and R_L = 100Ω to 0V, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Static, DC Performance						
I_S	Supply Current (per channel)	No load		6.5	9.5 **11**	mA
Miscellaneous Performance						
V_O	Output Swing High	R_L = 2kΩ to 0V	4.10 **3.80**	4.25		V
		R_L = 150Ω to 0V	3.90 **3.70**	4.20		
		R_L = 75Ω to 0V	3.75 **3.50**	4.18		
	Output Swing Low	R_L = 2kΩ to 0V		–4.19	–4.07 **–3.80**	mV
		R_L = 150Ω to 0V		–4.05	–3.89 **–3.65**	
		R_L = 75Ω to 0V		–4.00	–3.70 **–3.50**	
I_{OUT}	Output Current	V_O = 1V from either supply rail	±45	+85/–80		mA
I_{SC}	Output Short Circuit Current (Note 5) , (Note 6),(Note 10)	Sourcing to 0V	–120 **–100**	–180		mA
		Sinking from 0V	120 **100**	230		
R_{IN}	Common Mode Input Resistance			4		MΩ
C_{IN}	Common Mode Input Capacitance			1.6		pF
R_{OUT}	Output Resistance Closed Loop	f = 1kHz, A = +2, R_L = 50Ω		0.02		Ω
		f = 1MHz, A = +2, R_L = 50Ω		0.12		

Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Machine Model, 0Ω in series with 200pF.

Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 5: Short circuit test is a momentary test. See next note.

Note 6: Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

Note 7: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 8: Typical values represent the most likely parametric norm.

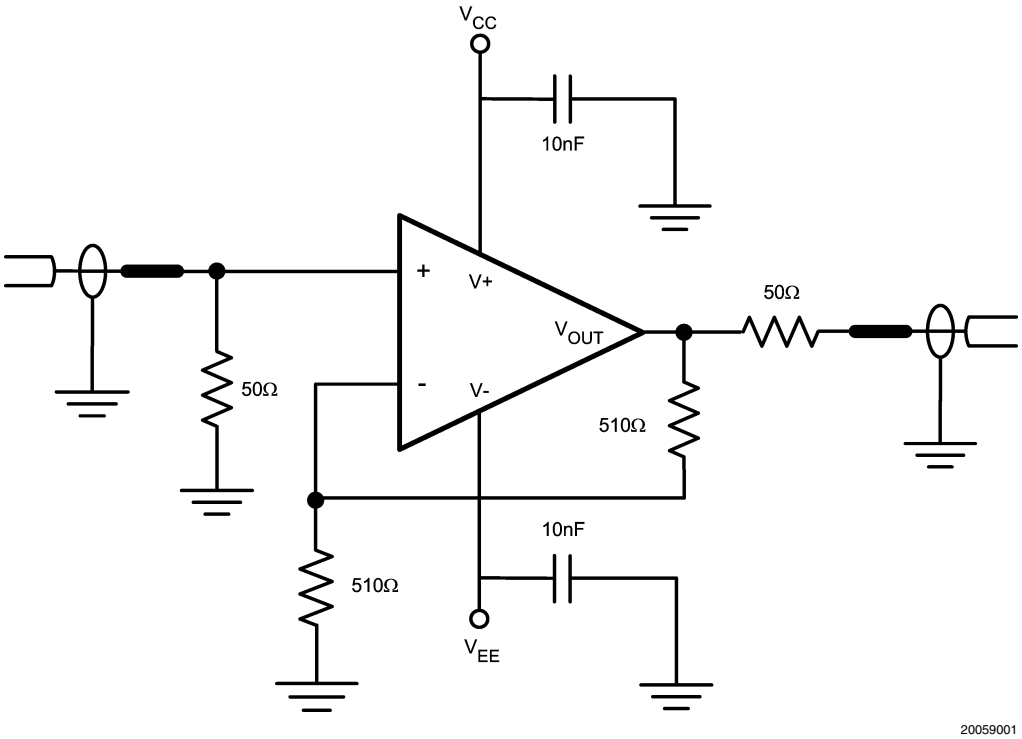
Note 9: All limits are guaranteed by testing or statistical analysis.

Note 10: Positive current corresponds to current flowing into the device.

Note 11: Slew rate is the average of the rising and falling slew rates

Note 12: Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Typical Schematic



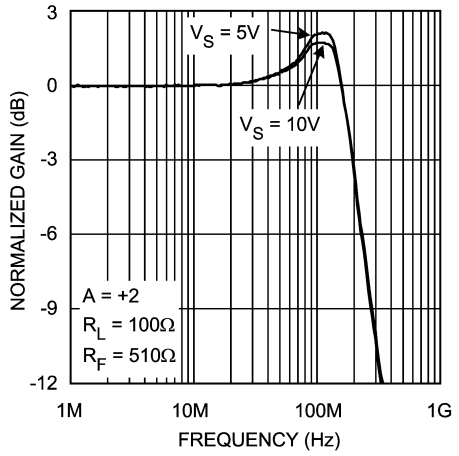
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6682MA	LMH6682MA	95 Units/Rail	M08A
	LMH6682MAX		2.5k Units Tape and Reel	
8-Pin MSOP	LMH6682MM	A90A	1k Units Tape and Reel	MUA08A
	LMH6682MMX		2.5k Units Tape and Reel	
14-Pin SOIC	LMH6683MA	LMH6683MA	55 Units/Rail	M14A
	LMH6683MAX		2.5k Units Tape and Reel	
14-Pin TSSOP	LMH6683MT	LMH6683MT	94 Units/Rail	MTC14
	LMH6683MTX		2.5 Units Tape and Reel	

Typical Performance Characteristics

At T_A = 25˚C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

Non-Inverting Frequency Response



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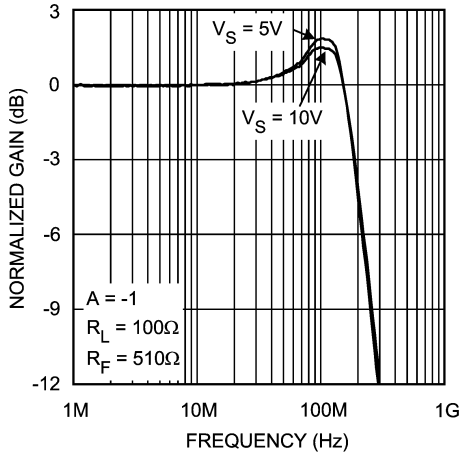
Inverting Frequency Response



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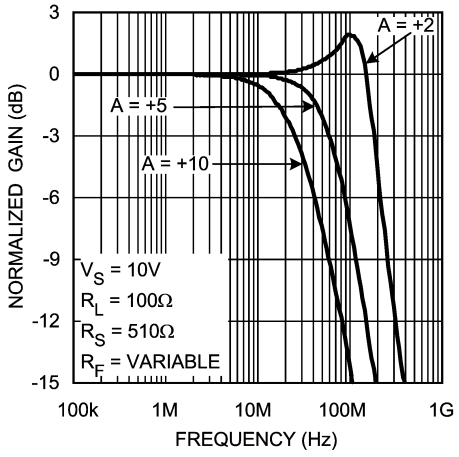
Non-Inverting Frequency Response for Various Gain



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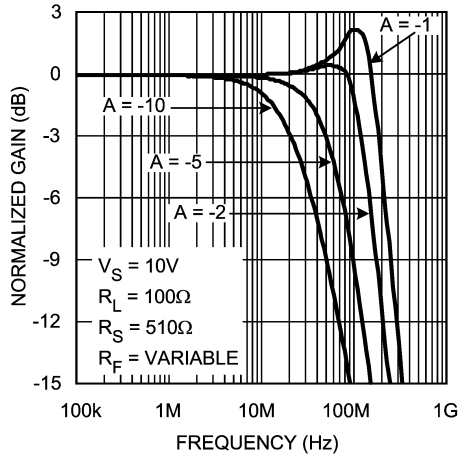
Inverting Frequency Response for Various Gain



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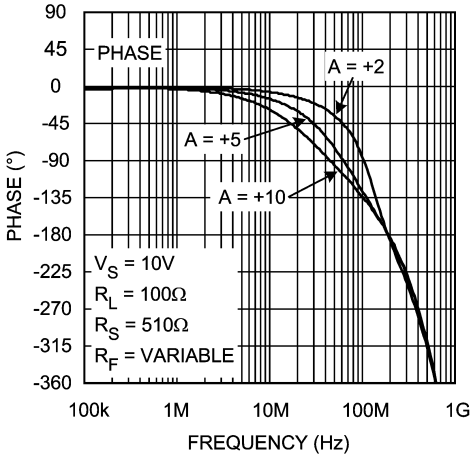
Non-Inverting Phase vs. Frequency for Various Gain



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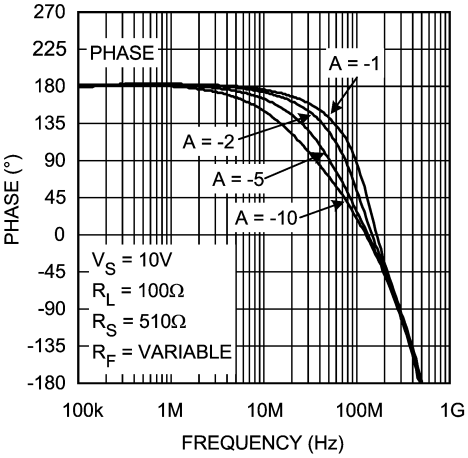
Inverting Phase vs. Frequency for Various Gain



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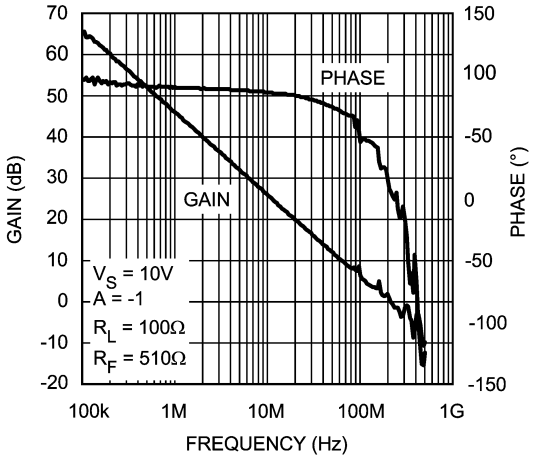
Typical Performance Characteristics (Continued)

Open Loop Gain & Phase vs. Frequency



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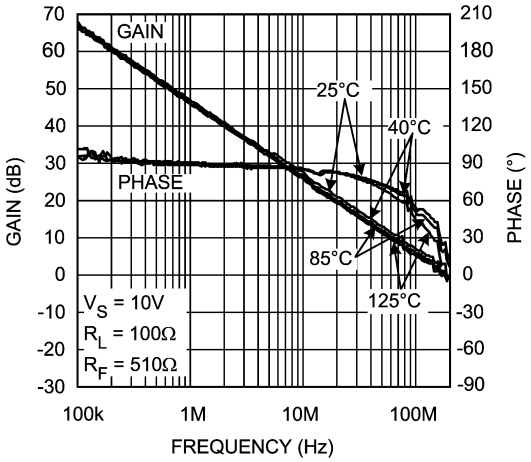
Open Loop Gain and Phase vs. Frequency Over Temperature



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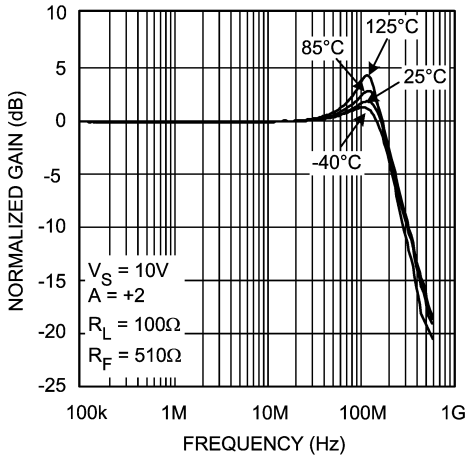
Non-Inverting Frequency Response Over Temperature



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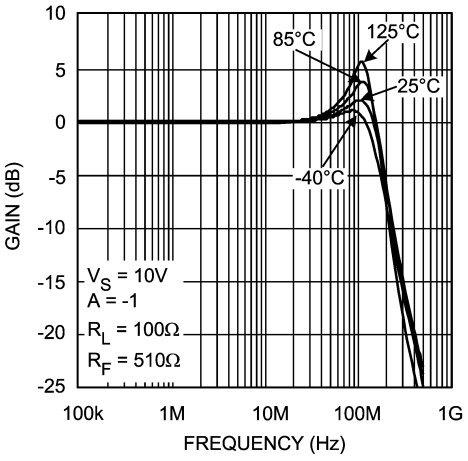
Inverting Frequency Response Over Temperature



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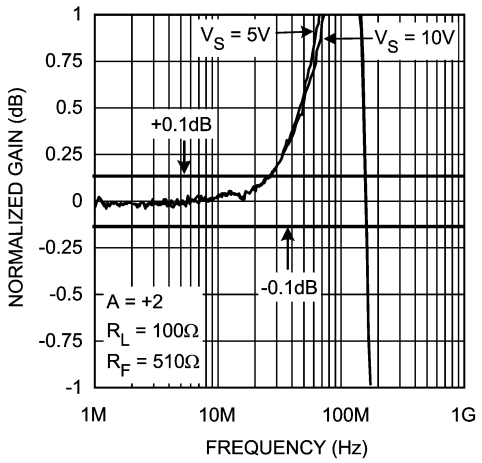
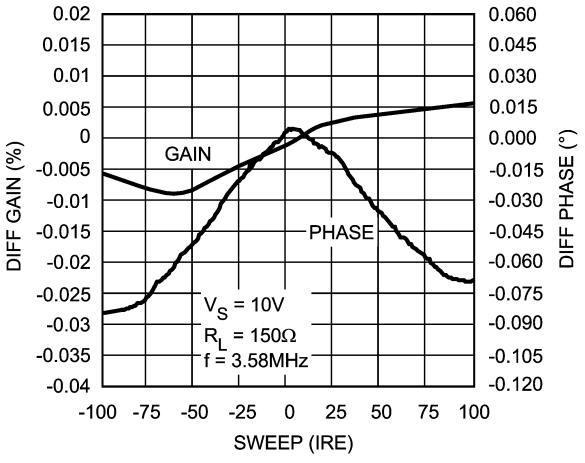
Gain Flatness 0.1dB



20059009

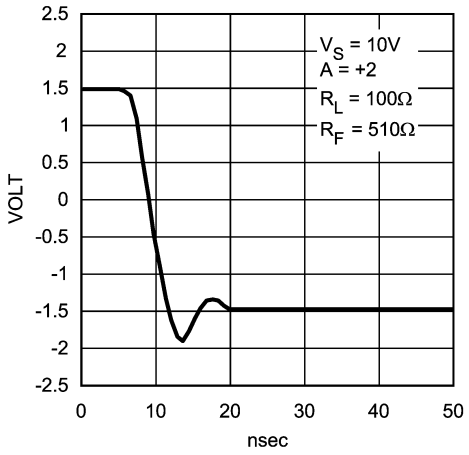
Differential Gain & Phase for A = +2



20059013

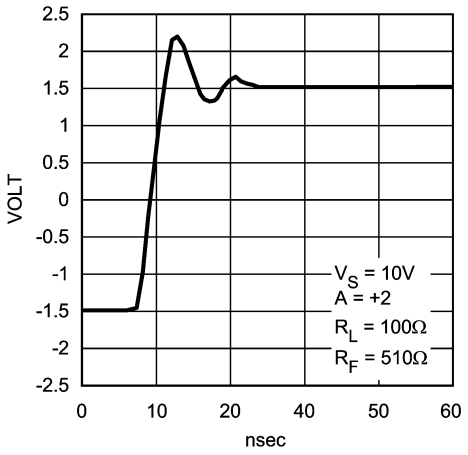
Typical Performance Characteristics (Continued)

Transient Response Negative



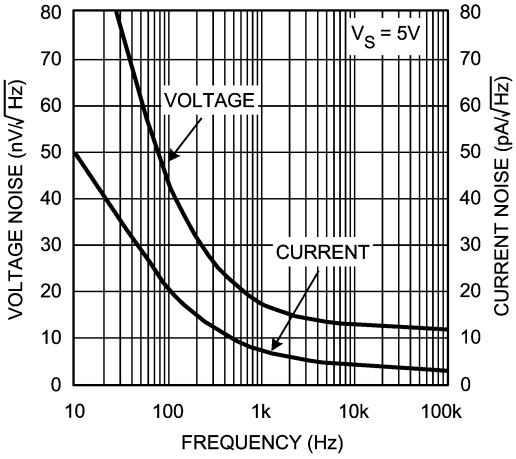
20059012

Transient Response Positive



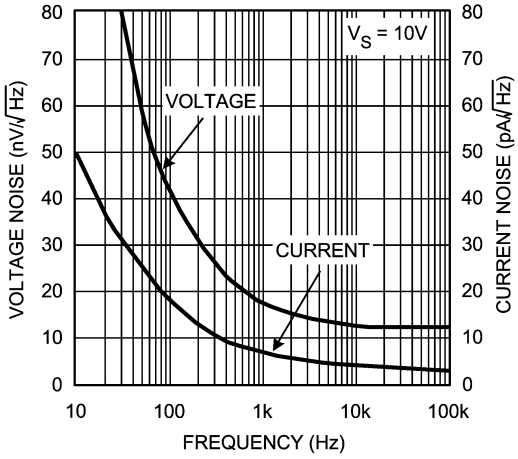
20059010

Noise vs. Frequency



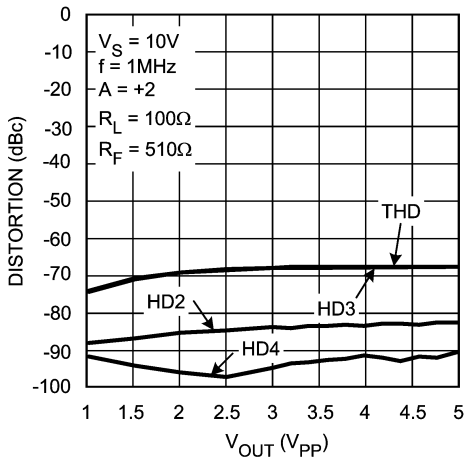
20059039

Noise vs. Frequency



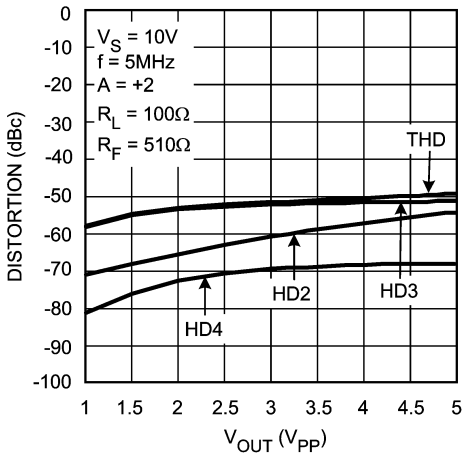
20059020

Harmonic Distortion vs. V_{OUT}



20059045

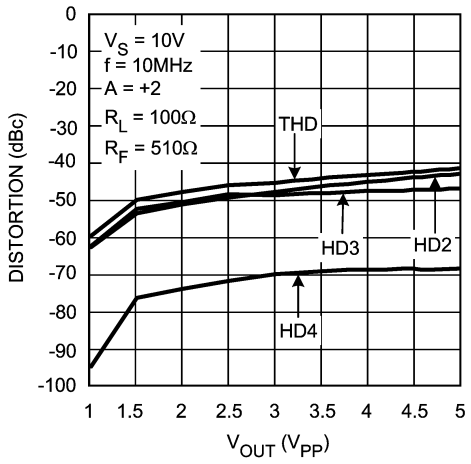
Harmonic Distortion vs. V_{OUT}



20059044

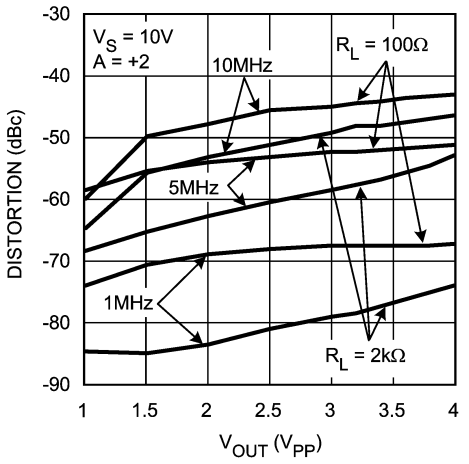
Typical Performance Characteristics (Continued)

Harmonic Distortion vs. V_{OUT}



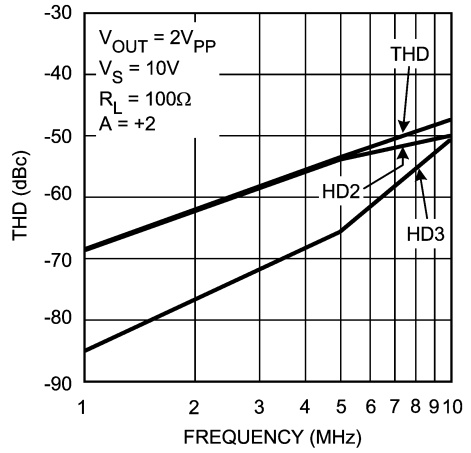
20059043

THD vs. for Various Frequencies



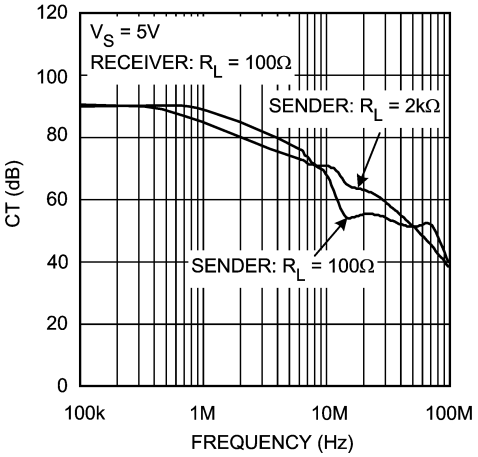
20059042

Harmonic Distortion vs. Frequency



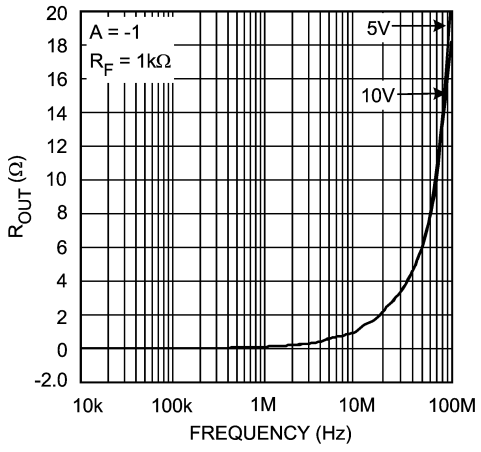
20059046

Crosstalk vs. Frequency



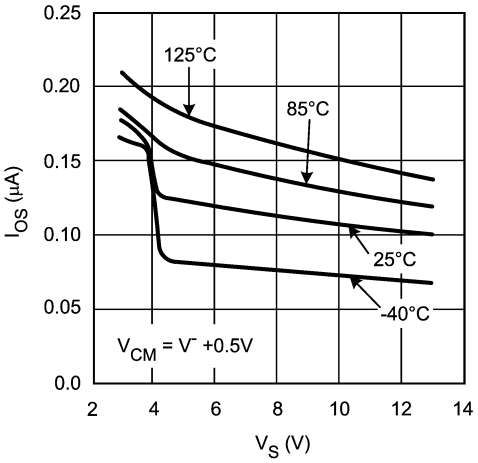
20059014

R_{OUT} vs. Frequency



20059021

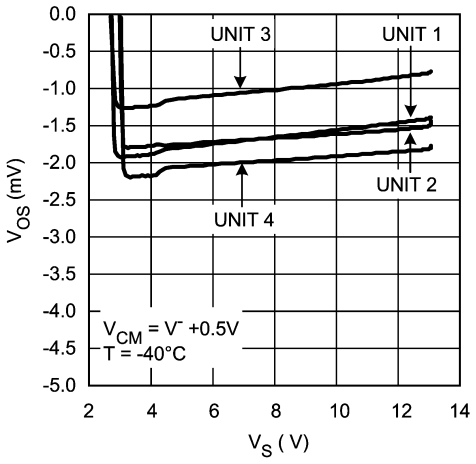
I_{OS} vs. V_{SUPPLY} Over Temperature



20059023

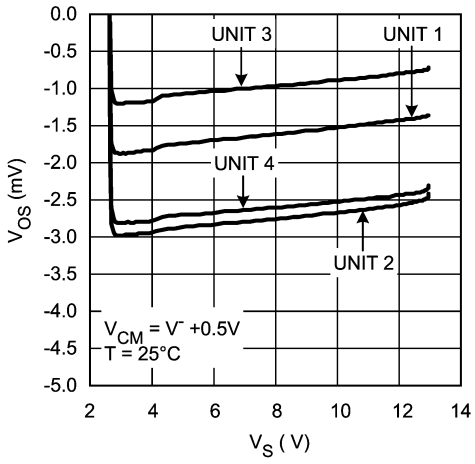
Typical Performance Characteristics (Continued)

V_{OS} vs. V_S @ –40˚C



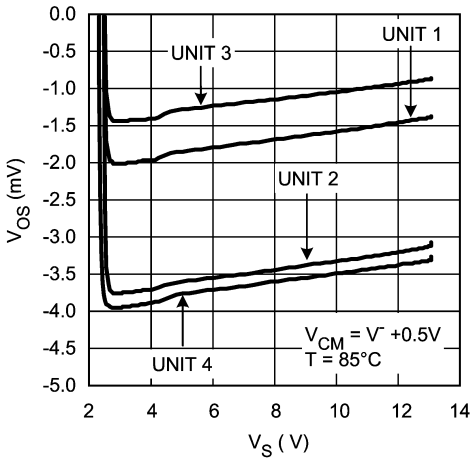
20059047

V_{OS} vs. V_S @ 25˚C



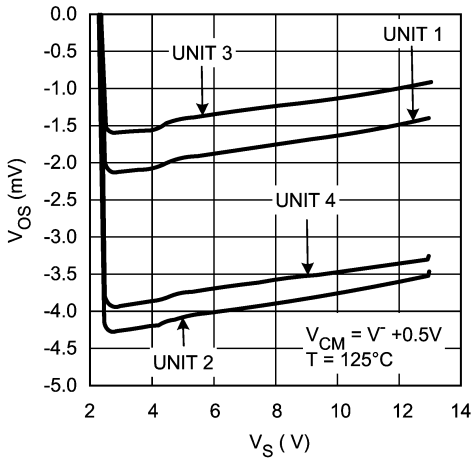
20059048

V_{OS} vs. V_S @ 85˚C



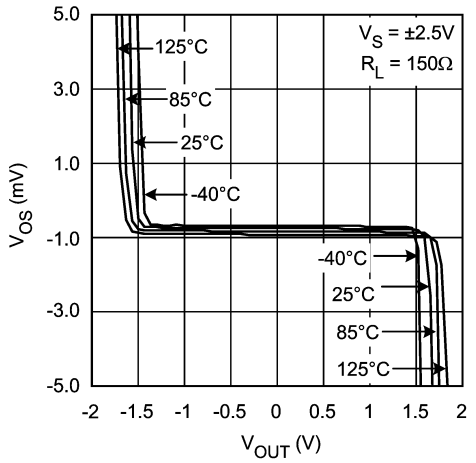
20059049

V_{OS} vs. V_S @ 125˚C



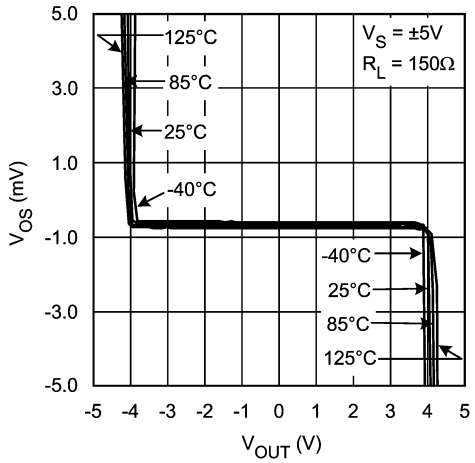
20059050

V_{OS} vs. V_{OUT}



20059035

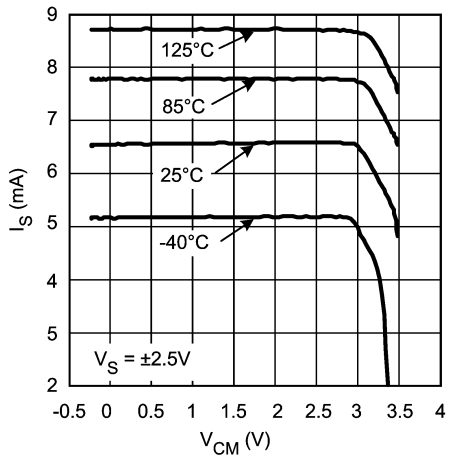
V_{OS} vs. V_{OUT}



20059036

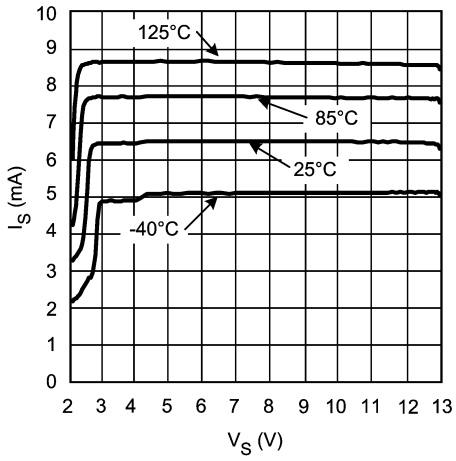
Typical Performance Characteristics (Continued)

I_{SUPPLY}/Amp vs. V_{CM}



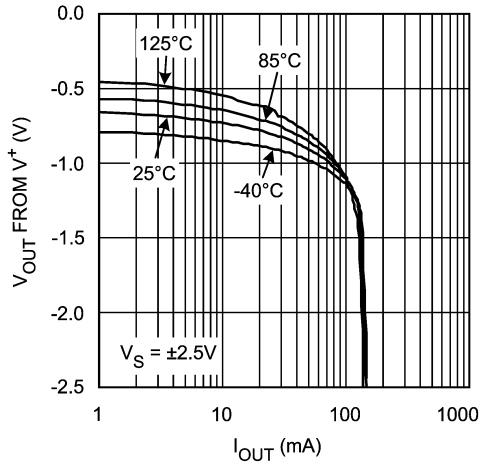
20059030

I_{SUPPLY}/Amp vs. V_{SUPPLY}



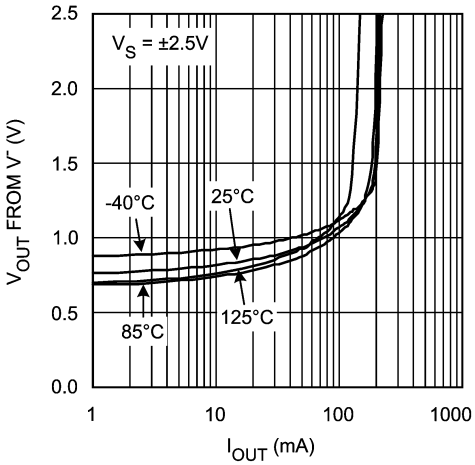
20059026

V_{OUT} vs. I_{SOURCE}



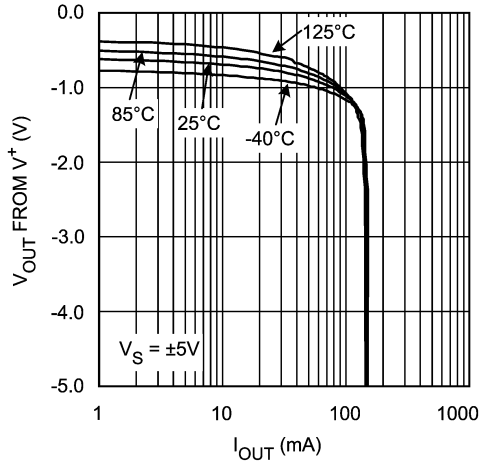
20059031

V_{OUT} vs. I_{SINK}



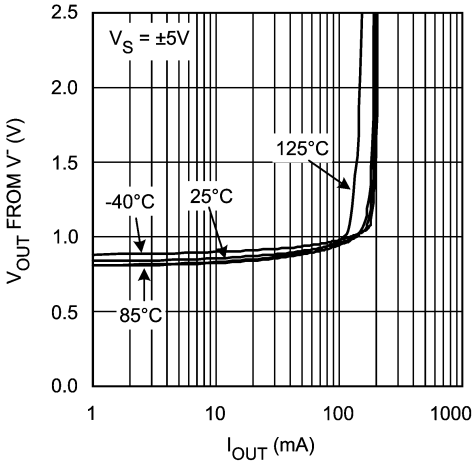
20059033

V_{OUT} vs. I_{SOURCE}



20059032

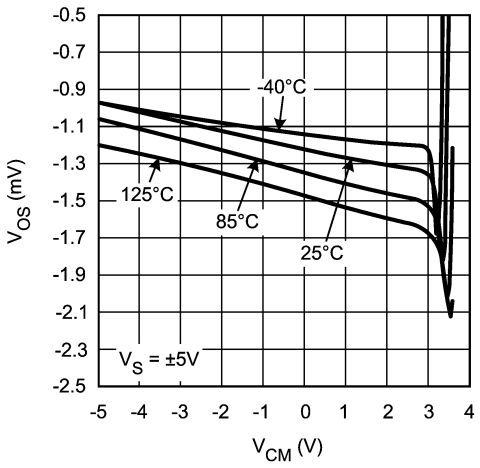
V_{OUT} vs. I_{SINK}



20059034

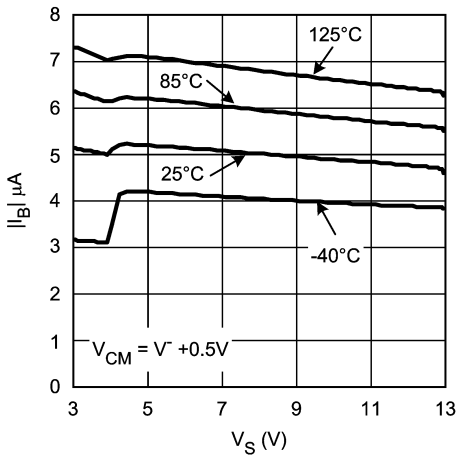
Typical Performance Characteristics (Continued)

V_{OS} vs. V_{CM}



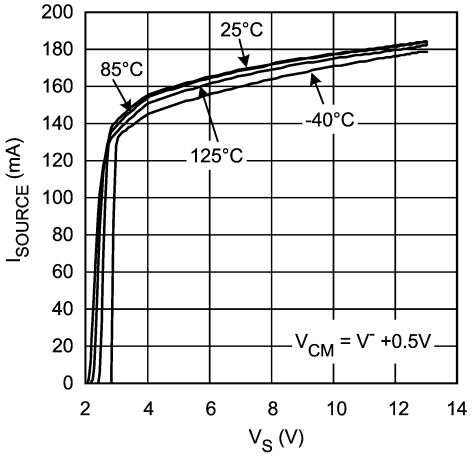
20059028

$|I_B|$vs. V_S



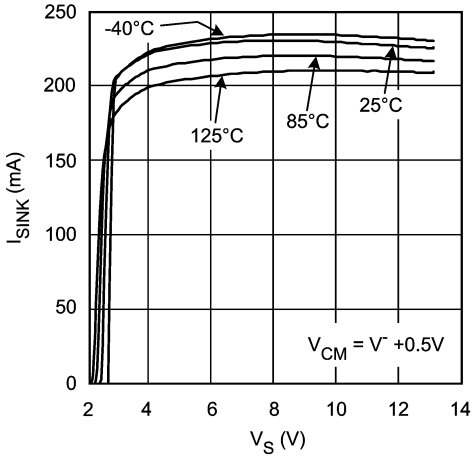
20059064

Short Circuit I_{SOURCE} vs. V_S



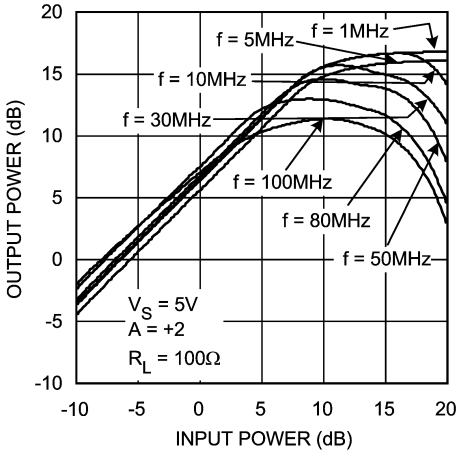
20059059

Short Circuit I_{SINK} vs. V_S



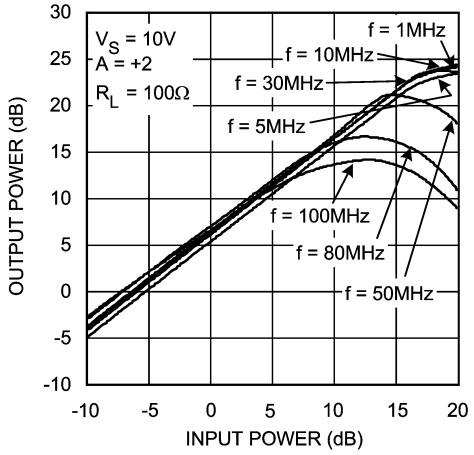
20059058

Linearity Input vs. Output



20059041

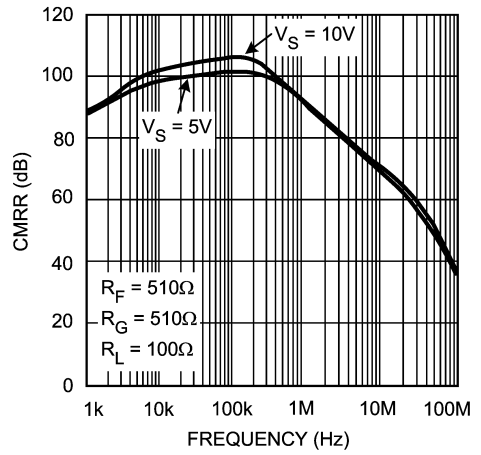
Linearity Input vs. Output



20059040

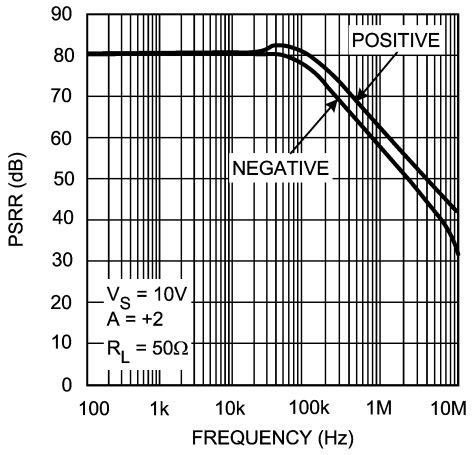
Typical Performance Characteristics (Continued)

CMRR vs. Frequency



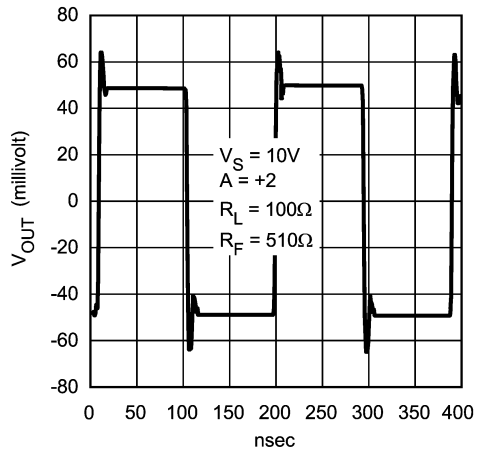
20059022

PSRR vs. Frequency



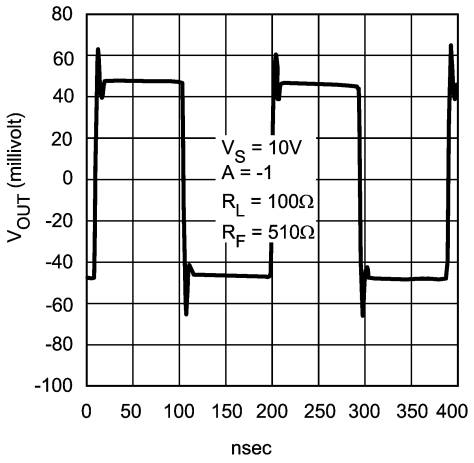
20059011

Small Signal Pulse Response for A = +2



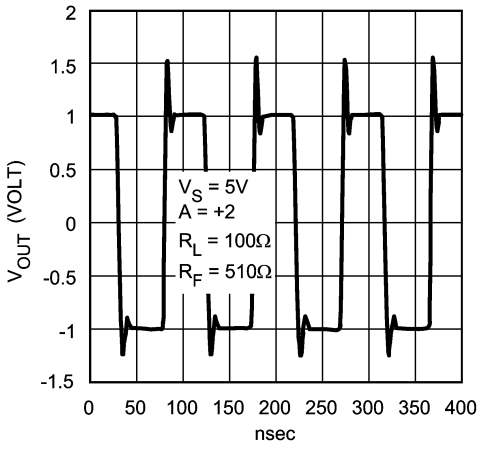
20059015

Small Signal Pulse Response A = –1



20059016

Large Signal Pulse Response



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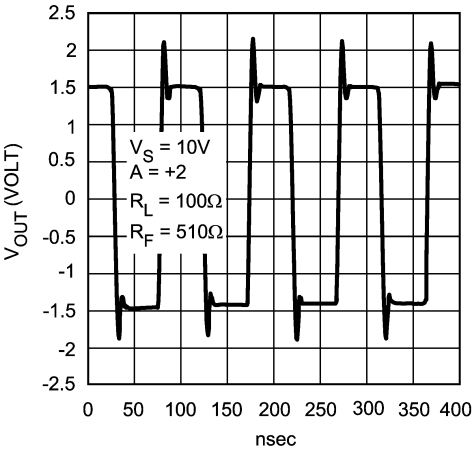
Large Signal Pulse Response



20059018

Applications Section

LARGE SIGNAL BEHAVIOR

Amplifying high frequency signals with large amplitudes (as in video applications) has some special aspects to look after. The bandwidth of the Op Amp for large amplitudes is less than the small signal bandwidth because of slew rate limitations. While amplifying pulse shaped signals the slew rate properties of the OpAmp become more important at higher amplitude ranges. Due to the internal structure of an Op Amp the output can only change with a limited voltage difference per time unit (dV/dt). This can be explained as follows: To keep it simple, assume that an Op Amp consists of two parts; the input stage and the output stage. In order to stabilize the Op Amp, the output stage has a compensation capacitor in its feedback path. This Miller C integrates the current from the input stage and determines the pulse response of the Op Amp. The input stage must charge/discharge the feedback capacitor, as can be seen in *Figure 1*.

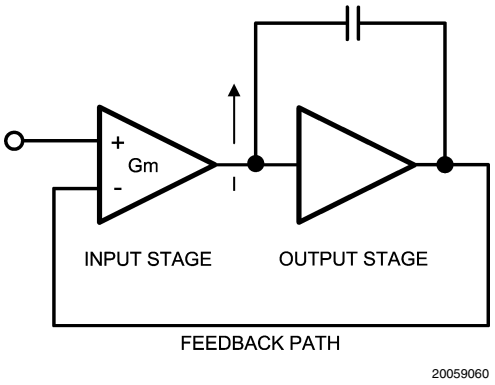


FIGURE 1.

When a voltage transient is applied to the non inverting input of the Op Amp, the current from the input stage will charge the capacitor and the output voltage will slope up. The overall feedback will subtract the gradually increasing output voltage from the input voltage. The decreasing differential input voltage is converted into a current by the input stage (Gm).

$$I*\Delta t = C*\Delta V \quad (1)$$

$$\Delta V/\Delta t = I/C \quad (2)$$

$$I=\Delta V*Gm \quad (3)$$

where I = current

t = time

C = capacitance

V = voltage

Gm = transconductance

Slew rate $\Delta V/\Delta t$ = volt/second

In most amplifier designs the current I is limited for high differential voltages (Gm becomes zero). The slew rate will than be limited as well:

$$\Delta V/\Delta t = Imax/C \quad (4)$$

The LMH6682/83 has a different setup of the input stage. It has the property to deliver more current to the output stage when the input voltage is higher (class AB input). The current into the Miller capacitor exhibits an exponential character, while this current in other Op Amp designs reaches a saturation level at high input levels: (see *Figure 2*)

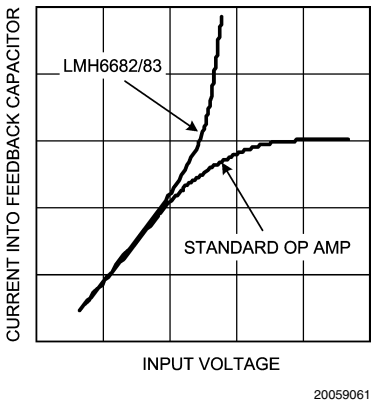


FIGURE 2.

This property of the LMH6682/83 guaranties a higher slew rate at higher differential input voltages.

$$\Delta V/\Delta t = \Delta V*Gm/C \quad (5)$$

In *Figure 3* one can see that a higher transient voltage than will lead to a higher slew rate.

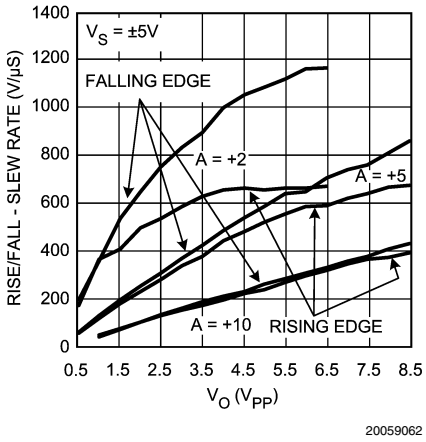


FIGURE 3.

HANDLING VIDEO SIGNALS

When handling video signals, two aspects are very important especially when cascading amplifiers in a NTSC- or PAL video system. A composite video signal consists of both amplitude and phase information. The amplitude represents saturation while phase determines color (color burst is 3.59MHz for NTSC and 4.58MHz for PAL systems). In this case it is not only important to have an accurate amplification of the amplitude but also it is important not to add a varying phase shift to the video signals. It is a known phenomena that at different dc levels over a certain load the phase of the amplified signal will vary a little bit. In a video chain many amplifiers will be cascaded and all errors will be added together. For this reason, it is necessary to have strict requirements for the variation in gain and phase in conjunction to different dc levels. As can be seen in the tables the number for the differential gain for the LMH6682/83 is only 0.01% and for the differential phase it is only 0.08° at a supply voltage of ±5V. Note that the phase is very depen-

Applications Section (Continued)

dent of the load resistance, mainly because of the dc current delivered by the parts output stage into the load. For more information about differential gain and phase and how to measure it see National Semiconductors application note OA-24 which can be found on via Nationals home page http://www.national.com

OUTPUT PHASE REVERSAL

This is a problem with some operational amplifiers. This effect is caused by phase reversal in the input stage due to saturation of one or more of the transistors when the inputs exceed the normal expected range of voltages. Some applications, such as servo control loops among others, are sensitive to this kind of behavior and would need special safeguards to ensure proper functioning. The LMH6682/6683 is immune to output phase reversal with input overload. With inputs exceeded, the LMH6682/6683 output will stay at the clamped voltage from the supply rail. Exceeding the input supply voltages beyond the Absolute Maximum Ratings of the device could however damage or otherwise adversely effect the reliability or life of the device.

DRIVING CAPACITIVE LOADS

The LMH6682/6683 can drive moderate values of capacitance by utilizing a series isolation resistor between the output and the capacitive load. Capacitive load tolerance will improve with higher closed loop gain values. Applications such as ADC buffers, among others, present complex and varying capacitive loads to the Op Amp; best value for this isolation resistance is often found by experimentation and actual trial and error for each application.

DISTORTION

Applications with demanding distortion performance requirements are best served with the device operating in the inverting mode. The reason for this is that in the inverting configuration, the input common mode voltage does not vary with the signal and there is no subsequent ill effects due to this shift in operating point and the possibility of additional non-linearity. Moreover, under low closed loop gain settings (most suited to low distortion), the non-inverting configuration is at a further disadvantage of having to contend with the input common voltage range. There is also a strong relationship between output loading and distortion performance (i.e. 2kΩ vs. 100Ω distortion improves by about 15dB @1MHz) especially at the lower frequency end where the distortion tends to be lower. At higher frequency, this dependence diminishes greatly such that this difference is only about 5dB at 10MHz. But, in general, lighter output load leads to reduced HD3 term and thus improves THD. (see the curve THD vs. V_{OUT} over various frequencies).

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SELECTION

Generally it is a good idea to keep in mind that for a good high frequency design both the active parts and the passive ones are suitable for the purpose you are using them for. Amplifying frequencies of several hundreds of MHz is possible while using standard resistors but it makes life much easier when using surface mount ones. These resistors (and capacitors) are smaller and therefore parasitics have lower values and will have less influence on the properties of the amplifier. Another important issue is the PCB, which is no longer a simple carrier for all the parts and a medium to interconnect them. The board becomes a real part itself, adding its own high frequency properties to the overall performance of the circuit. It's good practice to have at least one ground plane on a PCB giving a low impedance path for all decouplings and other ground connections. Care should be taken especially that on board transmission lines have the same impedance as the cables they are connected to (i.e. 50Ω for most applications and 75Ω in case of video and cable TV applications). These transmission lines usually require much wider traces on a standard double sided PCB than needed for a 'normal' connection. Another important issue is that inputs and outputs must not 'see' each other or are routed together over the PCB at a small distance. Furthermore it is important that components are placed as flat as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB avoids oscillations or other unwanted behavior. When working with really high frequencies, the only components which can be used will be the surface mount ones (for more information see OA-15).

As an example of how important the component values are for the behavior of your circuit, look at the following case: On a board with good high frequency layout, an amplifier is placed. For the two (equal) resistors in the feedback path, 5 different values are used to set the gain to +2. The resistors vary from 200Ω to 3kΩ.

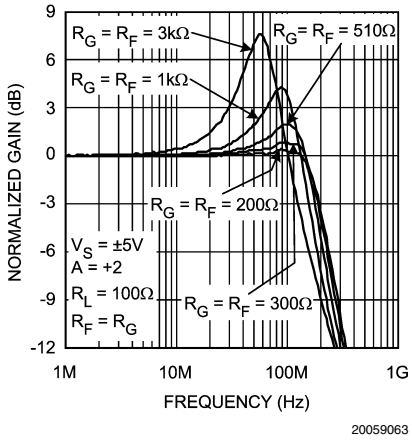


FIGURE 4.

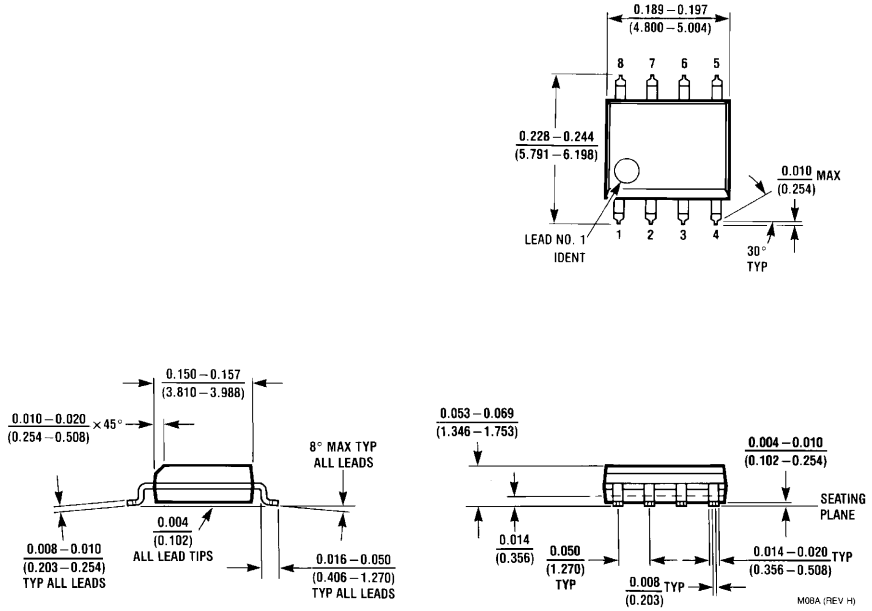
In *Figure 4* can be seen that there's more peaking with higher resistor values, which can lead to oscillations and bad pulse responses. On the other hand the low resistor values will contribute to higher overall power consumption.

NSC suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

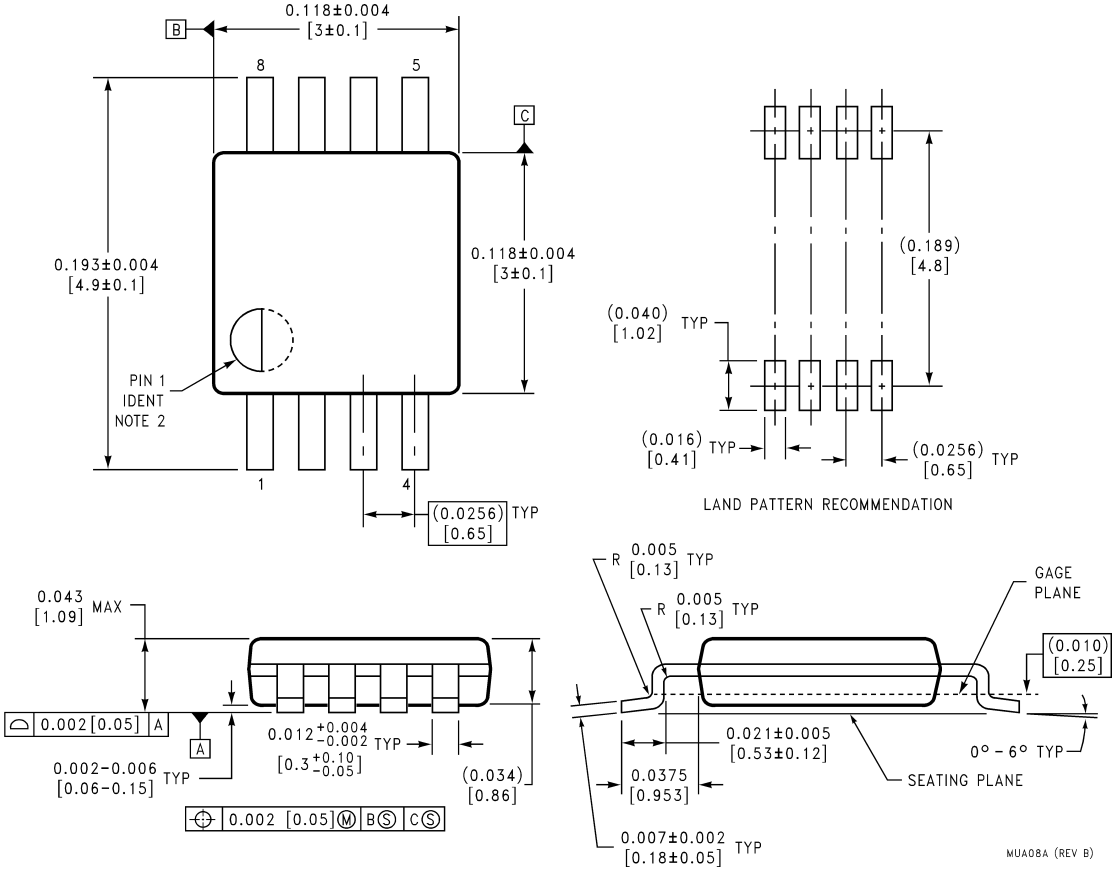
Device	Package	Evaluation Board PN
LMH6682MA	8-Pin SOIC	CLC730036
LMH6682MM	8-Pin MSOP	CLC730123
LMH6683MA	14-Pin SOIC	CLC730031
LMH6683MT	14-Pin TSSOP	CLC730131

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters) unless otherwise noted

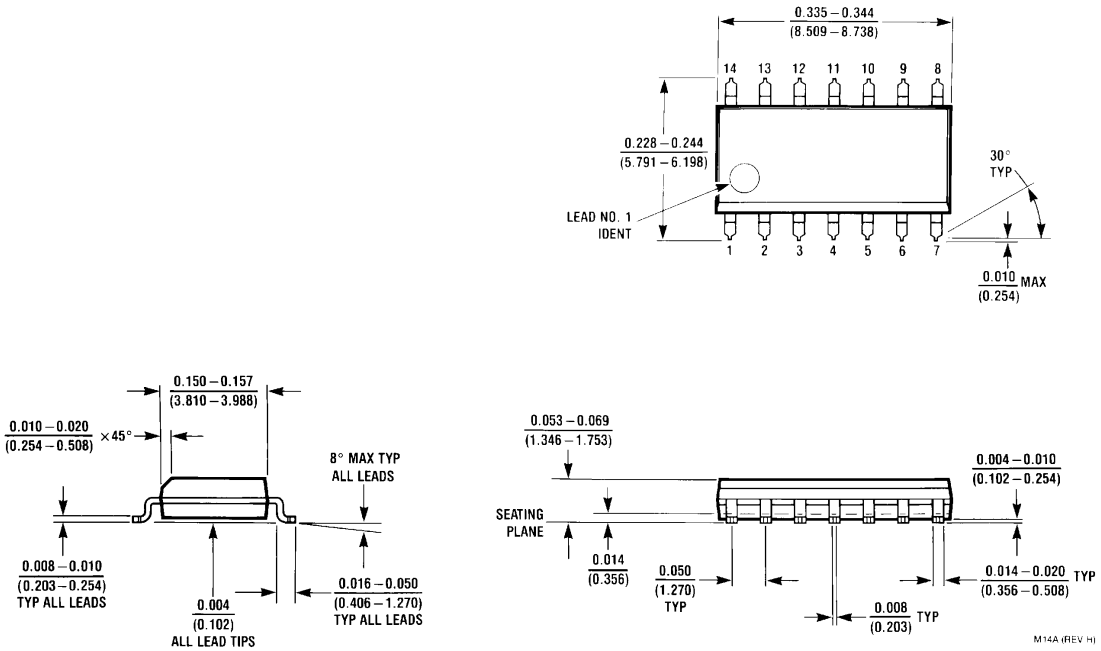


8-Pin SOIC
NS Package Number M08A

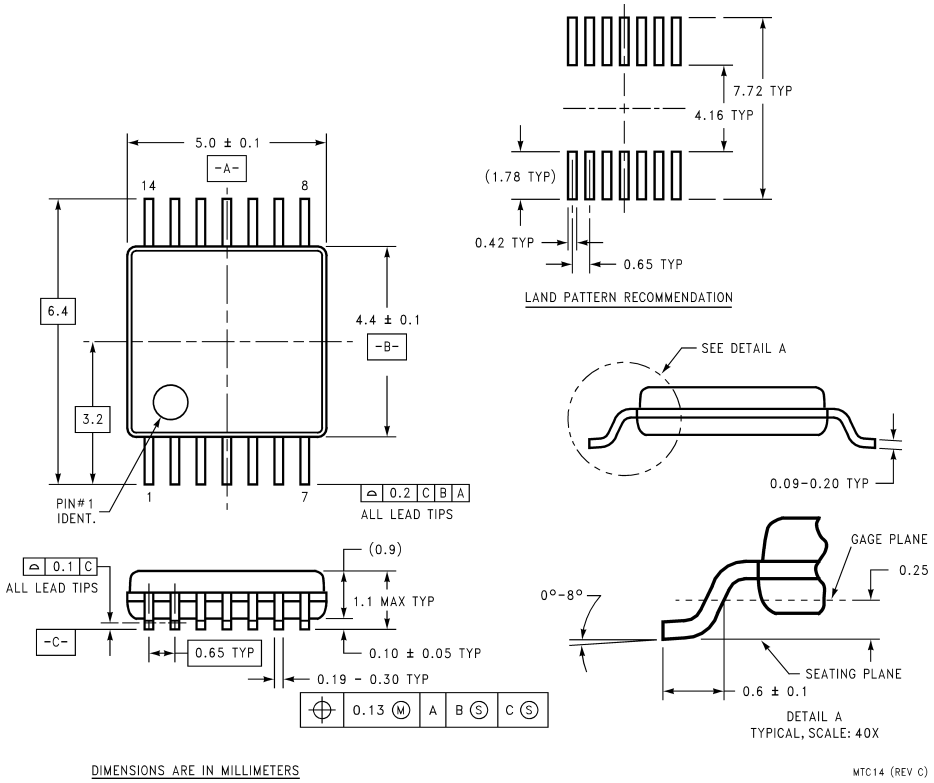


8-Pin MSOP
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin SOIC
NS Package Number M14A



14-Pin TSSOP
NS Package Number MTC14

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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