95H00 FOUR BIT UNIVERSAL SHIFT REGISTER

9502.9503.9504 **BASIC GATES**

Parkage 16 Pin . 3 Fow PESCRIPTION The 95H00 is a four borage, shifting the shift region orage, shifting the shift region of the Wanie. ParFSC + LATIA

MHz

Features include assertion outputs on each state, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of all these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

- HIGH SPEED . . . 150 MHz SHIFT FREQUENCY
- D TYPE INPUT IN SERIAL AND PARALLEL
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- 50 Ω DRIVE ON Q3 OUTPUT
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER VCC PINS - ELIMINATE NOISE COUPLING
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULL DOWN**
- SINGLE -5.2 VOLT POWER SUPPLY
- **HERMETIC CERAMIC 16 PIN DIP**
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

DESCRIPTION The 9502, 9503 and 9504 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

Input and output 2K Ω pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

- HIGH SPEED . . . 2.3 ns PER GATE
- SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING
- **TEMPERATURE COMPENSATION**
- INTERNAL PULLDOWN RESISTORS
- **COMMON ENABLE INPUTS**
- LOW CROSSTALK AND NOISE GENERATION
- **WIRE-OR CAPABILITY**
- 50 Ω LINE DRIVING CAPABILITY
- COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)
- SINGLE -5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



