


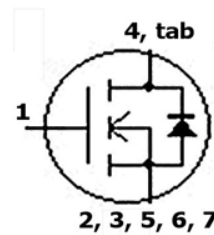
**OptiMOS™ 3 Power-Transistor**
**Features**

- for sync. rectification, motor-drives and dc/dc SMPS
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

**Product Summary**

|                  |     |            |
|------------------|-----|------------|
| $V_{DS}$         | 60  | V          |
| $R_{DS(on),max}$ | 3.4 | m $\Omega$ |
| $I_D$            | 100 | A          |

|                |  |
|----------------|--|
| <b>Type</b>    | IPB034N06N3 G  |
|                |  |
| <b>Package</b> | PG-TO263-7   |
| <b>Marking</b> | 034N06N  |


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

| Parameter                                    | Symbol         | Conditions                            | Value       | Unit               |
|--|----------------|---------------------------------------|-------------|--------------------|
| Continuous drain current                     | $I_D$          | $T_C=25\text{ °C}^{2)}$               | 100         | A                  |
|  |                | $T_C=100\text{ °C}$                   | 100         |                    |
| Pulsed drain current <sup>3)</sup>           | $I_{D,pulse}$  | $T_C=25\text{ °C}$                    | 400         |                    |
| Avalanche energy, single pulse <sup>4)</sup> | $E_{AS}$       | $I_D=100\text{ A}, R_{GS}=25\ \Omega$ | 149         | mJ                 |
| Gate source voltage                          | $V_{GS}$       |                                       | $\pm 20$    | V                  |
| Power dissipation                            | $P_{tot}$      | $T_C=25\text{ °C}$                    | 167         | W                  |
| Operating and storage temperature            | $T_j, T_{stg}$ |                                       | -55 ... 175 | $^{\circ}\text{C}$ |
| IEC climatic category; DIN IEC 68-1          |                |                                       | 55/175/56   |                    |

<sup>1)</sup>J-STD20 and JESD22

<sup>2)</sup> Current is limited by bondwire; with an  $R_{thJC}=0.9\text{ K/W}$  the chip is able to carry 164 A.

<sup>3)</sup> See figure 3 for more detailed information

<sup>4)</sup> See figure 13 for more detailed information

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

**Thermal characteristics**

|  |            |  |   |   |     |     |
|--|------------|--|---|---|-----|-----|
| Thermal resistance, junction - case    | $R_{thJC}$ |  | - | - | 0.9 | K/W |
| Thermal resistance, junction - ambient | $R_{thJA}$ | minimal footprint                            | - | - | 62  |     |
|  |            | 6 cm <sup>2</sup> cooling area <sup>5)</sup> | - | - | 40  |     |

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

|                                  |               |  |    |     |     |               |
|----------------------------------|---------------|--|----|-----|-----|---------------|
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=1\text{ mA}$                       | 60 | -   | -   | V             |
| Gate threshold voltage           | $V_{GS(th)}$  | $V_{DS}=V_{GS}, I_D=93\text{ }\mu\text{A}$                 | 2  | 3   | 4   |               |
| Zero gate voltage drain current  | $I_{DSS}$     | $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$  | -  | 0.1 | 1   | $\mu\text{A}$ |
|                                  |               | $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$ | -  | 10  | 100 |               |
| Gate-source leakage current      | $I_{GSS}$     | $V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$                    | -  | 1   | 100 | nA            |
| Drain-source on-state resistance | $R_{DS(on)}$  | $V_{GS}=10\text{ V}, I_D=100\text{ A}$                     | -  | 2.7 | 3.4 | m $\Omega$    |
| Gate resistance                  | $R_G$         |  | -  | 1.3 | -   | $\Omega$      |
| Transconductance                 | $g_{fs}$      | $ V_{DS} >2 I_D R_{DS(on)max}, I_D=100\text{ A}$           | 68 | 135 | -   | S             |

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

**Dynamic characteristics**

|                              |              |   |   |      |       |    |
|------------------------------|--------------|---|---|------|-------|----|
| Input capacitance            | $C_{iss}$    | $V_{GS}=0\text{ V}, V_{DS}=30\text{ V},$<br>$f=1\text{ MHz}$                    | - | 8000 | 11000 | pF |
| Output capacitance           | $C_{oss}$    |   | - | 1700 | 2300  |    |
| Reverse transfer capacitance | $C_{rss}$    |   | - | 58   | -     |    |
| Turn-on delay time           | $t_{d(on)}$  | $V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$<br>$I_D=90\text{ A}, R_G=3.2\ \Omega$ | - | 38   | -     | ns |
| Rise time                    | $t_r$        |   | - | 161  | -     |    |
| Turn-off delay time          | $t_{d(off)}$ |   | - | 63   | -     |    |
| Fall time                    | $t_f$        |   | - | 16   | -     |    |

**Gate Charge Characteristics<sup>6)</sup>**

|                       |               |   |   |     |     |    |
|-----------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | $Q_{gs}$      | $V_{DD}=30\text{ V}, I_D=100\text{ A},$<br>$V_{GS}=0\text{ to }10\text{ V}$ | - | 43  | -   | nC |
| Gate to drain charge  | $Q_{gd}$      |   | - | 9   | -   |    |
| Switching charge      | $Q_{sw}$      |   | - | 28  | -   |    |
| Gate charge total     | $Q_g$         |   | - | 98  | 130 |    |
| Gate plateau voltage  | $V_{plateau}$ |   | - | 5.4 | -   | V  |
| Output charge         | $Q_{oss}$     | $V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$                                     | - | 79  | 105 | nC |

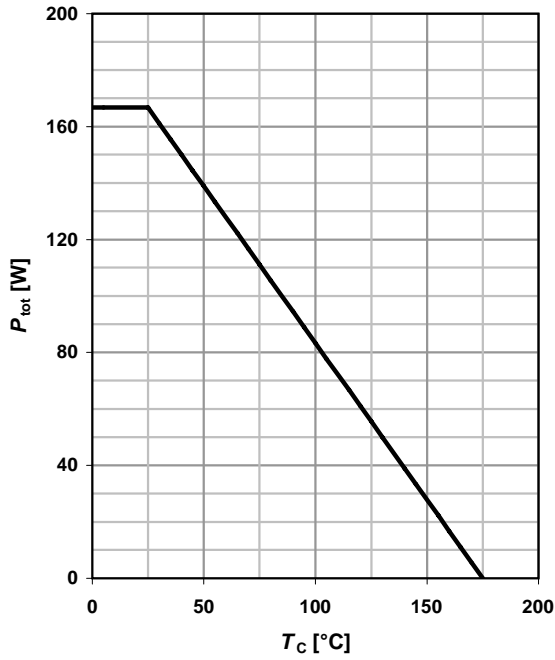
**Reverse Diode**

|                                  |               |   |   |     |     |    |
|----------------------------------|---------------|---|---|-----|-----|----|
| Diode continuous forward current | $I_S$         | $T_C=25\text{ }^\circ\text{C}$  | - | -   | 100 | A  |
| Diode pulse current              | $I_{S,pulse}$ |   | - | -   | 400 |    |
| Diode forward voltage            | $V_{SD}$      | $V_{GS}=0\text{ V}, I_F=100\text{ A},$<br>$T_j=25\text{ }^\circ\text{C}$  | - | 0.9 | 1.2 | V  |
| Reverse recovery time            | $t_{rr}$      | $V_R=30\text{ V}, I_F=80\text{ A},$<br>$di_F/dt=100\text{ A}/\mu\text{s}$ | - | 48  | -   | ns |
| Reverse recovery charge          | $Q_{rr}$      |   | - | 73  | -   | nC |

<sup>6)</sup> See figure 16 for gate charge parameter definition

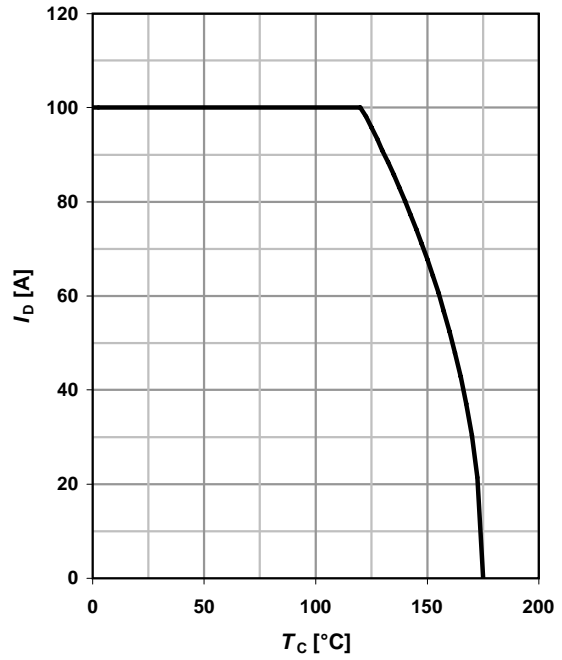
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

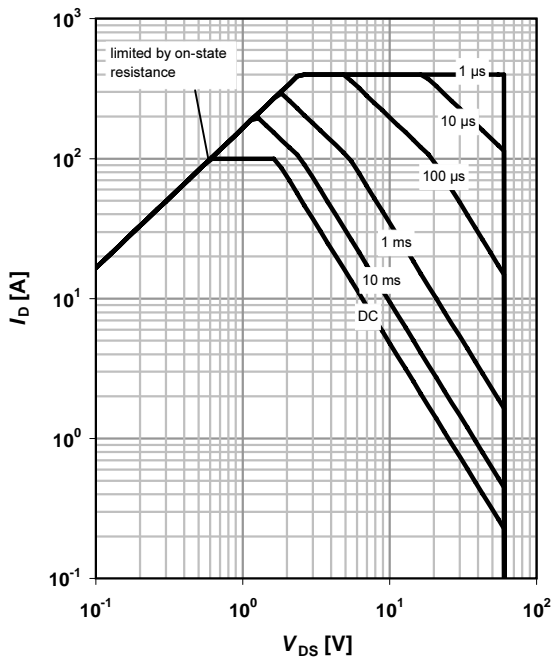
$I_D=f(T_C); V_{GS} \geq 10 V$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25^\circ C; D=0$

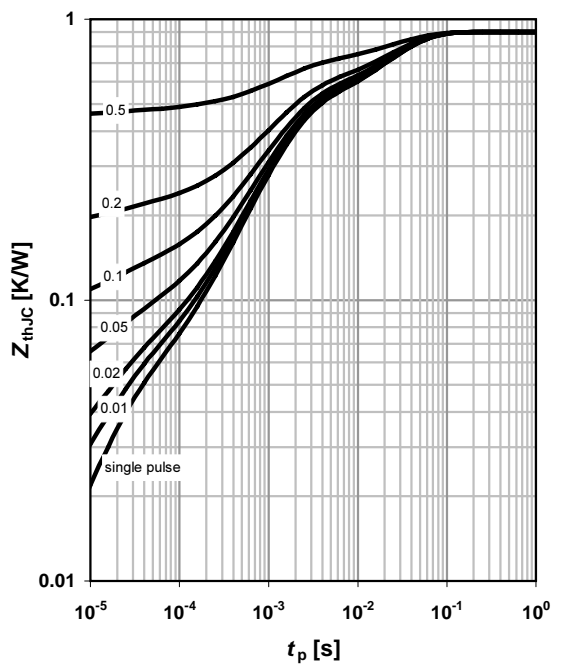
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

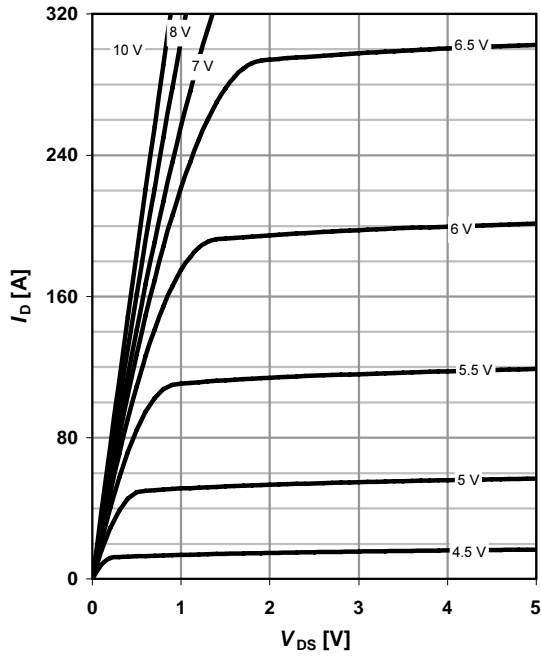
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

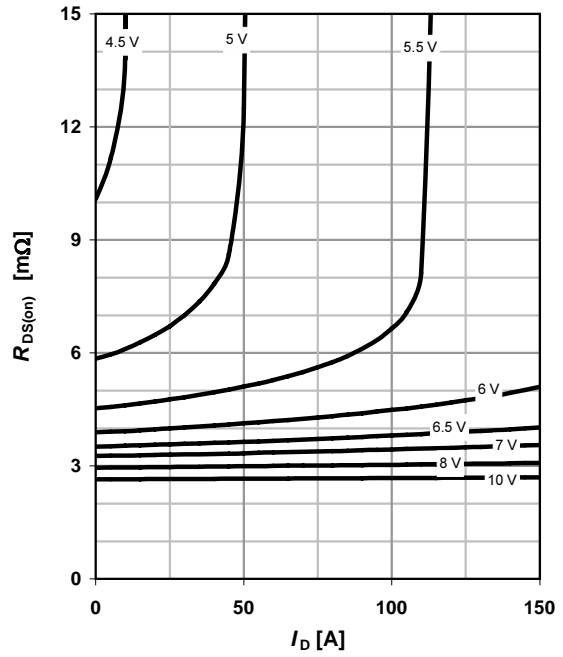
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

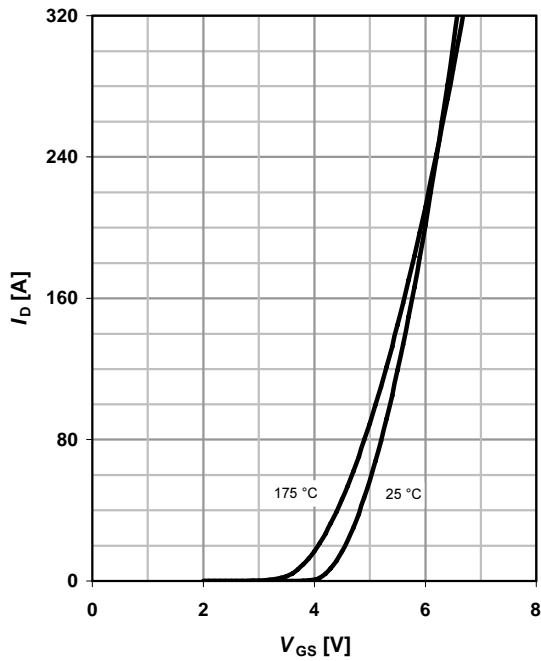
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

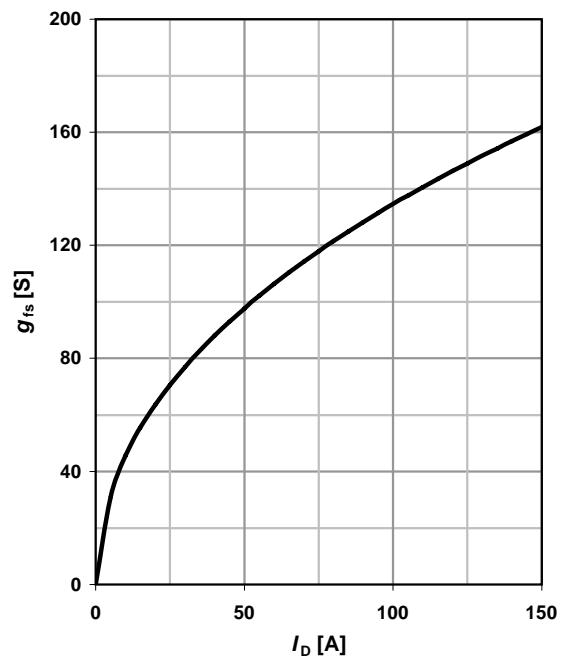
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



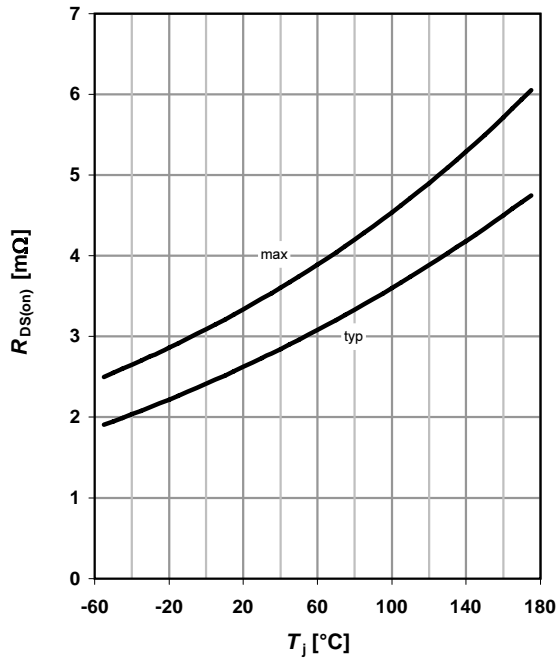
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



**9 Drain-source on-state resistance**

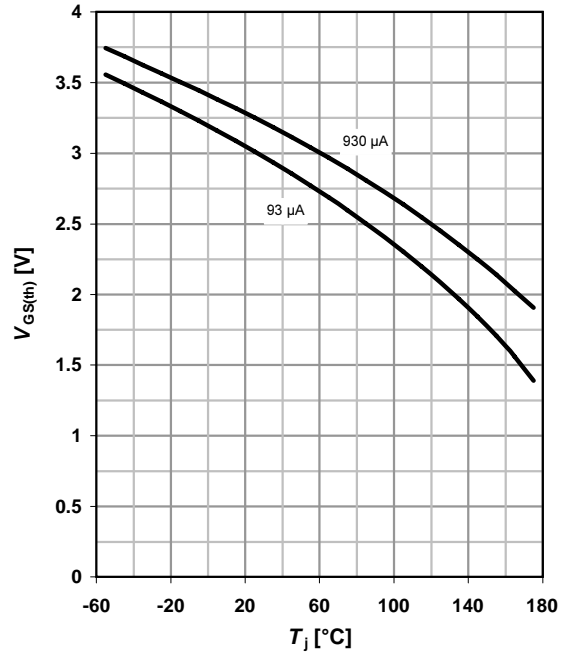
$$R_{DS(on)} = f(T_j); I_D = 100 \text{ A}; V_{GS} = 10 \text{ V}$$



**10 Typ. gate threshold voltage**

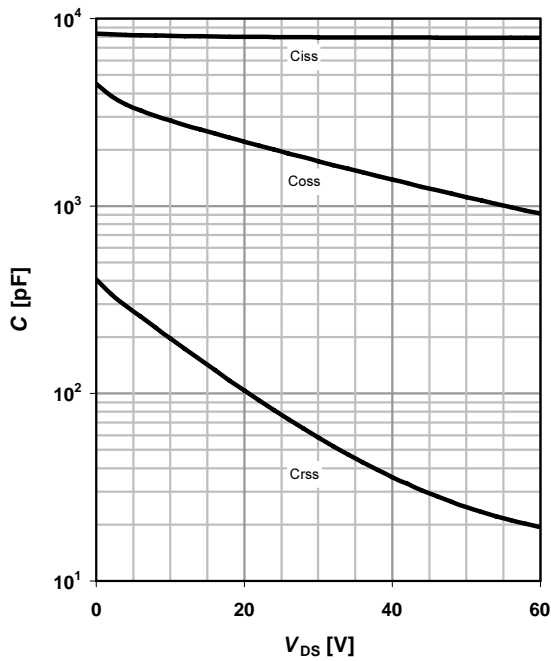
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$



**11 Typ. capacitances**

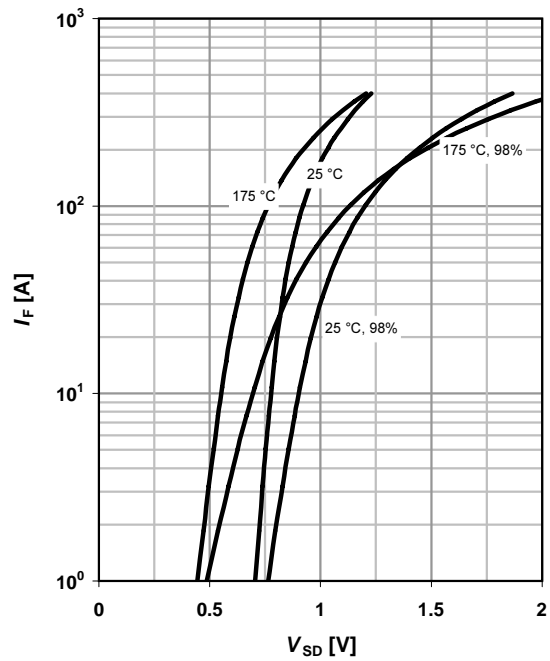
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



**12 Forward characteristics of reverse diode**

$$I_F = f(V_{SD})$$

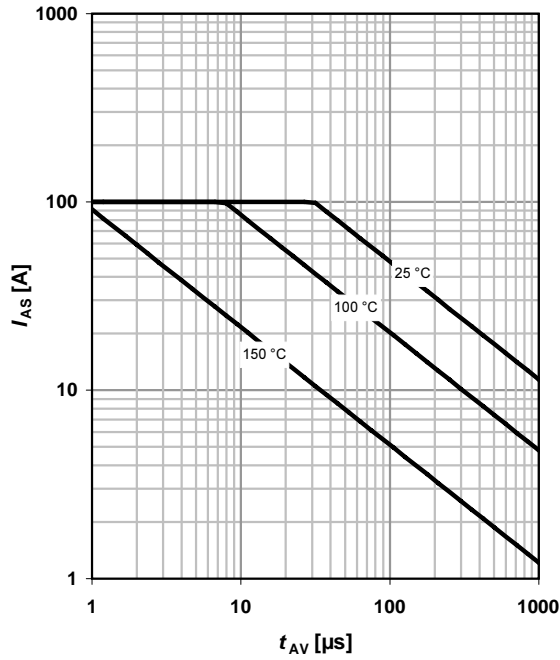
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

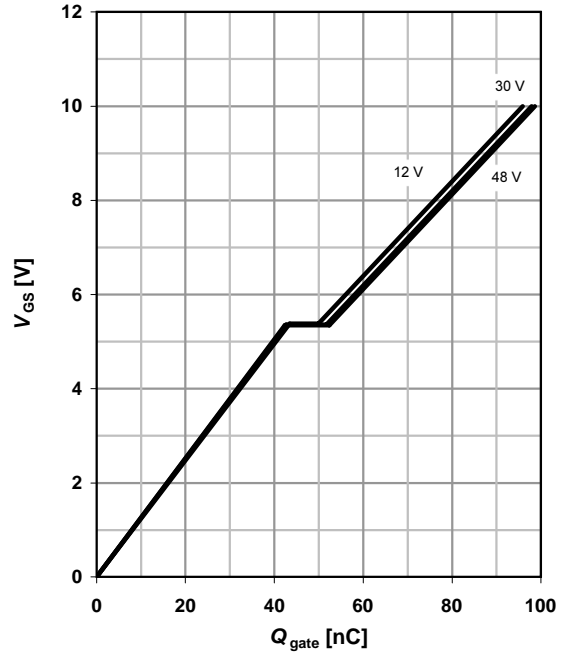
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

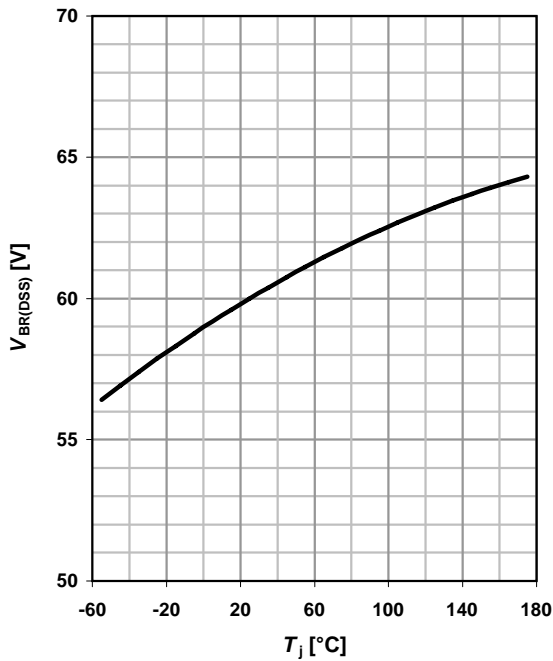
$V_{GS}=f(Q_{gate}); I_D=100 \text{ A pulsed}$

parameter:  $V_{DD}$



**15 Drain-source breakdown voltage**

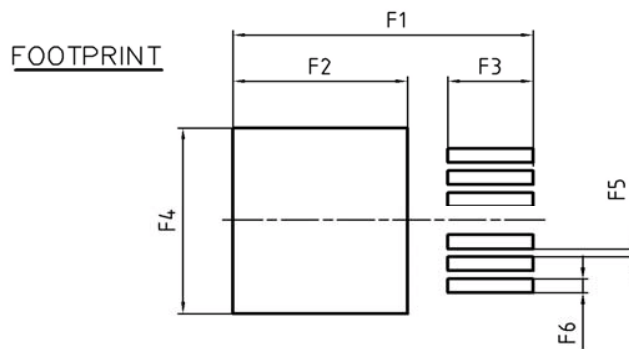
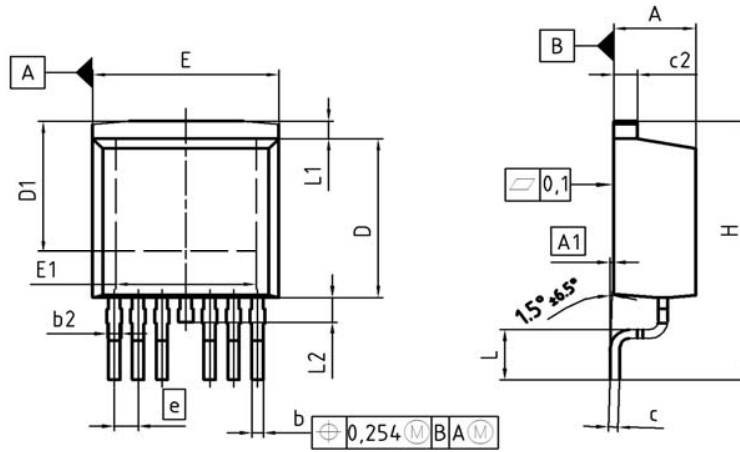
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



**16 Gate charge waveforms**



PG-TO263-7 (D<sup>2</sup>-Pak 7pin)



| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| A   | 4.30        | 4.57  | 0.169  | 0.180 |
| A1  | 0.00        | 0.25  | 0.000  | 0.010 |
| b   | 0.50        | 0.70  | 0.020  | 0.028 |
| b2  | 0.50        | 1.00  | 0.020  | 0.039 |
| c   | 0.33        | 0.65  | 0.013  | 0.026 |
| c2  | 1.17        | 1.40  | 0.046  | 0.055 |
| D   | 8.51        | 9.45  | 0.335  | 0.372 |
| D1  | 6.90        | 7.90  | 0.272  | 0.311 |
| E   | 9.80        | 10.31 | 0.386  | 0.406 |
| E1  | 6.50        | 8.60  | 0.256  | 0.339 |
| e   | 1.27        |       | 0.050  |       |
| N   | 6           |       | 6      |       |
| H   | 14.61       | 15.88 | 0.575  | 0.625 |
| L   | 2.29        | 3.00  | 0.090  | 0.118 |
| L1  | 0.70        | 1.60  | 0.028  | 0.063 |
| L2  | 1.00        | 1.78  | 0.039  | 0.070 |
| F1  | 16.05       | 16.25 | 0.632  | 0.640 |
| F2  | 9.30        | 9.50  | 0.366  | 0.374 |
| F3  | 4.50        | 4.70  | 0.177  | 0.185 |
| F4  | 10.70       | 10.90 | 0.421  | 0.429 |
| F5  | 0.37        | 0.57  | 0.015  | 0.022 |
| F6  | 0.70        | 0.90  | 0.028  | 0.035 |

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