

74LVCH162374A

16-bit edge-triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

Rev. 5 — 20 April 2021

Product data sheet

1. General description

The 74LVCH162374A is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. The device consists of two sections of 8 edge-triggered flip-flops. A clock (CP) input and an output enable (\overline{OE}) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications. The flip-flops store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW to HIGH CP transition. When \overline{OE} is LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

To reduce line noise, 30 Ω series termination resistors are included in both high and low output stages.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- High-impedance outputs when $V_{CC} = 0$ V
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|------------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVCH162374ADGG | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

4. Functional diagram

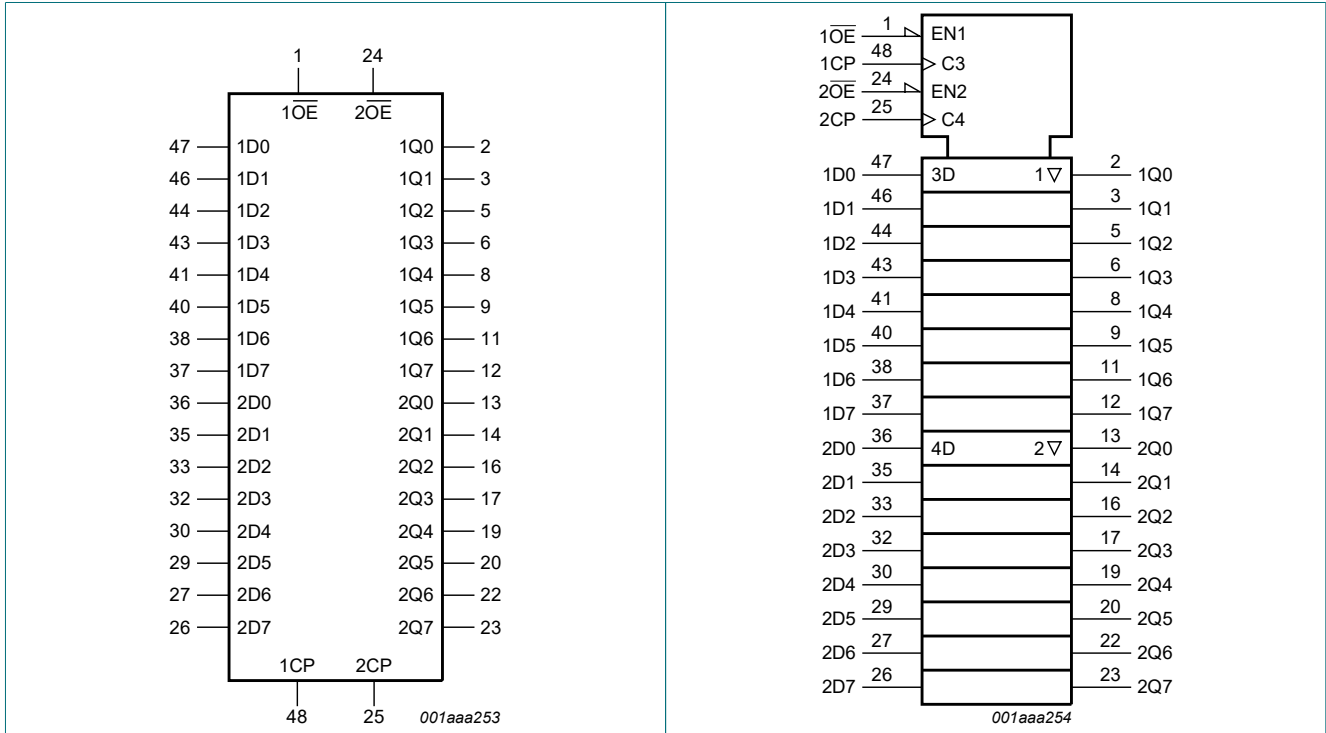


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

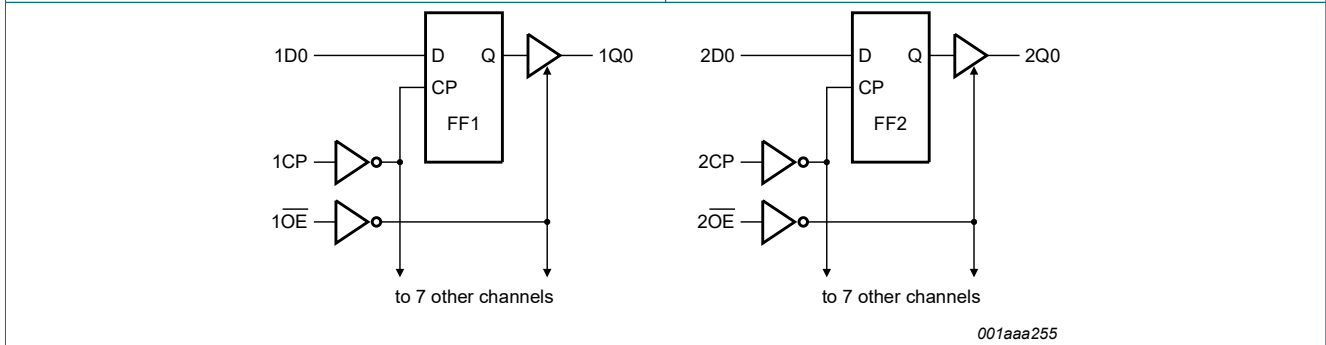


Fig. 3. Logic diagram

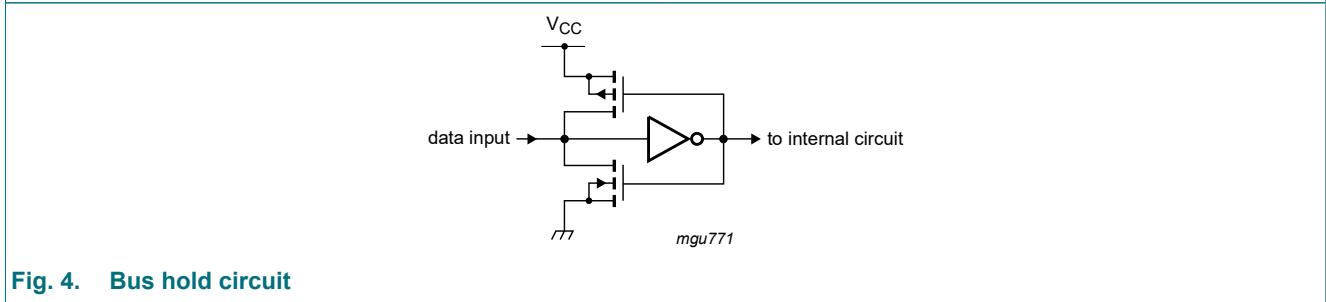


Fig. 4. Bus hold circuit

5. Pinning information

5.1. Pinning

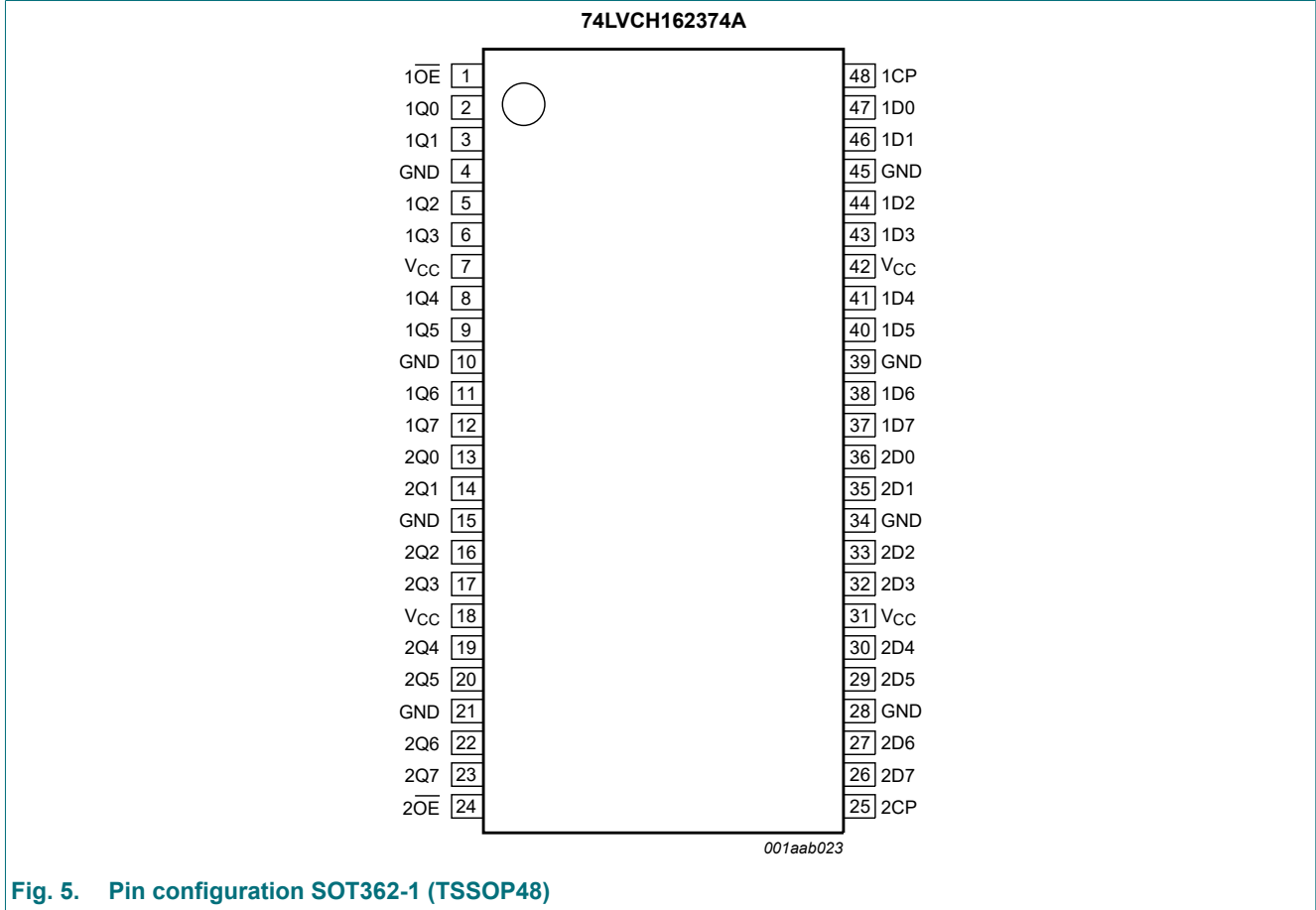


Fig. 5. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|--------------------------------|----------------------------------|
| 1OE, 2OE | 1, 24 | output enable input (active LOW) |
| 1CP, 2CP | 48, 25 | clock input |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7 | 2, 3, 5, 6, 8, 9, 11, 12 | data output |
| 2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7 | 13, 14, 16, 17, 19, 20, 22, 23 | data output |
| 1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input |
| 2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input |

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6. Functional description

Table 3. Function selection

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z = high-impedance OFF-state; \uparrow = LOW to HIGH CP transition

| Operation modes | Input | | | Internal flip-flop | Output nQ0 to nQ7 |
|------------------------------------|-------|------------|------------|--------------------|----------------------|
| | nOE | nCP | nD0 to nD7 | | |
| Load and read register | L | \uparrow | l | L | L |
| | L | \uparrow | h | H | H |
| Latch register and disable outputs | H | \uparrow | l | L | Z |
| | H | \uparrow | h | H | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|----------|----------------|--------------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ± 50 | mA |
| V_O | output voltage | output HIGH or LOW state | [2] -0.5 | $V_{CC} + 0.5$ | V |
| | | output 3-state | [2] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | $^{\circ}$ C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C | [3] - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages: P_{tot} derates linearly with 12.2 mW/K above 109 $^{\circ}$ C.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|----------------------------|------|-----|----------|--------------|
| V_{CC} | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | output HIGH or LOW state | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | $^{\circ}$ C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0 | - | 10 | ns/V |

16-bit edge-triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant;
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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit | |
|-----------------|---------------------------|---|-----------------------|-----------|---------------------|-----------------------|---------------------|----------|---------|
| | | | Min | Typ [1] | Max | Min | Max | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65V _{CC} | - | - | 0.65V _{CC} | - | V | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V | |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V | |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V | |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35V _{CC} | - | 0.35V _{CC} | V | |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V | |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | |
| | | I _O = -100 μ A; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.2 | - | - | V _{CC} - 0.3 | - | V | |
| | | I _O = -2 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V | |
| | | I _O = -4 mA; V _{CC} = 2.3 V | 1.7 | - | - | 1.55 | - | V | |
| | | I _O = -6 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | |
| | | I _O = 100 μ A; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V | |
| | | I _O = 2 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V | |
| | | I _O = 4 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V | |
| | | I _O = 6 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V | |
| I _I | input leakage current | V _{CC} = 3.6 V; V _I = 5.5 V or GND | [2] | - | \pm 0.1 | \pm 5 | - | \pm 20 | μ A |
| | | V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND | [2] | - | \pm 0.1 | \pm 5 | - | \pm 20 | μ A |
| | | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | \pm 0.1 | \pm 10 | - | \pm 20 | μ A | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.1 | 20 | - | 80 | μ A | |
| | | per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 5 | 500 | - | 5000 | μ A | |
| C _I | input capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 5.0 | - | - | - | pF | |

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| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-------------------|---------------------------------|---|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| I _{BHL} | bus hold LOW current | V _{CC} = 1.65; V _I = 0.58 V [3] [4] | 10 | - | - | 10 | - | μA |
| | | V _{CC} = 2.3; V _I = 0.7 V | 30 | - | - | 25 | - | μA |
| | | V _{CC} = 3.0; V _I = 0.8 V | 75 | - | - | 60 | - | μA |
| I _{BHH} | bus hold HIGH current | V _{CC} = 1.65; V _I = 1.07 V [3] [4] | -10 | - | - | -10 | - | μA |
| | | V _{CC} = 2.3; V _I = 1.7 V | -30 | - | - | -25 | - | μA |
| | | V _{CC} = 3.0; V _I = 2.0 V | -75 | - | - | -60 | - | μA |
| I _{BHLO} | bus hold LOW overdrive current | V _{CC} = 1.95 V [3] [5] | 200 | - | - | 200 | - | μA |
| | | V _{CC} = 2.7 V | 300 | - | - | 300 | - | μA |
| | | V _{CC} = 3.6 V | 500 | - | - | 500 | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current | V _{CC} = 1.95 V [3] [5] | -200 | - | - | -200 | - | μA |
| | | V _{CC} = 2.7 V | -300 | - | - | -300 | - | μA |
| | | V _{CC} = 3.6 V | -500 | - | - | -500 | - | μA |

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.

[3] For data inputs only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs do not have a bus hold circuit.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------|------------------------------------|-------------------------------------|---------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _{pd} | propagation delay | nCP to nQn; see Fig. 6 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 14 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 2.6 | 8.3 | 18.0 | 2.6 | 20.8 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.8 | 4.4 | 8.8 | 1.8 | 10.2 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 4.0 | 7.8 | 1.5 | 10.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.7 | 6.8 | 1.5 | 8.5 | ns |
| t _{en} | enable time | nOE to nQn; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 20 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.9 | 7.5 | 17.1 | 1.9 | 19.7 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.5 | 4.2 | 9.0 | 1.5 | 10.3 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 4.5 | 8.3 | 1.5 | 10.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.4 | 6.6 | 1.5 | 8.5 | ns |
| t _{dis} | disable time | nOE to nQn; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 12 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 2.7 | 4.5 | 8.0 | 2.7 | 9.3 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.5 | 4.3 | 1.0 | 5.0 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.3 | 4.6 | 1.5 | 6.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.1 | 4.4 | 1.5 | 5.5 | ns |

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| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|--------------------|-------------------------------|--------------------------------------|-------------------------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _w | pulse width | nCP HIGH; see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 5.0 | - | - | 5.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 4.0 | - | - | 4.0 | - | ns |
| | | V _{CC} = 2.7 V | 3.0 | | - | 3.0 | - | ns |
| t _{su} | set-up time | nDn to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 4.0 | - | - | 4.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 3.0 | - | - | 3.0 | - | ns |
| | | V _{CC} = 2.7 V | 1.9 | - | - | 1.9 | - | ns |
| t _h | hold time | nDn to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 3.0 | - | - | 3.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 2.5 | - | - | 2.5 | - | ns |
| | | V _{CC} = 2.7 V | 1.5 | - | - | 1.5 | - | ns |
| f _{max} | maximum frequency | see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 100 | - | - | 80 | - | MHz |
| | | V _{CC} = 2.3 V to 2.7 V | 125 | - | - | 100 | - | MHz |
| | | V _{CC} = 2.7 V | 150 | - | - | 120 | - | MHz |
| t _{sk(o)} | output skew time | V _{CC} = 3.0 V to 3.6 V [3] | - | - | 1.0 | - | 1.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V [4] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | - | 9.6 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 11.7 | - | - | - | pF |
| C _{PD} | power dissipation capacitance | V _{CC} = 3.0 V to 3.6 V | - | 13.5 | - | - | - | pF |
| | | V _{CC} = 3.0 V to 3.6 V | - | 13.5 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

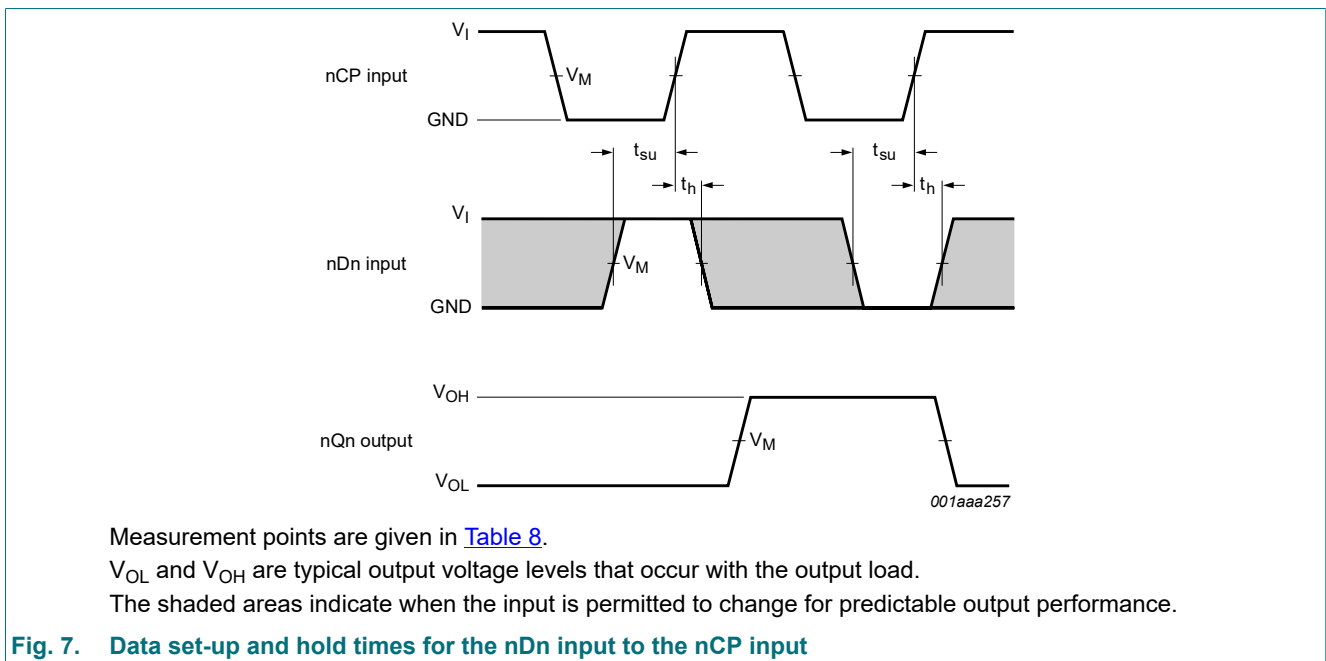
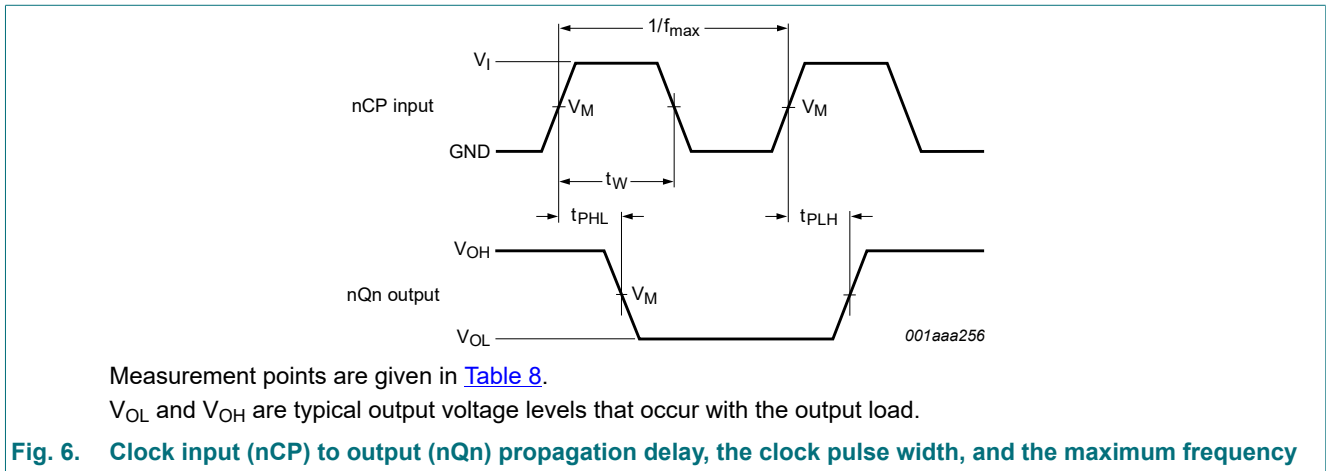
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1. Waveforms and test circuit



16-bit edge-triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

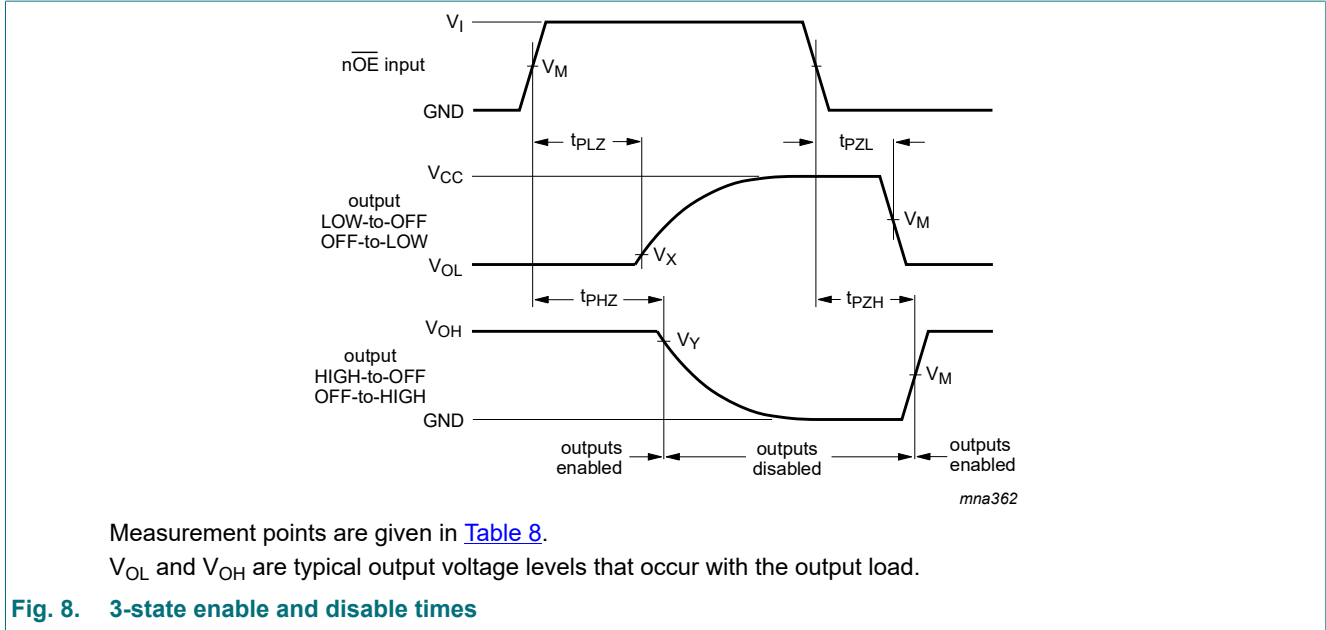
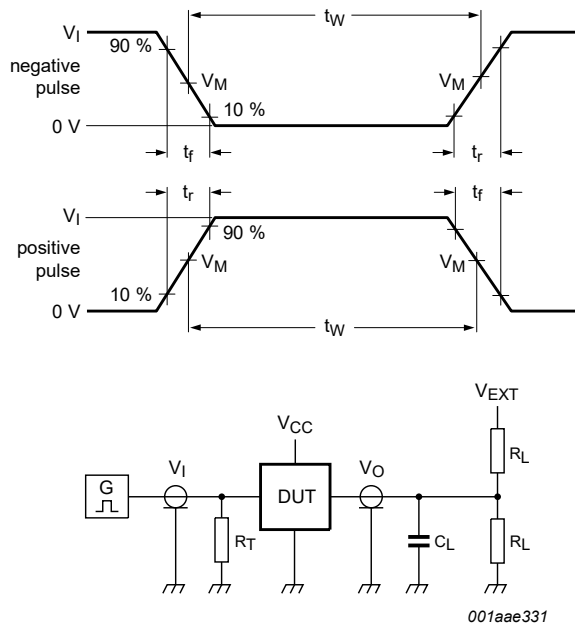


Table 8. Measurement points

| Supply voltage | Input | | Output | | |
|------------------|----------|---------------------|---------------------|---------------------------|---------------------------|
| V_{CC} | V_I | V_M | V_M | V_X | V_Y |
| 1.2 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 1.65 V to 1.95 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.3 V to 2.7 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |

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Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|-------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 1.2 V | V_{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

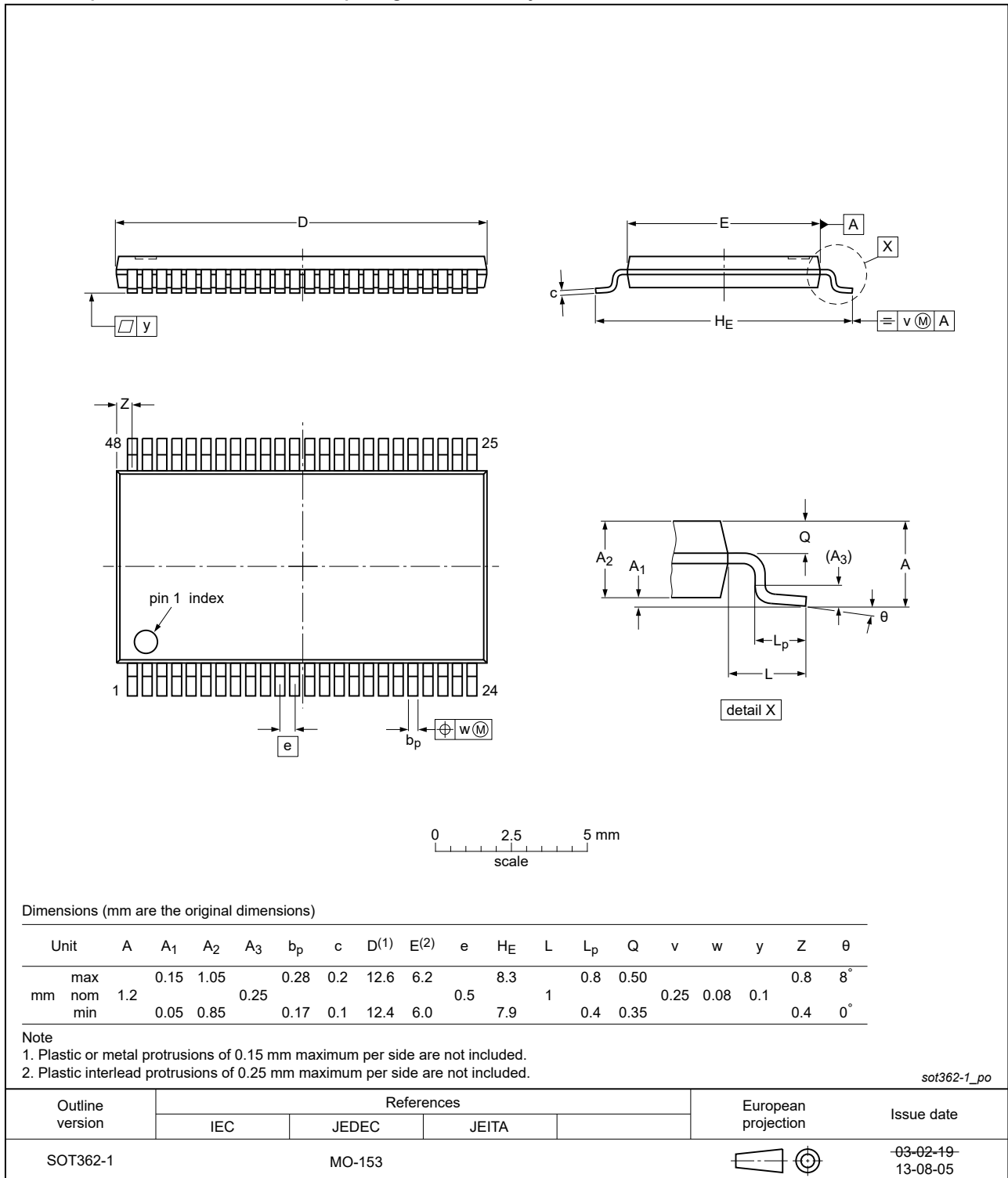


Fig. 10. Package outline SOT362-1 (TSSOP48)

16-bit edge-triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant;
3-state

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|---|-----------------------|---------------|-----------------------|
| 74LVCH162374A v.5 | 20210420 | Product data sheet | - | 74LVCH162374A v.4 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVCH162374ADL (SOT370-1 / SSOP48) removed. Section 7: Derating values for P_{tot} total power dissipation updated. Fig. 10: Package outline drawing SOT362-1 (TSSOP48) updated. | | | |
| 74LVCH162374A v.4 | 20130122 | Product data sheet | - | 74LVCH162374A v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges. | | | |
| 74LVCH162374A v.3 | 20040519 | Product specification | - | 74LVC_LVCH162374A v.2 |
| 74LVC_LVCH162374A v.2 | 20040325 | Product specification | - | 74LVC_LVCH162374A v.1 |
| 74LVC_LVCH162374A v.1 | 19990805 | Product specification | - | - |

16-bit edge-triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 20 April 2021
