

## 1. General description

AC Thyristor power switch in a SOT54 (TO-92) plastic package with self-protective capabilities against low and high energy transients.

## 2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- Remote gate separates the gate driver from the effects of the load current
- Safe clamping of low energy over-voltage transients
- High voltage capability
- Self-protective turn-on during high energy voltage transients
- Very high noise immunity

## 3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

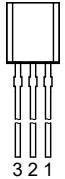
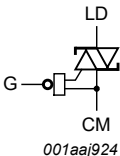
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 75\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	0.8	A
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	1	-	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD- G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	1	-	10	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>TO-92 (SOT54)</p>	
2	G	gate		
3	LD	load		

## 6. Ordering information

Table 3. Ordering information

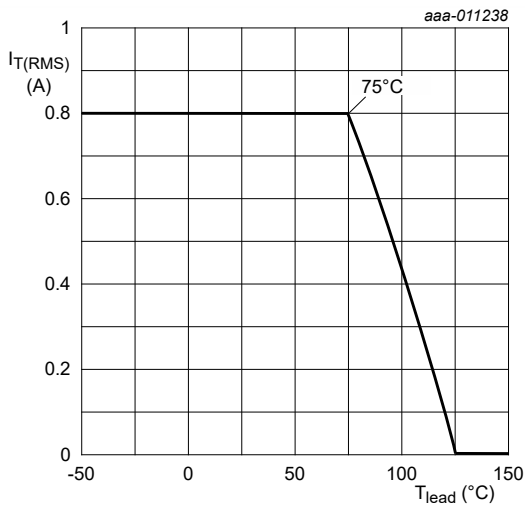
Type number	Package		
	Name	Description	Version
ACT108-800E	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 7. Limiting values

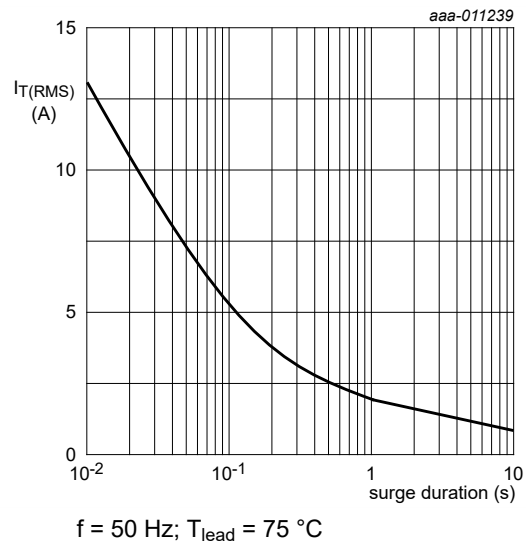
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 75\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	13	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	14.3	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse	-	0.84	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_G = 20\text{ mA}$	-	100	A/ $\mu$ s
$I_{GM}$	peak gate current	$t = 20\text{ }\mu$ s	-	1	A
$V_{GM}$	peak gate voltage	positive applied gate voltage	-	15	V
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C
$V_{PP}$	peak pulse voltage	$T_j = 25\text{ °C}$ ; non-repetitive, off-state; ten pulses on each voltage polarity; 20s or more between successive pulses; <a href="#">Fig. 6</a>	-	2.5	kV



**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**



$f = 50\text{ Hz}$ ;  $T_{lead} = 75\text{ °C}$

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

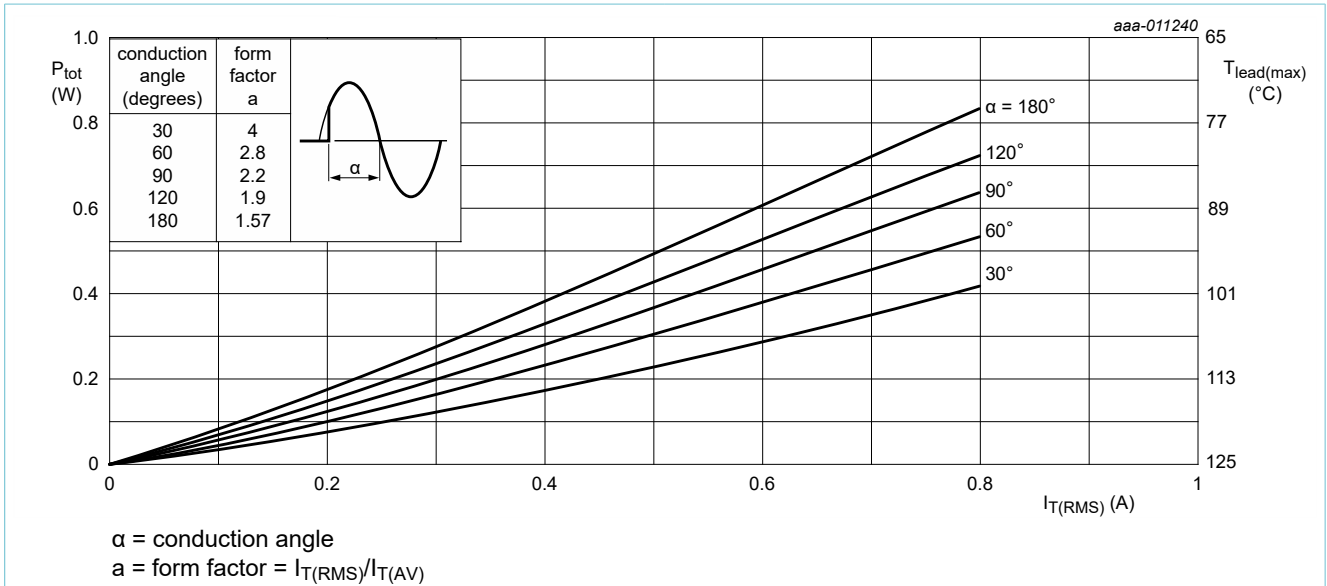


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

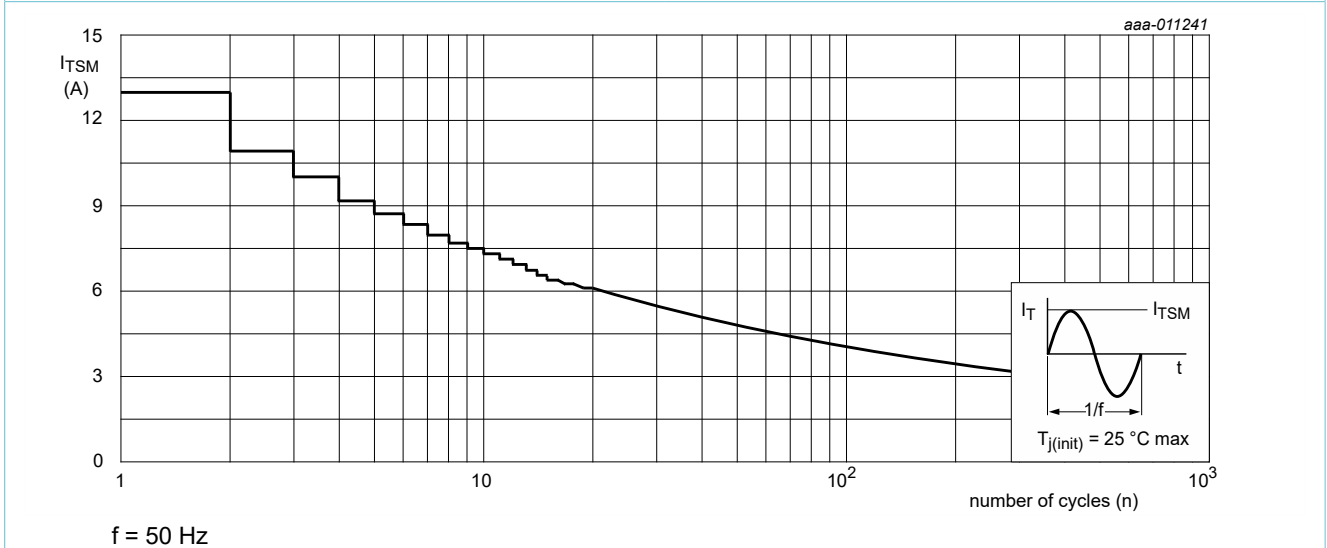


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

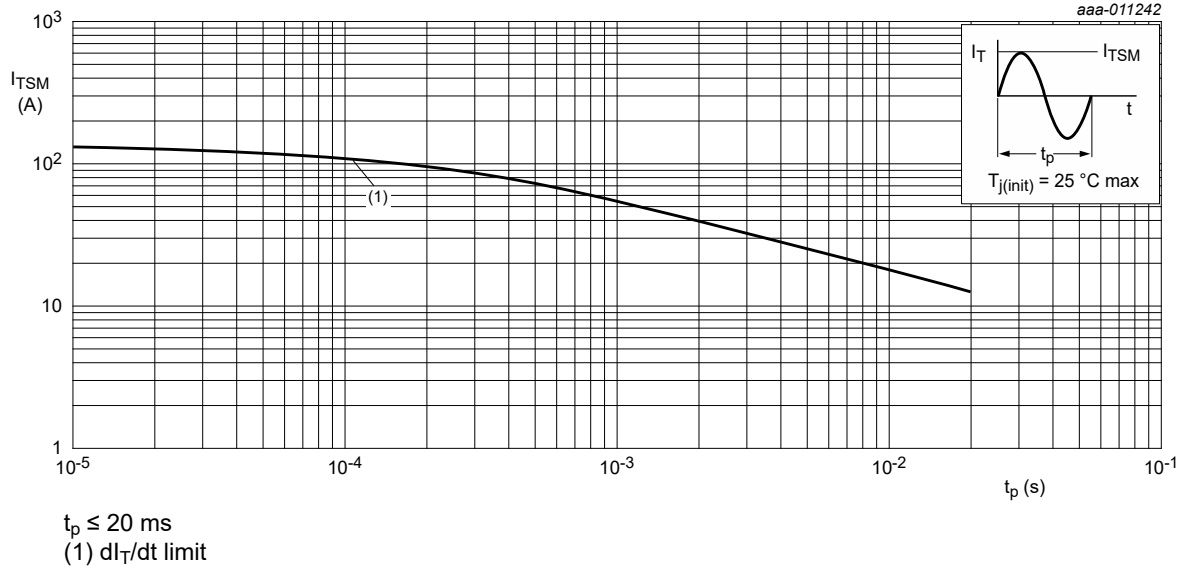


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

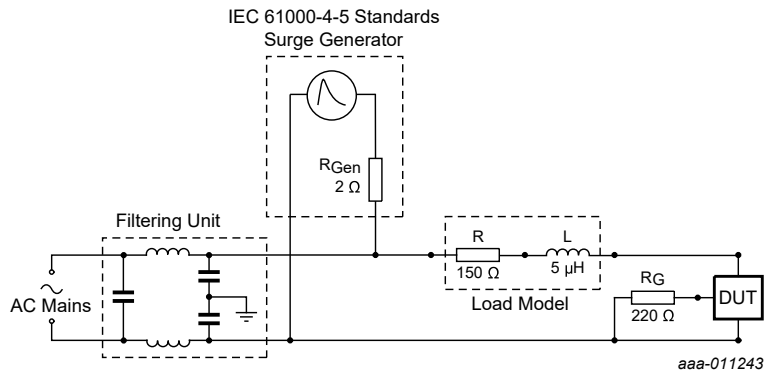


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

### 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle with heatsink compound; <a href="#">Fig. 7</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	full cycle; printed-circuit board mounted; lead length 4 mm	-	150	-	K/W

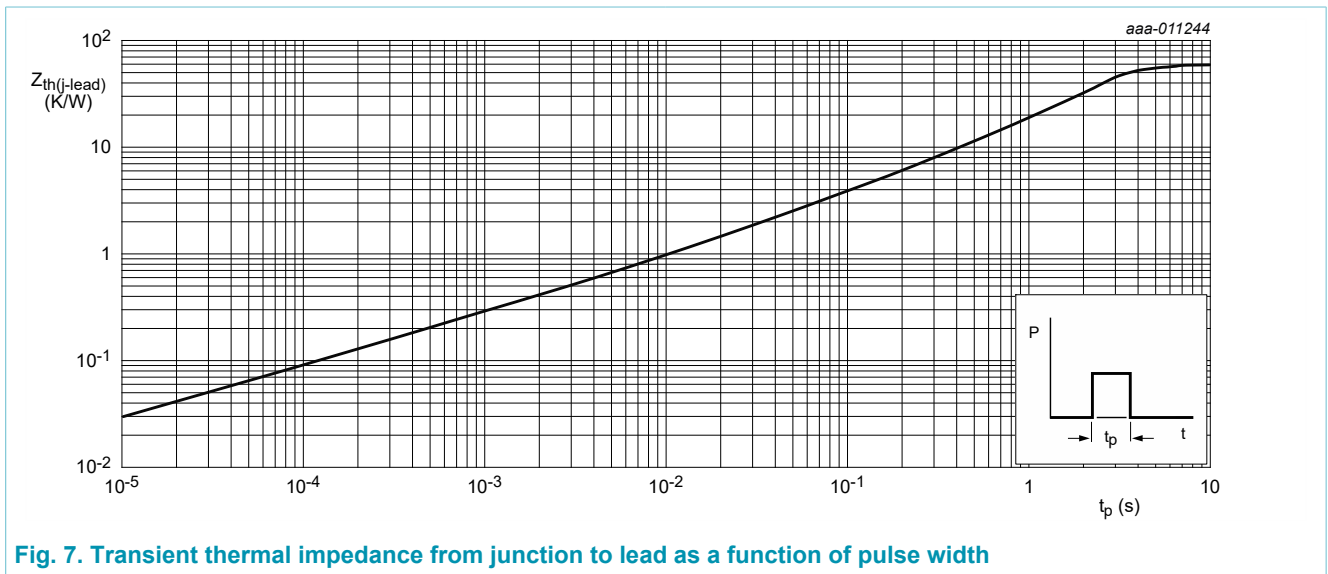
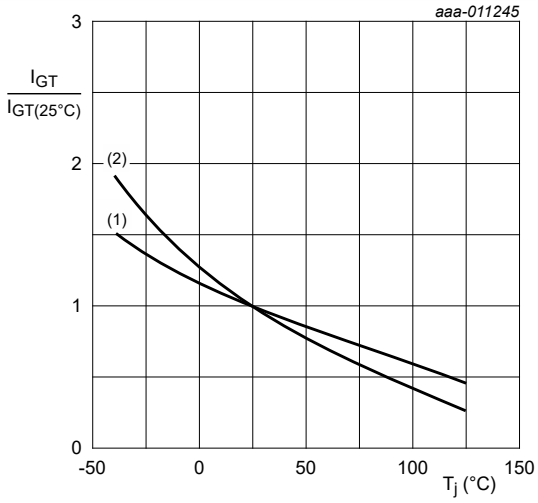


Fig. 7. Transient thermal impedance from junction to lead as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	1	-	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	1	-	10	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 100\text{ mA}$ ; LD+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	-	25	mA
		$V_D = 12\text{ V}$ ; $I_G = 100\text{ mA}$ ; LD- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	-	20	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	-	20	mA
$V_T$	on-state voltage	$I_T = 1.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	-	1.3	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 12</a>	-	-	1	V
		$V_D = 400\text{ V}$ ; $I_T = 100\text{ mA}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; <a href="#">Fig. 12</a>	0.15	-	-	V
$I_D$	off-state current	$V_D = 800\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_D = 800\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$	-	-	0.2	mA
$V_{CL}$	clamping voltage	$I_{CL} = 0.1\text{ mA}$ ; $t_p = 1\text{ ms}$ ; $T_j = 25\text{ }^\circ\text{C}$	850	-	-	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 13</a>	500	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 0.8\text{ A}$ ; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$ ; (snubberless condition); gate open circuit; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	0.5	-	-	A/ms



(1) LD+ G-  
(2) LD- G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

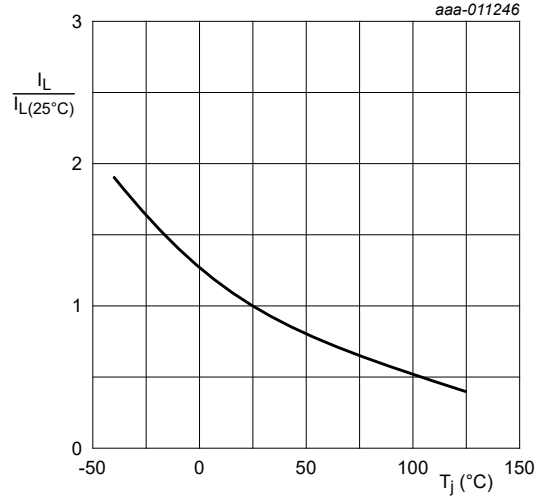


Fig. 9. Normalized latching current as a function of junction temperature

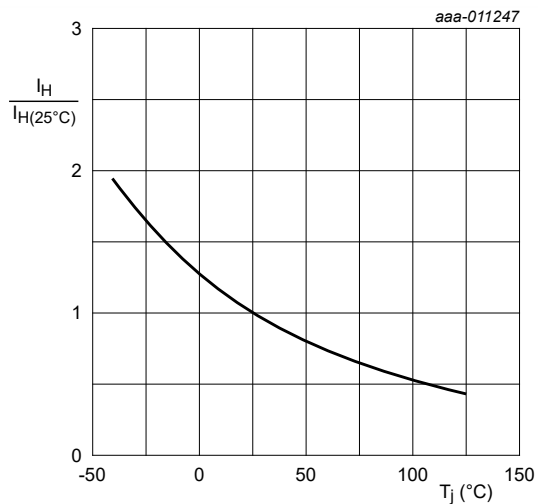
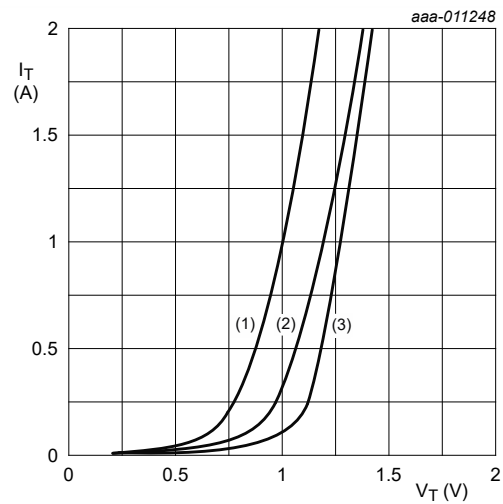


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 0.967 \text{ V}; R_s = 0.225 \Omega$

- (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values
- (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values
- (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

Fig. 11. On-state current as a function of on-state voltage



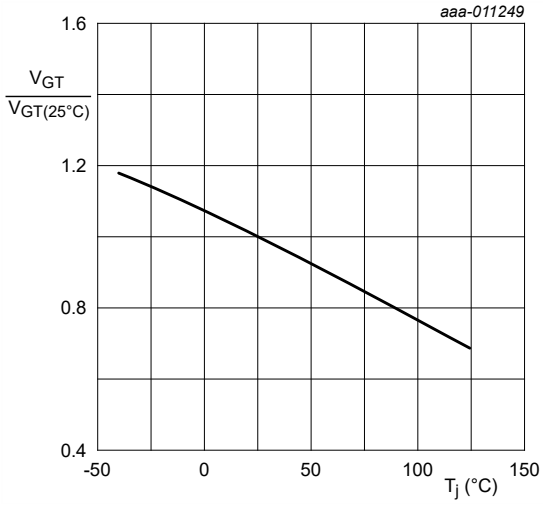
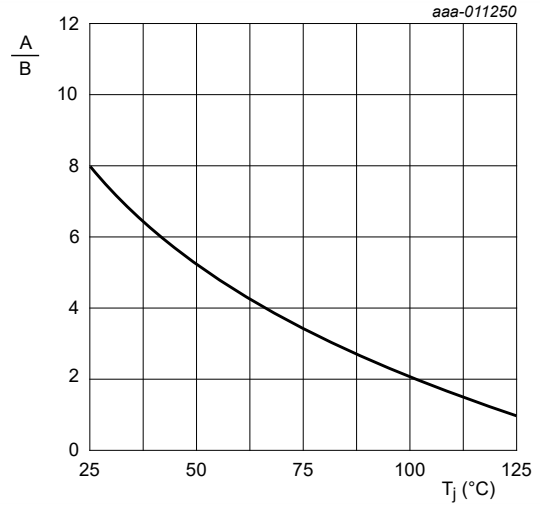
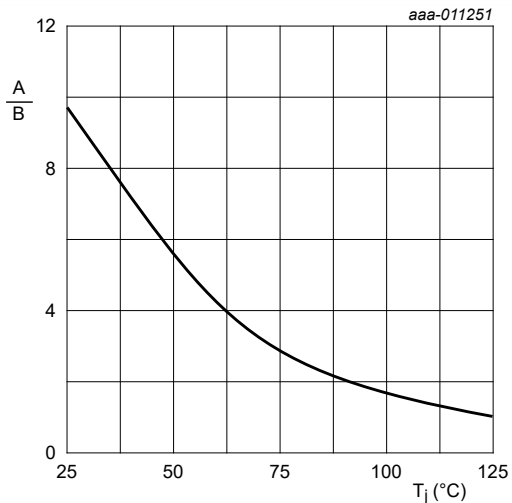


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



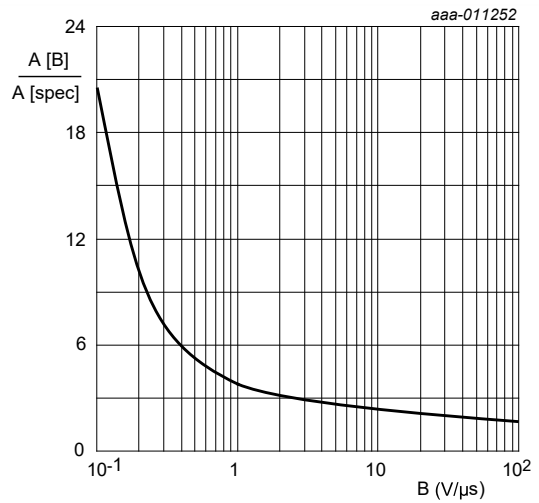
A =  $dV_D/dt$  at condition  $T_j$  °C  
 B =  $dV_D/dt$  at condition  $T_j$  [125] °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A =  $di_{com}/dt$  at condition  $T_j$  °C  
 B =  $di_{com}/dt$  at condition  $T_j$  [125] °C  
 $V_D = 400$  V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] =  $di_{com}/dt$  at condition B,  $dV_{com}/dt$   
 A [spec] is the data sheet value for  $di_{com}/dt$   
 turn-off time is less than 20 ms

Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

### 10. Package outline



Fig. 16. Package outline TO-92 (SOT54)

## 11. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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