

Features

- Zero Input Output Propagation Delay, adjustable by Capacitive Load on FBK input
- Multiple configurations (see Table 3 on page 4)
- Multiple Low-skew Outputs
 - 45 ps Typical Output-output skew (-1)
 - Two banks of four Outputs, three-stateable by two select Inputs
- 10 MHz to 140 MHz Operating Range
- 65 ps Typical Cycle-to-cycle Jitter (-1, -1H)
- Advanced 0.65 μm CMOS Technology
- Space saving 16-pin, SOIC and TSSOP Packages
- 3.3V Operation
- Spread Aware

Functional Description

The CY23S08 is a 3.3V zero delay buffer designed to distribute high speed clocks in PC, workstation, datacom, telecom, and other high performance applications.

The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback must be driven into the FBK pin, and obtained from one of the outputs. The input-to-output propagation delay is less than 350 ps, and output-to-output skew is less than 250 ps.

The CY23S08 has two banks of four outputs each, which can be controlled by the Select inputs as shown in Table 2 on page 4. If all output clocks are not required, Bank B can be three-stated. The select inputs also enable the input clock to be directly applied to the output for chip and system testing purposes.

The CY23S08 PLL enters a power down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 μA of current draw. The PLL shuts down in two additional cases as shown in Table 2 on page 4.

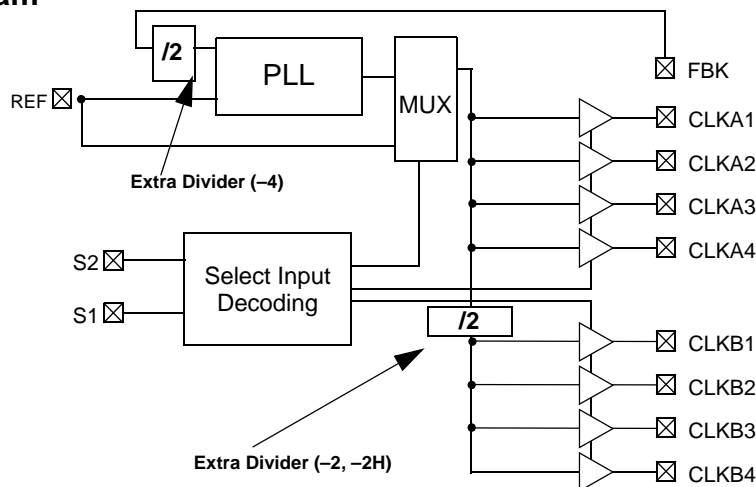
Multiple CY23S08 devices accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is less than 700 ps.

The CY23S08 is available in five different configurations, as shown in Table 3 on page 4. The CY23S08-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The CY23S08-1H is the high drive version of the -1, and rise and fall times on this device are much faster.

The CY23S08-2 enables you to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. The CY23S08-2H is the high drive version of the -2, and rise and fall times on this device are much faster.

The CY23S08-4 enables you to obtain 2X clocks on all outputs. Thus, the part is versatile, and can be used in a variety of applications.

Logic Block Diagram



Contents

| | | | |
|---|----------|--|-----------|
| 3.3V Zero Delay Buffer | 1 | Switching Characteristics for CY23S08SXC-xx | |
| Features | 1 | Commercial Temperature Devices | 5 |
| Functional Description | 1 | Switching Waveforms | 7 |
| Logic Block Diagram | 1 | Test Circuits | 8 |
| Contents | 2 | Ordering Information | 9 |
| Pinouts | 3 | Package Drawings and Dimensions | 10 |
| Spread Aware | 4 | Document History Page | 12 |
| Maximum Ratings | 5 | Sales, Solutions, and Legal Information | 13 |
| Operating Conditions | 5 | Worldwide Sales and Design Support | 13 |
| Electrical Characteristics for CY23S08SXC-xx | | Products | 13 |
| Commercial Temperature Devices | 5 | PSoC Solutions | 13 |

Pinouts

Figure 1. Pin Configuration – 16-Pin Package

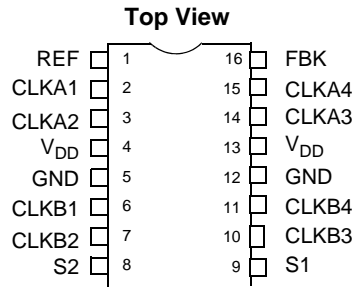


Table 1. Pin Definition

| Pin | Signal | Description |
|-----|----------------------|--|
| 1 | REF ^[1] | Input reference frequency, 5V tolerant input |
| 2 | CLKA1 ^[2] | Clock output, Bank A |
| 3 | CLKA2 ^[2] | Clock output, Bank A |
| 4 | V _{DD} | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ^[2] | Clock output, Bank B |
| 7 | CLKB2 ^[2] | Clock output, Bank B |
| 8 | S2 ^[3] | Select input, bit 2 |
| 9 | S1 ^[3] | Select input, bit 1 |
| 10 | CLKB3 ^[2] | Clock output, Bank B |
| 11 | CLKB4 ^[2] | Clock output, Bank B |
| 12 | GND | Ground |
| 13 | V _{DD} | 3.3V supply |
| 14 | CLKA3 ^[2] | Clock output, Bank A |
| 15 | CLKA4 ^[2] | Clock output, Bank A |
| 16 | FBK | PLL feedback input |

Notes

1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

Table 2. Select Input Decoding

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | Output Source | PLL Shutdown |
|----|----|-------------|-------------|---------------|--------------|
| 0 | 0 | Three-State | Three-State | PLL | Y |
| 0 | 1 | Driven | Three-State | PLL | N |
| 1 | 0 | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | PLL | N |

Table 3. Available CY23S08 Configurations

| Device | Feedback From | Bank A Frequency | Bank B Frequency |
|------------|------------------|------------------|------------------|
| CY23S08–1 | Bank A or Bank B | Reference | Reference |
| CY23S08–1H | Bank A or Bank B | Reference | Reference |
| CY23S08–2 | Bank A | Reference | Reference/2 |
| CY23S08–2H | Bank A | Reference | Reference/2 |
| CY23S08–2 | Bank B | 2 X Reference | Reference |
| CY23S08–2H | Bank B | 2 X Reference | Reference |
| CY23S08–4 | Bank A or Bank B | 2 X Reference | 2 X Reference |

Spread Aware

Many systems designed now use the Spread Spectrum Frequency Timing Generation (SSFTG) technology. Cypress is one of the pioneers of SSFTG development, and designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer does not pass through the SS feature, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see Cypress's application note [EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator \(SSFTG\) ICs](#).

Note

- Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the CY23S08–2.

Maximum Ratings

| | | | |
|---|--------------------------|---|--------|
| Supply Voltage to Ground Potential..... | -0.5V to +7.0V | Max Soldering Temperature (10 sec.) | 260°C |
| DC Input Voltage (Except Ref) | -0.5V to $V_{DD} + 0.5V$ | Junction Temperature | 150°C |
| DC Input Voltage REF | -0.5 to 7V | Static Discharge Voltage | |
| Storage Temperature | -65°C to +150°C | (per MIL-STD-883, Method 3015) | >2000V |

Operating Conditions

| Parameter ^[5] | Description | Min | Max | Unit |
|--------------------------|---|-----|-----|------|
| V_{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T_A | Ambient Operating Temperature, Commercial | 0 | 70 | °C |
| | Ambient Operating Temperature, Industrial | -40 | 85 | °C |
| C_L | Load Capacitance, below 100 MHz | — | 30 | pF |
| | Load Capacitance, from 100 MHz to 140 MHz | — | 15 | pF |
| C_{IN} | Input Capacitance ^[6] | — | 7 | pF |

Electrical Characteristics for CY23S08SXC-xx Commercial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|------------------------------------|---|-----|--------------------|------|
| V_{IL} | Input LOW Voltage | | — | 0.8 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | — | V |
| I_{IL} | Input LOW Current | $V_{IN} = 0V$ | — | 50.0 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | — | 100.0 | μA |
| V_{OL} | Output LOW Voltage ^[7] | $I_{OL} = 8\text{ mA } (-1, -2, -4)$ $I_{OL} = 12\text{ mA } (-1H, -2H)$ | — | 0.4 | V |
| V_{OH} | Output HIGH Voltage ^[7] | $I_{OH} = -8\text{ mA } (-1, -2, -4)$ $I_{OH} = -12\text{ mA } (-1H, -2H)$ | 2.4 | — | V |
| I_{DD} (PD mode) | Power down Supply Current | REF = 0 MHz | — | 12.0 | μA |
| I_{DD} | Supply Current | Unloaded outputs, 100 MHz REF, Select inputs at V_{DD} or GND | — | 45.0 | mA |
| | | | — | 70.0 (-1H, -2H) | mA |
| | | Unloaded outputs, 66 MHz REF (-1,-2,-4) | — | 32.0 | mA |
| | | Unloaded outputs, 33 MHz REF (-1,-2,-4) | — | 18.0 | mA |

Switching Characteristics for CY23S08SXC-xx Commercial Temperature Devices

| Parameter ^[8] | Name | Test Conditions | Min | Typ | Max | Unit |
|--------------------------|---|---|------|------|-------|------|
| t_1 | Output Frequency | 30 pF load, -1, -1H, -2 devices | 10 | — | 100 | MHz |
| t_1 | Output Frequency | 30 pF load, -4 devices | 15 | — | 100 | MHz |
| t_1 | Output Frequency | 20 pF load, -1H device | 10 | — | 133.3 | MHz |
| t_1 | Output Frequency | 15 pF load, -1, -2 devices | 10 | — | 140.0 | MHz |
| t_1 | Output Frequency | 15 pF load, -4 devices | 15 | — | 140.0 | MHz |
| | Duty Cycle ^[7] = $t_2 \div t_1$ (-1,-2,-4,-1H, -2H) | Measured at $V_{DD}/2$, $F_{OUT} = 66.66\text{ MHz}$ 30-pF load | 40.0 | 50.0 | 60.0 | % |
| | Duty Cycle ^[7] = $t_2 \div t_1$ (-1,-2,-4,-1H, -2H) | Measured at $V_{DD}/2$, $F_{OUT} < 66.66\text{ MHz}$ 15 pF load | 45.0 | 50.0 | 55.0 | % |

Notes

- Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
- Applies to both Ref Clock and FBK.
- Parameter is guaranteed by design and characterization. Not 100% tested in production.
- All parameters are specified with loaded outputs.

Switching Characteristics for CY23S08SXC-xx Commercial Temperature Devices (continued)

| Parameter ^[8] | Name | Test Conditions | Min | Typ | Max | Unit |
|--------------------------|--|---|------|-----|------|------|
| t ₃ | Rise Time ^[7] (-1, -2, -4) | Measured between 0.8V and 2.0V, 30 pF load | — | — | 2.20 | ns |
| t ₃ | Rise Time ^[7] (-1, -2, -4) | Measured between 0.8V and 2.0V, 15 pF load | — | — | 1.50 | ns |
| t ₃ | Rise Time ^[7] (-1H, -2H) | Measured between 0.8V and 2.0V, 30 pF load | — | — | 1.50 | ns |
| t ₄ | Fall Time ^[7] (-1, -2, -4) | Measured between 0.8V and 2.0V, 30 pF load | — | — | 2.20 | ns |
| t ₄ | Fall Time ^[7] (-1, -2, -4) | Measured between 0.8V and 2.0V, 15 pF load | — | — | 1.50 | ns |
| t ₄ | Fall Time ^[7] (-1H, 2H) | Measured between 0.8V and 2.0V, 30 pF load | — | — | 1.25 | ns |
| t ₅ | Output to Output Skew on same Bank (-1) ^[7] | All outputs equally loaded | — | 45 | 200 | ps |
| | Output to Output Skew on same Bank (-1H,-2,-2H) ^[7] | All outputs equally loaded | — | 105 | 150 | ps |
| | Output to Output Skew on same Bank (-4) ^[7] | All outputs equally loaded | — | 70 | 100 | ps |
| | Output to Output Skew (-1H, -2H) | All outputs equally loaded | — | — | 200 | ps |
| | Output Bank A to Output Bank B Skew (-1,-2) | All outputs equally loaded | — | — | 300 | ps |
| | Output Bank A to Output Bank B Skew (-4) | All outputs equally loaded | — | — | 215 | ps |
| | Output Bank A to Output Bank B Skew (-1H) | All outputs equally loaded | — | — | 250 | ps |
| t ₆ | Delay, REF Rising Edge to FBK Rising Edge ^[7] | Measured at V _{DD} /2 | -250 | — | +275 | ps |
| t ₇ | Device to Device Skew ^[7] | Measured at V _{DD} /2 on the FBK pins of devices | — | — | 700 | ps |
| t ₈ | Output Slew Rate ^[7] | Measured between 0.8V and 2.0V on -1H, -2H device using Test Circuit #2 | 1 | — | — | V/ns |
| t _J | Cycle to Cycle Jitter ^[7] (-1, -1H) | Measured at 66.67 MHz, loaded outputs, 15, 30 pF loads: 133 MHz, 15 pF load | — | 65 | 125 | ps |
| | Cycle to Cycle Jitter ^[7] (-2) | Measured at 66.67 MHz, loaded outputs, 15 pF load | — | 85 | 300 | ps |
| | Cycle to Cycle Jitter ^[7] (-2) | Measured at 66.67 MHz, loaded outputs, 30 pF load | — | — | 400 | ps |
| t _J | Cycle to Cycle Jitter ^[7] (-4) | Measured at 66.67 MHz, loaded outputs 15, 30 pF loads | — | — | 200 | ps |
| t _{LOCK} | PLL Lock Time ^[7] | Stable power supply, valid clocks presented on REF and FBK pins | — | — | 1.0 | ms |

Switching Waveforms

Figure 2. Duty Cycle Timing

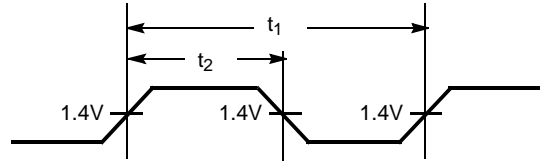


Figure 3. All Outputs Rise and Fall Time

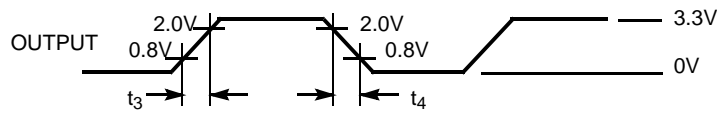


Figure 4. Output-Output Skew

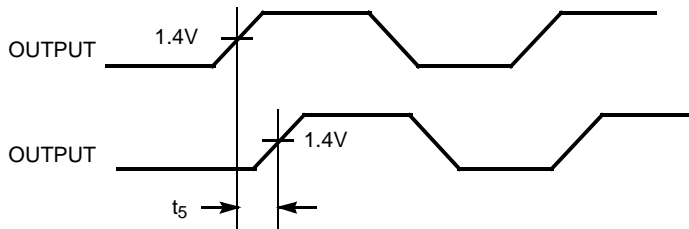


Figure 5. Input-Output Propagation Delay

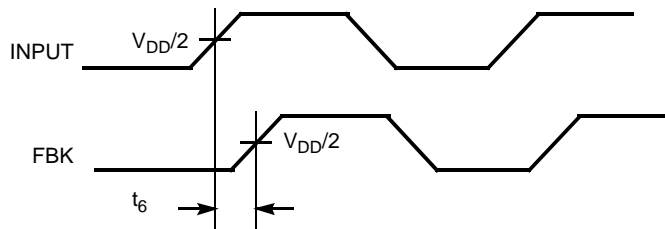
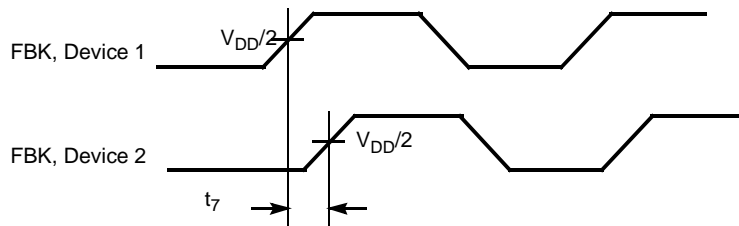
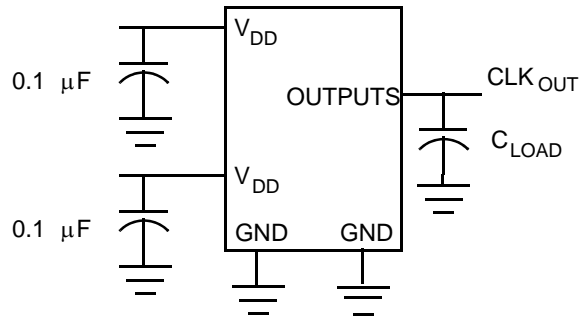


Figure 6. Device-Device Skew



Test Circuits

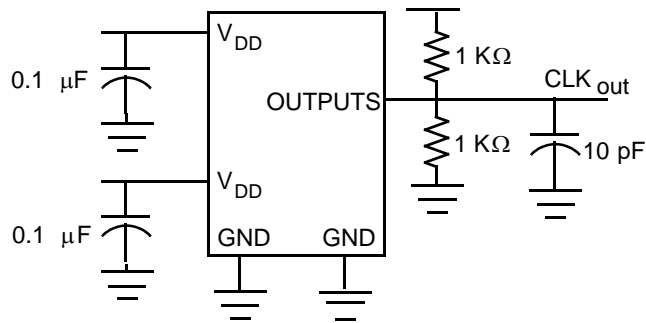
Figure 7. Test Circuit 1



Test Circuit for all parameters except t_8

Figure 8. Test Circuit 2

Test Circuit # 2



Test Circuit for t_8 , Output slew rate on -1H device

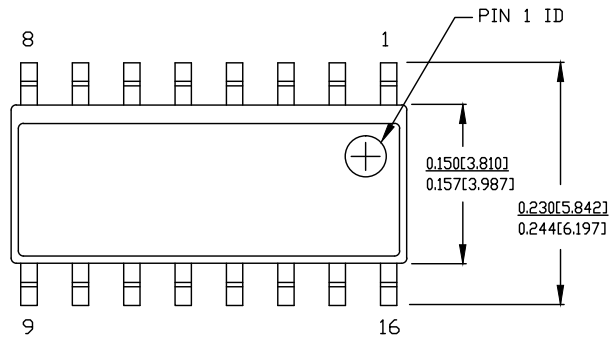
Ordering Information

| Ordering Code | Package Type | Operating Range |
|----------------|-----------------------------------|---------------------------|
| Pb-free | | |
| CY23S08SXC-1 | 16-pin 150-mil SOIC | Commercial (0° to 70°C) |
| CY23S08SXC-1T | 16-pin 150-mil SOIC-Tape and Reel | Commercial (0° to 70°C) |
| CY23S08SXI-1H | 16-pin 150-mil SOIC | Industrial (-40° to 85°C) |
| CY23S08SXI-1HT | 16-pin 150-mil SOIC-Tape and Reel | Industrial (-40° to 85°C) |
| CY23S08ZXC-1H | 16-pin 4.4mm TSSOP | Commercial (0° to 70°C) |
| CY23S08ZXC-1HT | 16-pin 4.4mm TSSOP | Commercial (0° to 70°C) |
| CY23S08SXC-2H | 16-pin 150-mil SOIC | Commercial (0° to 70°C) |
| CY23S08SXC-2HT | 16-pin 150-mil SOIC-Tape and Reel | Commercial (0° to 70°C) |
| CY23S08SXI-2 | 16-pin 150-mil SOIC | Industrial (-40° to 85°C) |
| CY23S08SXI-2T | 16-pin 150-mil SOIC-Tape and Reel | Industrial (-40° to 85°C) |
| CY23S08SXC-4 | 16-pin 150-mil SOIC | Commercial (0° to 70°C) |
| CY23S08SXC-4T | 16-pin 150-mil SOIC-Tape and Reel | Commercial (0° to 70°C) |

Package Drawings and Dimensions

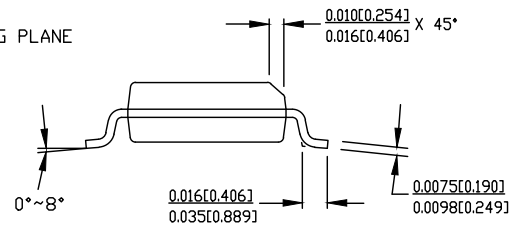
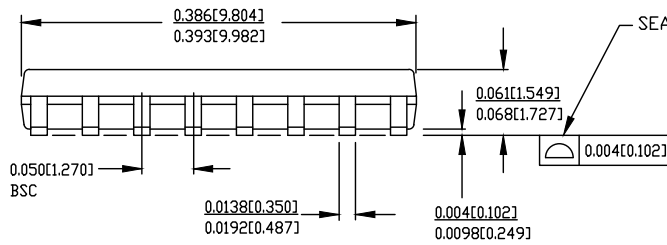
Figure 9. 16-Pin (150-Mil) SOIC S16

16 Lead (150 Mil) SOIC



DIMENSIONS IN INCHES[MM] MIN. MAX.
 REFERENCE JEDEC MS-012
 PACKAGE WEIGHT 0.15gms

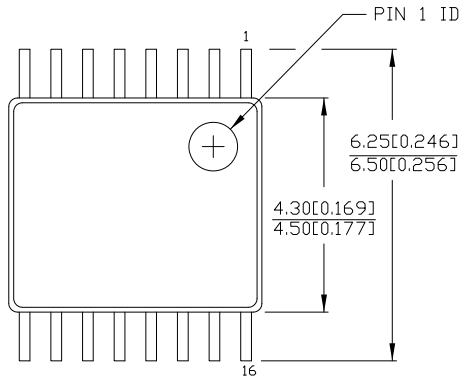
| PART # | |
|---------|----------------|
| S16.15 | STANDARD PKG. |
| SZ16.15 | LEAD FREE PKG. |



51-85068 °C

Figure 10. 16-Pin Thin Shrunken Small Outline Package (4.40 mm Body) Z16

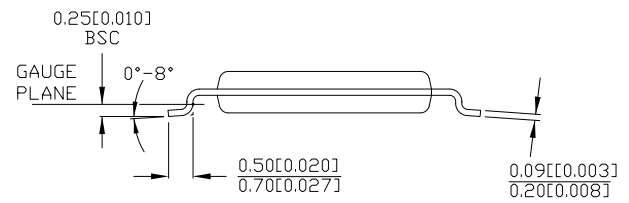
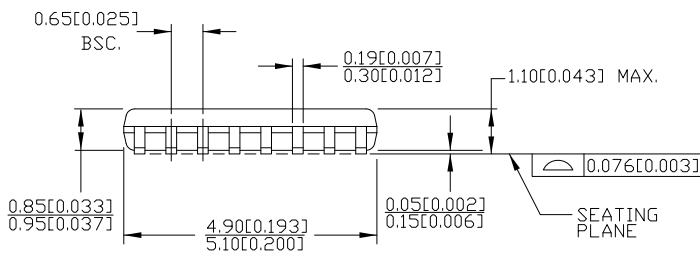
16 Lead TSSOP 4.40 MM BODY



DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153
PACKAGE WEIGHT 0.05gms

| PART # | |
|----------|----------------|
| Z16.173 | STANDARD PKG. |
| ZZ16.173 | LEAD FREE PKG. |



51-85091 *B

Document History Page

| Document Title: CY23S08 3.3V Zero Delay Buffer Document Number: 38-07265 | | | | |
|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 110530 | SZV | 12/02/01 | Change from Spec number: 38-01107 to 38-07265 |
| *A | 122863 | RBI | 12/20/02 | Added power up requirements to operating conditions information. |
| *B | 130951 | RGL | 11/26/03 | Corrected the Switching Characteristics parameters to reflect the W152 device and new characterization. |
| *C | 204201 | RGL | See ECN | Corrected the Block Diagram |
| *D | 231100 | RGL | See ECN | Fixed Typo in table 2. |
| *E | 378878 | RGL | See ECN | Added Industrial Temp and Pb Free Devices Added typical char data Removed "Preliminary" |
| *F | 391564 | RGL | See ECN | Changed output-to-output skew typical value from 90ps to 45ps Added cycle-to-cycle jitter (-2) typical value of 85ps |
| *G | 1442823 | WWZ/AESA | See ECN | Updated ordering info with status update. Added new Pb-free part numbers. |
| *H | 2600345 | WWZ/PYRS | 11/03/08 | Updated max frequency number from 133 MHz to 140 MHz on page 1 and page 4 load capacitance description |
| *I | 2658081 | KVM/PYRS | 02/16/09 | Corrected TSSOP package size (from 150 mil to 4.4 mm) in Ordering Information Table. Removed references to SOIC in the pinout drawing and pin description table on page 2. Added CY23S08ZXC-1HT to the Ordering Information Table. Updated Ordering Information Table to remove obsolete devices. Removed Status column. |
| *J | 2761988 | KVM | 09/10/09 | Added industrial temperature range to Operating Conditions table. Added numerical values to Operating Range column of Ordering Information table. Removed references to -3 device. |
| *K | 2904767 | CXQ | 04/05/10 | Removed parts CY23S08SXC-2,CY23S08SXC-2T,CY23S08SXI-4,CY23S08SXI-4T from Ordering Information. Updated Package Diagrams. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2001-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.