

Bora Embedded Linux Kit (BELK)



Info Box



Applies to Bora

Introduction

Bora Embedded Linux Kit (BELK for short) provides all the necessary components required to set up the developing environment for:

- configuring the system (PS and PL) at hardware level
- build the first-stage bootloader (FSBL)
- building the second stage bootloader (U-Boot)
- building and running Linux operating system on Bora-based systems
- building Linux applications that will run on the target

DAVE Embedded Systems provides all the customization required (in particular at bootloader and Linux kernel levels) to enable customers use the standard Zynq-7000 development tools for building all the firmware/software components that will run on the target system.

Logical structure of Bora Embedded Linux Kit (BELK)

To understand the structure of BELK, it is necessary to describe the basic organization of Xilinx Vivado Design Suite/Xilinx SDK and to recall briefly the recent history of development tools provided by Xilinx.

A little bit of history

At the time of this writing (October 2013) Xilinx is migrating from mature ISE 14.x Design Suite - that should be the last series of this suite - to the new Vivado environment. Both are composed by several programs and some of these are in common. From the general standpoint, the main difference between ISE and Vivado - even if ISE does support Zynq - is the the latter has been expressively conceived to support newer SOC architectures such as Zynq, besides traditional FPGAs. Thus, adopting Vivado as the default environment for BELK would seem the natural choice. However, the migration process mentioned above has just begun and the majority of application notes and reference designs released by Xilinx still refers to ISE suite. Plus Vivado is still a little bit "green" and several bug fixes and improvements are introduced by every new release.

Since Bora was presented in 2013 and because this product addresses long longevity markets such as industrial and biomedical, **DAVE Embedded Systems** chose to build BELK upon Vivado that undoubtedly represents today the future of Xilinx development environments.

Structure of BELK reference designs

The typical linux-based Zynq design is composed by the following parts:

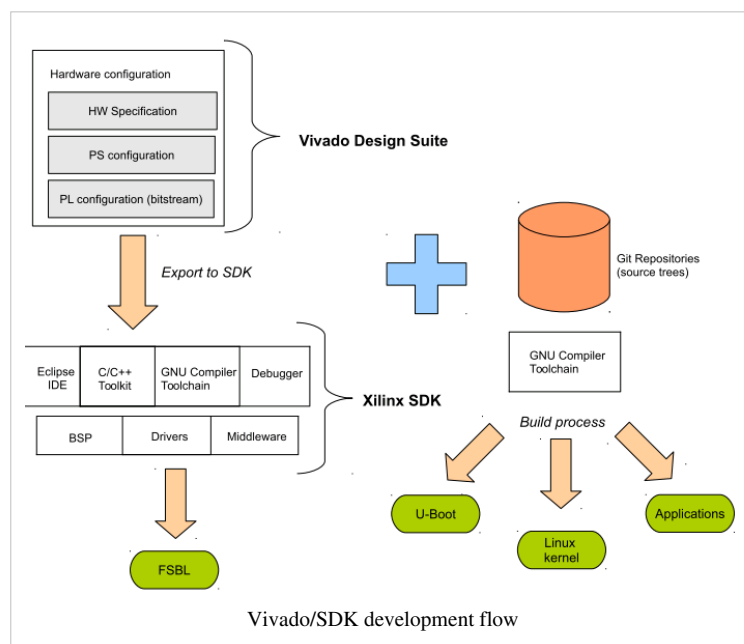
- FSBL
- U-Boot
- device tree file
- Linux kernel
- Root file system
- Executable image of core #1 (in case of AMP systems)
- FPGA bitstream.

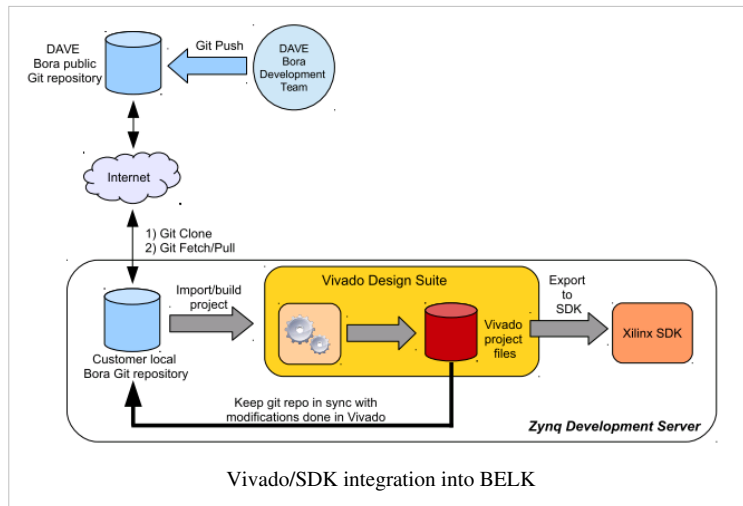
Generally speaking, this parts - in the binary/sinthesized form - are combined together in one monolithic file that is stored in a non-volatile memory such as SPI NOR flash. Generating this file is quite easy as described by Vivado documentation. However in real world products, this may be too rigid because developers may want to handle these parts separately and independently.

Basic structure of Vivado Design Suite and integration into BELK

Vivado/SDK (1) can be viewed as a collection of programs required to deal with all of the development aspects related to Xilinx components (software running on ARM cores, FPGA fabric verification and programming, power estimation etc.). These include strictly FPGA-related tools such as Floorplanner and pure-software development tools such as SDK. The ambitious objective is to provide a complete, user friendly, integrated environment that allows software developers to deal with FPGA development even if they are not familiar with this technology, by hiding a lot of its complexities (2). As usual this ease of use comes at the expence of control and flexibility. This could not be acceptable in many cases where engineers need to control and customize many aspects of the project to implement what is required by system specifications. For this reason BELK has been built around Vivado but some deviations from the default development approach suggested by Xilinx have been introduced, in order to push the modularization and the maintainability of the projects to the maximum extent.

The following pictures are retrieved from BELK Quick Start Guide and shows respectively the Vivado/SDK default development flow and how this has been integrated in the BELK infrastructure.





(1) The Software Development Kit (SDK) is the Xilinx Integrated Design Environment for creating embedded applications on Zynq™-7000 All Programmable SoCs. SDK is the first application IDE to deliver true homogenous and heterogenous multi-processor design and debug, it is optionally included with the Vivado Design Suite or ISE Design Suite, or available as a separate free download for application developers.

(2) Nevertheless FPGA developers will find all the traditional tools that allow complete control of FPGA fabric.

BELK software components

DAVE Embedded Systems adds to the latest Linux BSP from Xilinx the customization required to support the Bora platform, in particular at bootloader and linux kernel levels.

The following table reports the XELK releases information.

	BELK version		
Release number	1.0.0	1.1.0	2.0.0
Status	Released	Released	Scheduled
Release date	July 2013	November 2013	1Q2014
Release notes	Ver 1.0.0	Ver 1.1.0	Ver 2.0.0
SOM PCB version	CS020313A	CS020313A	CS020313B
Supported carrier boards	BoraEVB-Lite	BoraEVB-Lite	BoraEVB
U-Boot version	2013.04-belk-1.0.0	2013.04-belk-1.1.0	t.b.a.
Linux version	3.9.0-bora-1.0.0	3.9.0-bora-1.1.0	t.b.a.
Drivers	-	-	Gigabit Eth #0 UART NOR NAND SD/MMC USB Host/Device RTC CAN I2C

Release notes

BELK 2.0.0

Updates:

1. Added support for the BoraEVB carrier board
2. Updated supported drivers list (please refer to BELK_software_components)

Known Limitations

The following table reports the known limitations of this BELK release:

Issue	Description
External DDR3 bank	The DDR3 SDRAM bank on the BoraEVB is not supported in this BELK version.
ETH1 interface	The additional Gigabit Ethernet interface (ETH1) is not supported in this BELK version.

BELK 1.1.0





Updates:

1. Switched to Vivado 2013.3
2. Added application note "AMP on Bora"

BELK 1.0.0

First official release

Kit Contents

Component	Description	Notes
	Bora SOM CPU: Xilinx Zynx 7000	Please refer to Bora Hardware Manual
	Bora-EVB-Lite Carrier board	Please refer to BoraEVB-Lite page
	AC/DC Single Output Wall Mount adapter Output: +12V – 2.0 A	Please refer to Belk Quick Start Guide
	MicroSDHC card with SD adapter and USB adapter	Please refer to Belk Quick Start Guide

Related Documents

- Bora Hardware Manual
- BoraEVB-Lite
- BoraEVB
- Belk Quick Start Guide (available for BELK kit owners)
- Application Note: AN-BELK-001: Asymmetric Multiprocessing (AMP) on Bora – Linux + FreeRTOS ^[1]
- Bora FAQs

References

- [1] <http://www.dave.eu/sites/default/files/files/an-belk-001-amp-linux-freertos.pdf>
-

Article Sources and Contributors

Bora Embedded Linux Kit (BELK) *Source:* <http://wiki.dave.eu/index.php?oldid=3014> *Contributors:* DevWikiAdmin

Image Sources, Licenses and Contributors

File:WorkInProgress.gif *Source:* <http://wiki.dave.eu/index.php?title=File:WorkInProgress.gif> *License:* unknown *Contributors:* DevWikiAdmin

File:Bora5-small.jpg *Source:* <http://wiki.dave.eu/index.php?title=File:Bora5-small.jpg> *License:* unknown *Contributors:* DevWikiAdmin

File:Belk-vivado-sdk-development-flow.png *Source:* <http://wiki.dave.eu/index.php?title=File:Belk-vivado-sdk-development-flow.png> *License:* unknown *Contributors:* DevWikiAdmin

File:Belk-vivado-sdk-integration.png *Source:* <http://wiki.dave.eu/index.php?title=File:Belk-vivado-sdk-integration.png> *License:* unknown *Contributors:* DevWikiAdmin

File:Boraevb-lite-01.png *Source:* <http://wiki.dave.eu/index.php?title=File:Boraevb-lite-01.png> *License:* unknown *Contributors:* DevWikiAdmin

File:Alimentatore.jpg *Source:* <http://wiki.dave.eu/index.php?title=File:Alimentatore.jpg> *License:* unknown *Contributors:* DevWikiAdmin

File:ProdSDC-MBLY-thumb.png *Source:* <http://wiki.dave.eu/index.php?title=File:ProdSDC-MBLY-thumb.png> *License:* unknown *Contributors:* DevWikiAdmin

License

General

All content and materials on this wiki are provided "as is" without warranty of any kind. The entire risk as to the results and the performance of the information is assumed by the user, and in no event shall **DAVE Embedded Systems** be liable for any consequential, incidental or direct damages suffered in the course of using the information in this wiki. **DAVE Embedded Systems** and its respective suppliers make no representations about the suitability of these materials for any purpose and disclaim all warranties and conditions with regard to these materials, including but not limited to, all implied warranties and conditions of merchantability, fitness for a particular purpose, title and non-infringement of any third party intellectual property right.

Contents

Content on this wiki may contain or be subject to specific guidelines or limitations on use and use of the content on this wiki is subject to the Terms of Use of the site; third parties using this content agree to abide by any limitations or guidelines and to comply with the Terms of Use of this site. **DAVE Embedded Systems** reserves the right to make corrections, deletions, modifications, enhancements, improvements and other changes to the content and materials, its products, programs and services at any time or to move or discontinue any content, products, programs, or services without notice. Information published by **DAVE Embedded Systems** regarding third-party products or services does not constitute a license from **DAVE Embedded Systems** to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from **DAVE Embedded Systems** under the patents or other intellectual property of **DAVE Embedded Systems**. Reproduction of **DAVE Embedded Systems** information in **DAVE Embedded Systems** data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. **DAVE Embedded Systems** is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

DAVE Embedded Systems holds no responsibility for the content of external sites that are linked to from this wiki.

Trademarks

Any of the trademarks, service marks, collective marks, design rights or similar rights that are mentioned, used or cited in this wiki are the property of their respective owners.

Availability

Every effort is made to keep the website up and running smoothly. However, **DAVE Embedded Systems** takes no responsibility for, and will not be liable for, the website being temporarily unavailable due to technical issues beyond our control.