Bora Embedded Linux Kit (BELK)

Info Box

Applies to Bora

Introduction

Bora Embedded Linux Kit (BELK for short) provides all the necessary components required to set up the developing environment for:

- configuring the system (PS and PL) at hardware level
- build the first-stage bootloader (FSBL)
- building the second stage bootloader (U-Boot)
- building and running Linux operating system on Bora-based systems
- building Linux applications that will run on the target

DAVE Embedded Systems provides all the customization required (in particular at bootloader and Linux kernel levels) to enable customers use the standard Zynq-7000 development tools for building all the firmware/software components that will run on the target system.

Logical structure of Bora Embedded Linux Kit (BELK)

To understand the structure of BELK, it is necessary to describe the basic organization of Xilinx Vivado Design Suite/Xilinx SDK and to recall briefly the recent history of development tools provided by Xilinx.

A little bit of history

At the time of this writing (October 2013) Xilinx is migrating from mature ISE 14.x Design Suite - that should be the last series of this suite - to the new Vivado environment. Both are composed by several programs and some of these are in common. From the general standpoint, the main difference between ISE and Vivado - even if ISE does support Zynq - is the the latter has been expressively conceived to support newer SOC architectures such as Zynq, besides traditional FPGAs. Thus, adopting Vivado as the default environment for BELK would seem the natural choice. However, the migration process mentioned above has just begun and the majority of application notes and reference designs released by Xilinx still refers to ISE suite. Plus Vivado is still a little bit "green" and several bug fixes and improvements are introduced by every new release.

Since Bora was presented in 2013 and because this product addresses long longevity markets such as industrial and biomedical, **DAVE Embedded Systems** chose to build BELK upon Vivado that undoubtedly represents today the future of Xilinx development environments.

Structure of BELK reference designs

The typical linux-based Zynq design is composed by the following parts:

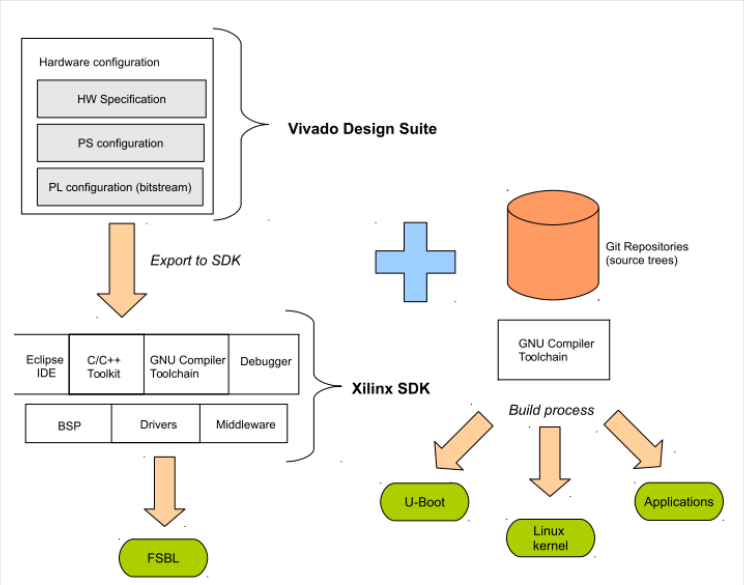
- FSBL
- U-Boot
- device tree file
- Linux kernel
- Root file system
- Executable image of core #1 (in case of AMP systems)
- FPGA bitstream.

Generally speaking, this parts - in the binary/sinthesized form - are combined together in one monolithic file that is stored in a non-volatile memory such as SPI NOR flash. Generating this file is quite easy as described by Vivado documentation. However in real world products, this may be too rigid because developers may want to handle these parts separately and independently.

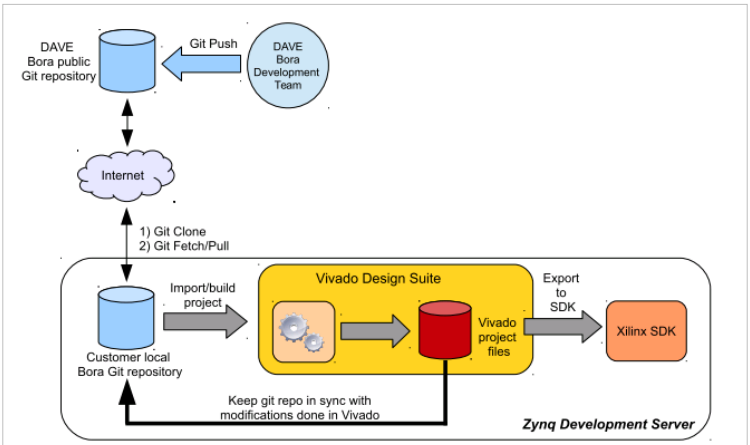
Basic structure of Vivado Design Suite and integration into BELK

Vivado/SDK (1) can be viewed as a collection of programs required to deal with all of the development aspects related to Xilinx components (software running on ARM cores, FPGA fabric verification and programming, power estimation etc.). These include strictly FPGA-related tools such as Floorplanner and pure-software development tools such as SDK. The ambitious objective is to provide a complete, user friendly, integrated environment that allows software developers to deal with FPGA development even if they are not familiar with this technology, by hiding a lot of its complexities (2). As usual this ease of use comes at the expence of control and flexibility. This could not be acceptable in many cases where engineers need to control and customize many aspects of the project to implement what is required by system specifications. For this reason BELK has been built around Vivado but some deviations from the default development approach suggested by Xilinx have been introduced, in order to push the modularization and the maintainability of the projects to the maximum extent.

The following pictures are retrieved from BELK Quick Start Guide and shows respectively the Vivado/SDK default development flow and how this has been integrated in the BELK infrastructure.



Vivado/SDK development flow



Vivado/SDK integration into BELK

(1) The Software Development Kit (SDK) is the Xilinx Integrated Design Environment for creating embedded applications on Zynq™-7000 All Programmable SoCs. SDK is the first application IDE to deliver true homogenous and heterogenous multi-processor design and debug, it is optionally included with the Vivado Design Suite or ISE Design Suite, or available as a separate free download for application developers.

(2) Nevertheless FPGA developers will find all the traditional tools that allow complete control of FPGA fabric.

BELK software components

DAVE Embedded Systems adds to the latest Linux BSP from Xilinx the customization required to support the Bora platform, in particular at bootloader and linux kernel levels.

The following table reports the XELK releases information.

	BELK version		
Release number	1.0.0	1.1.0	2.0.0
Status	Released	Released	Scheduled
Release date	July 2013	November 2013	1Q2014
Release notes	Ver 1.0.0	Ver 1.1.0	Ver 2.0.0
SOM PCB version	CS020313A	CS020313A	CS020313B
Supported carrier boards	BoraEVB-Lite	BoraEVB-Lite	BoraEVB
U-Boot version	2013.04-belk-1.0.0	2013.04-belk-1.1.0	t.b.a.
Linux version	3.9.0-bora-1.0.0	3.9.0-bora-1.1.0	t.b.a
Drivers	-	-	Gigabit Eth #0 UART NOR NAND SD/MMC USB Host/Device RTC CAN I2C

Release notes

BELK 2.0.0

Updates:

1. Added support for the BoraEVB carrier board
2. Updated supported drivers list (please refer to BELK_software_components)

Known Limitations

The following table reports the known limitations of this BELK release:

Issue	Description
External DDR3 bank	The DDR3 SDRAM bank on the BoraEVB is not supported in this BELK version.
ETH1 interface	The additional Gigabit Ethernet interface (ETH1) is not supported in this BELK version.

BELK 1.1.0

Updates:

1. Switched to Vivado 2013.3
2. Added application note "AMP on Bora"

BELK 1.0.0

First official release

Kit Contents

Component	Description	Notes
	Bora SOM CPU: Xilinx Zynx 7000	Please refer to Bora Hardware Manual
	Bora-EVB-Lite Carrier board	Please refer to BoraEVB-Lite page
	AC/DC Single Output Wall Mount adapter Output: +12V – 2.0 A	Please refer to Belk Quick Start Guide
	MicroSDHC card with SD adapter and USB adapter	Please refer to Belk Quick Start Guide

Related Documents

- Bora Hardware Manual
- BoraEVB-Lite
- BoraEVB
- Belk Quick Start Guide (available for BELK kit owners)
- Application Note: AN-BELK-001: Asymmetric Multiprocessing (AMP) on Bora – Linux + FreeRTOS [1]
- Bora FAQs

References

[1] http://www.dave.eu/sites/default/files/files/an-belk-001-amp-linux-freertos.pdf

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