AD9286-500EBZ User Guide
UG-191

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Evaluating the AD9286 Analog-to-Digital Converter

FEATURES

Full featured evaluation board for the AD9286
SPI interface for setup and control
Support LVDS output mode option
External or on-board oscillator options
Balun/transformer or amplifier input drive options
Switching power supply
VisualAnalog™ and SPIController software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
Two switching power supplies (6.0 V, 2.5 A),
CUI EPS060250UH-PHP-SZ, provided
PC running 32-bit Windows® XP, Window Vista, or Windows 7
USB 2.0 port, recommended (USB 1.1-compatible)
AD9286 evaluation board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPIController

DOCUMENTS NEEDED

AD9286 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*

GENERAL DESCRIPTION

This user guide describes the AD9286 evaluation board, which provides all of the support circuitry required to operate the AD9286 in its various modes and configurations. The application software used to interface with the device is also described.

The AD9286 data sheet provides additional information and should be consulted when using the evaluation board. All documents and software tools are available at the FIFO page. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP

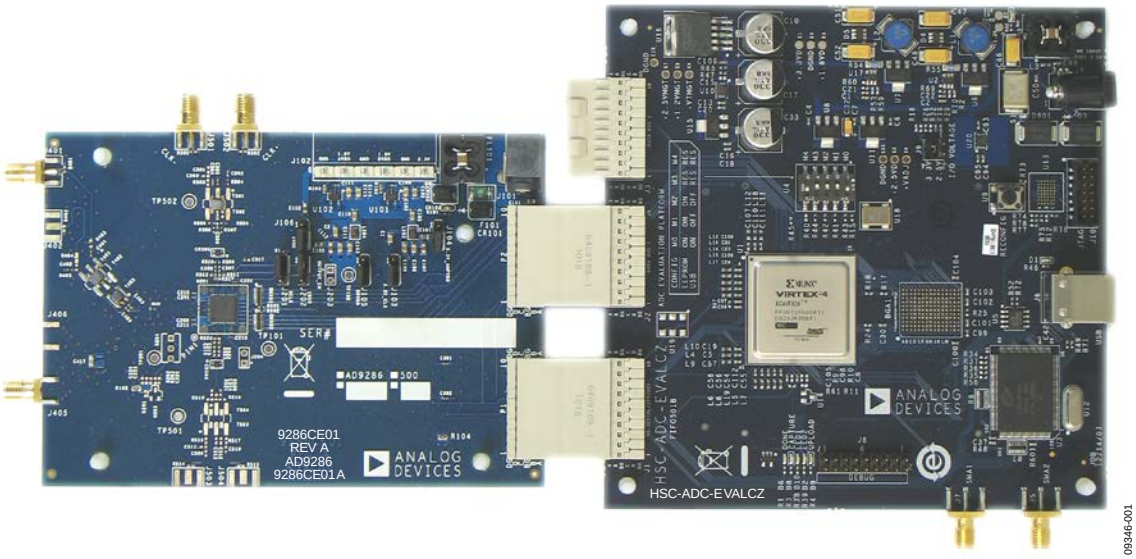

Figure 1. AD9286 Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

TABLE OF CONTENTS

REVISION HISTORY

6/14—Rev. 0 to Rev. A

Changes to Figure 13 9
Changes to Figure 14 10
Changes to Figure 15 11
Changes to Figure 16 12
Changes to Figure 17 13
Changes to Figure 18 14
Changes to Figure 19 15

REVISION HISTORY

5/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9286 evaluation board provides all of the support circuitry required to operate the AD9286 in its various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD9286 . It is critical that the signal source used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 13 to Figure 25 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using the AD9286 .

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to the 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at J101. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA, or HP8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the specifications in the AD9286 data sheet). When connecting the analog input source, a multipole, narrow-band, band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture.

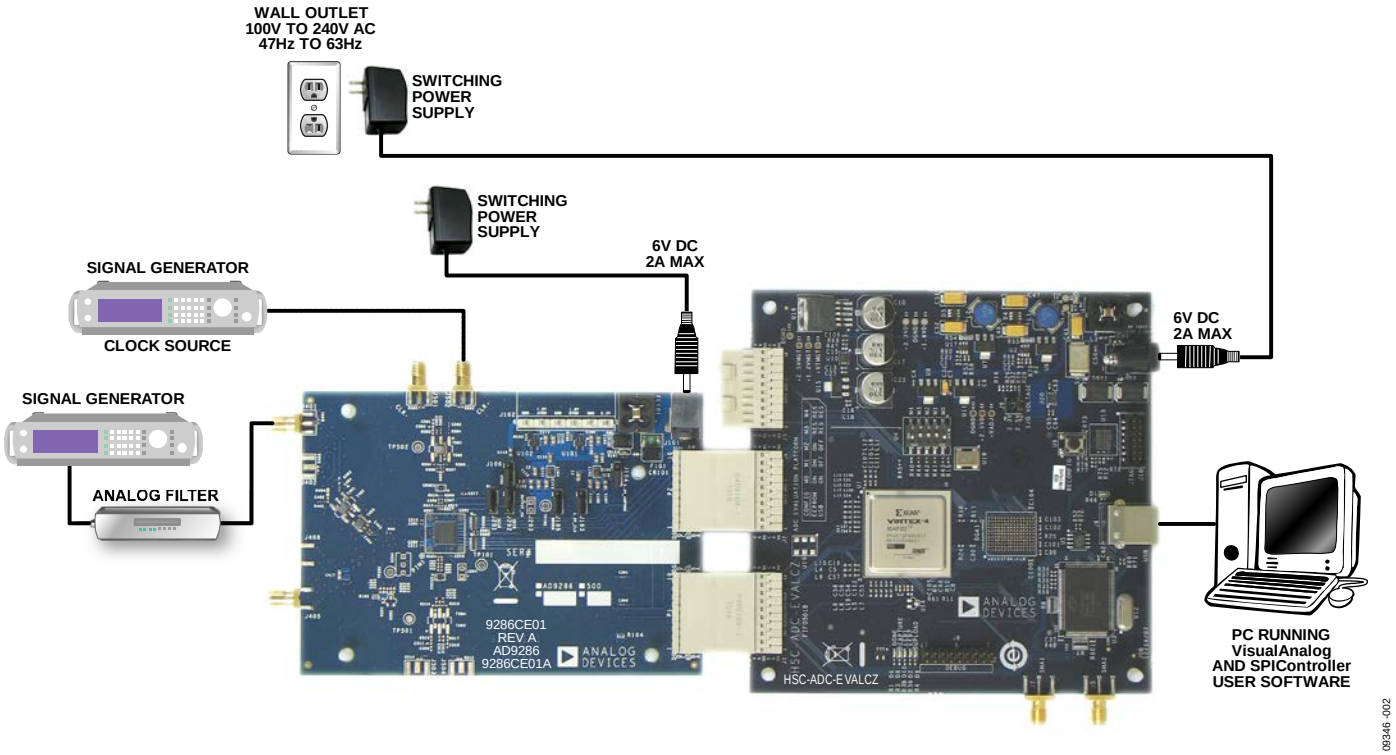

Figure 2. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD9286 evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and J101.

Analog Input

The analog input on the evaluation board default configuration uses a single transformer input with a 50 Ω impedance. The default analog input configuration supports analog input frequencies of up to ~200 MHz. This input network is optimized to support a wide frequency band.

An alternate analog input configuration uses a single ADA4937-1 ultralow distortion amplifier, which drives both VIN1 and VIN2. Special attention has been paid to provide a symmetrical layout between the two differential inputs to realize best performance. To configure the analog input circuitry, see Table 1.

The nominal input drive level is 10.5 dBm to achieve 1.2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

VREF

The AD9286 operates with a fixed 1.0 V reference. This sets the analog input span to 1.2 V p-p.

RBIAS

RBIAS has a default setting of 10 kΩ (R206) to ground and is used to set the ADC core bias current. Note that using a resistor value other than a 10 kΩ, 1% resistor for RBIAS may degrade the performance of the device.

Clock Circuitry

The default clock input circuit on the AD9286 evaluation board uses a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T501) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR501 before entering the ADC clock inputs. The AD9286 board has on-chip circuitry to distribute a single clock to each interleaved ADC channel.

Alternatively, the AD9286 evaluation board supports driving each internal ADC core with its own separate half speed clock. This is useful in applications where the user wants to externally control the clock timing per channel. To enable separate clocking, write a value 0 to SPI Address 0x09 and place a jumper across J204 to tie AUXCLKEN to DRVDD.

Non-SPI Mode

For users who want to operate the DUT without using SPI, remove the shorting jumpers on J302. This disconnects the CSB, SCLK, and SDIO/PWDN pins from the SPI control bus, allowing the DUT to operate in non-SPI mode. In this mode, the SDIO/PWDN pin takes on an alternate function to enable power-down functionality.

To enable the power-down feature, add a shorting jumper across J202 at Pin 2 and Pin 3 to connect the SDIO/PDWN pin to DRVDD.

Table 1. Analog Input Mode Configurations[1]

Analog Input Mode	R406	R407	R408	R409	R410	R411	R412	R413
Passive Path	DNI	0 Ω	0 Ω	DNI	33 Ω	33 Ω	33 Ω	33 Ω
Active Path	0 Ω	DNI	DNI	0 Ω	DNI	DNI	0 Ω	0 Ω

[1] DNI = do not install.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9286 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board using the following steps:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ) to the AD9286 board.
3. Connect one 6 V, 2.5 A switching power supply (such as the supplied CUI EPS060250UH-PHP-SZ) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable.
5. On the ADC evaluation board, confirm that six jumpers are installed as described as follows:
   - J103, Pin 2 and Pin 3 (clock with regulator)
   - J104, Pin 2 and Pin 3 (amp with regulator)
   - J105, Pin 2 and Pin 3 (DRVDD with regulator)
   - J106, Pin 2 and Pin 3 (AVDD with regulator)
   - J201, Pin 1 and Pin 2 (SCLK SPI)
   - J202, Pin 1 and Pin 2 (SDIO SPI)
6. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the desired A and/or B channel(s). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 3).
   Note that once power is applied to the AD9286 evaluation board, the device is powered down. To wake up the device, the SDIO/PWDN pin must be pulled low. This occurs automatically by VisualAnalog after you complete Step 1.

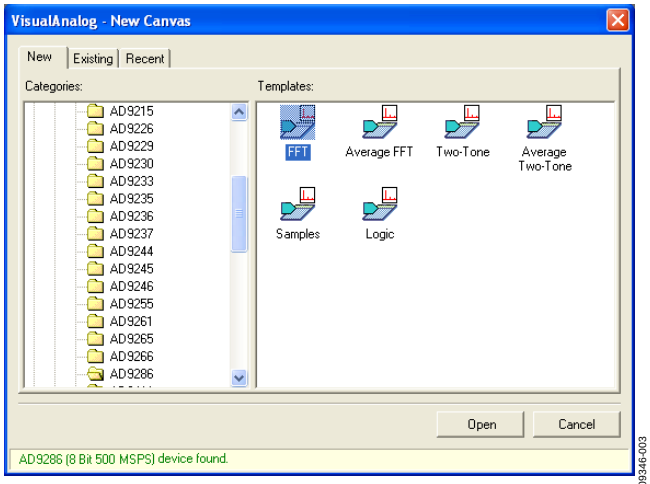

Figure 3. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 4). Click **Yes** to close the window.

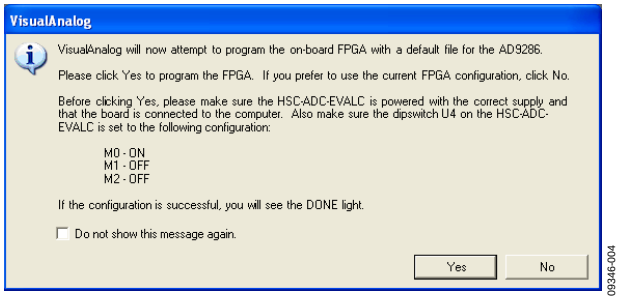

Figure 4. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window, to see what is shown in Figure 6. Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click the collapse display button (see the collapsed display in Figure 5).

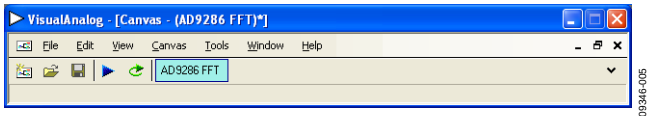

Figure 5. VisualAnalog Window Toolbar, Collapsed Display

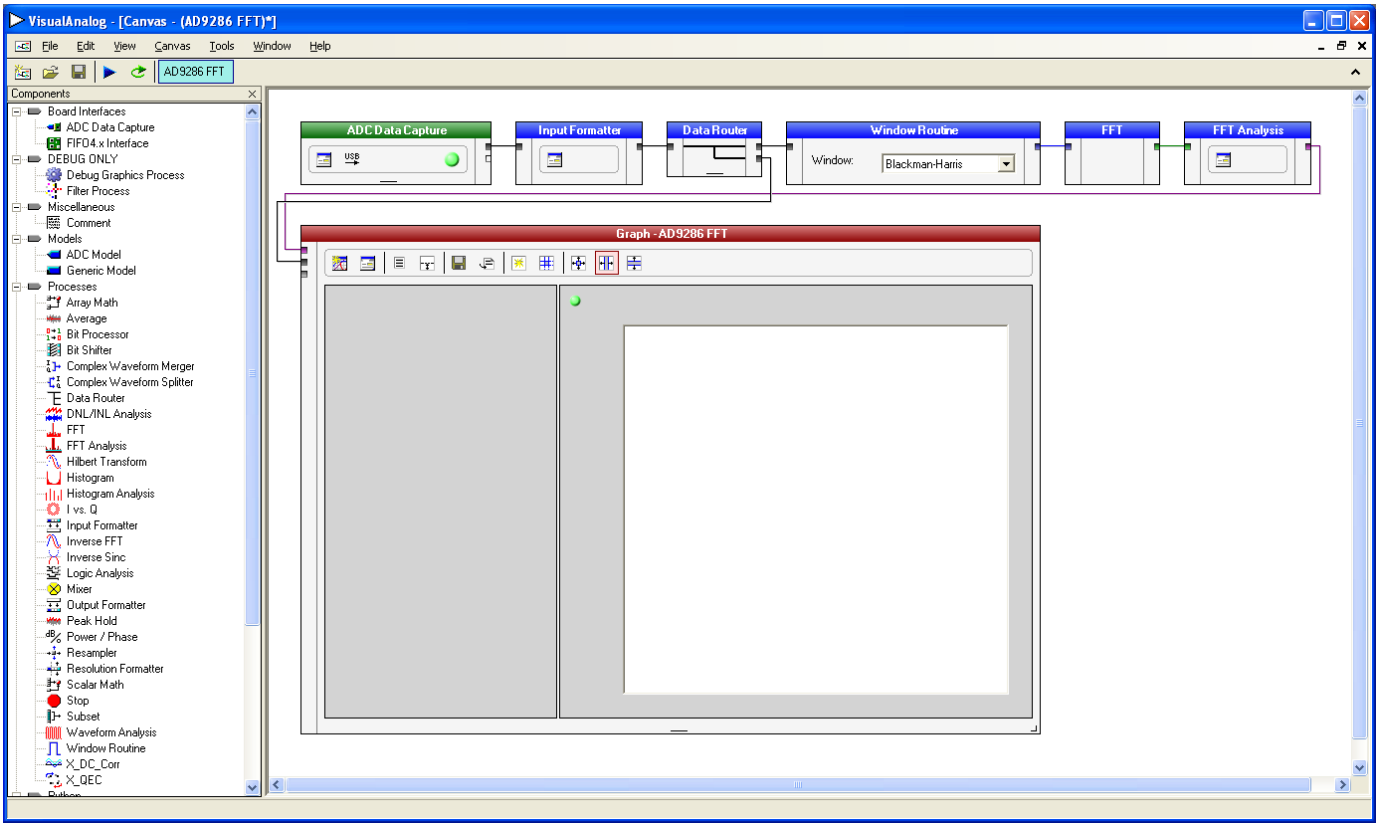

Figure 6. VisualAnalog Main Window

Setting Up the SPIController Software

After the ADC data capture board setup is complete, set up the SPIController software using the following procedure:

1. Open the SPIController software by selecting **Start** > **SPIController** or by double-clicking the **SPIController** software desktop icon.
   If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 7).

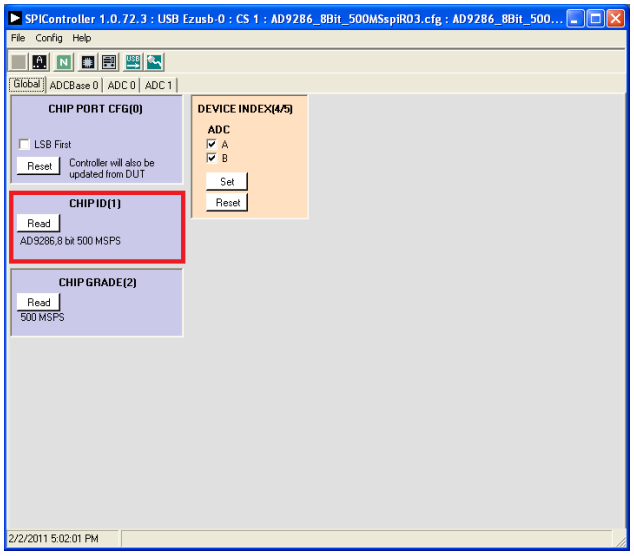

Figure 7. SPIController, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 8).

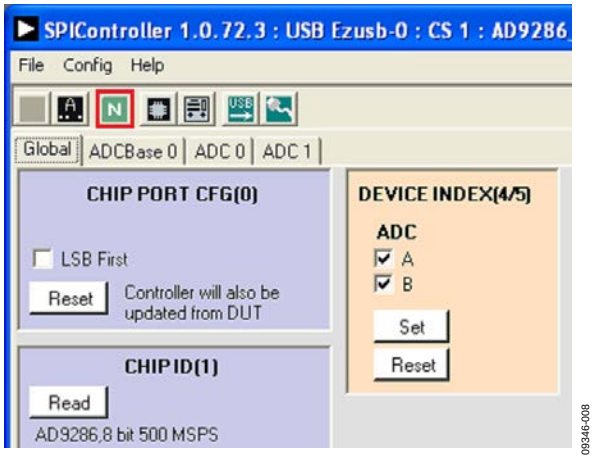

Figure 8. SPIController, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, you can access all global register settings (see Figure 9). See the AD9286 data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

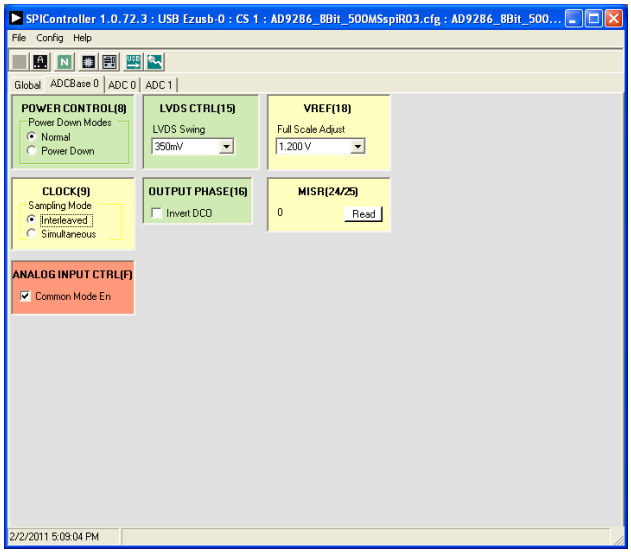

Figure 9. SPIController, ADC Base0

4. Note that other settings can be changed on the **ADCBase 0** page (see Figure 9) and the **ADC 0** and **ADC 1** pages (see Figure 10) to set up the part in the desired mode. The **ADCBase 0** page settings affect the entire part, whereas the settings on the **ADC 0** and **ADC 1** pages affect the selected channel only. See the AD9286 data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

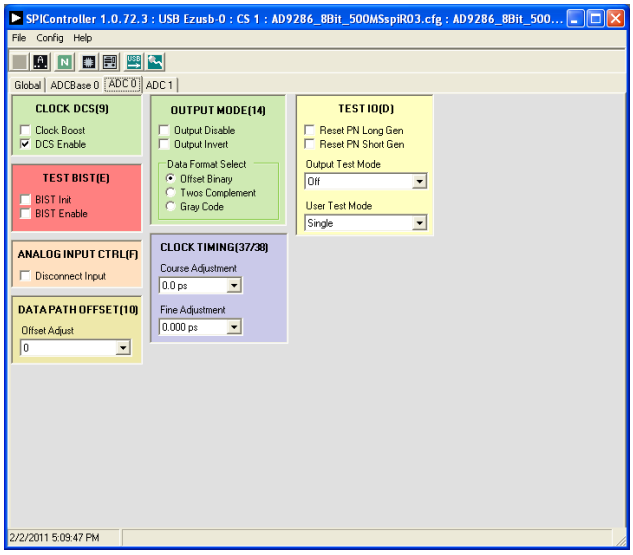

Figure 10. SPIController, ADC 0 Page

5. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 11).

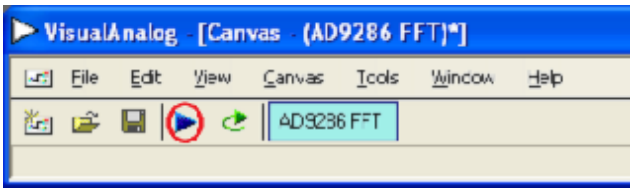

Figure 11. Run Button in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level (examine the **Fund Power** reading in the left panel of the **VisualAnalog Graph** - AD9286 **FFT** window). See Figure 12.

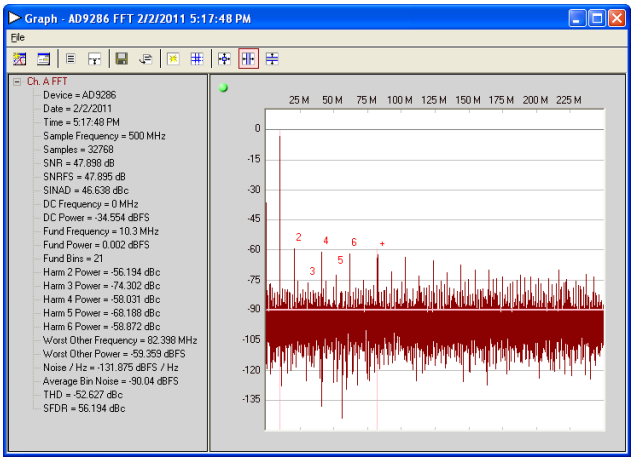

Figure 12. Graph Window of VisualAnalog

2. Repeat this procedure for Channel B.
3. Click the disk icon within the **Graph** window to save the performance plot data as a .csv formatted file.

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In VisualAnalog, click the **Settings** button in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** is clicked, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the HSC-ADC-EVALCZ board is in the correct position for USB configuration.
- Make sure the correct FPGA program was installed by selecting the **Settings** button in the **ADC Data Capture** block in VisualAnalog. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If VisualAnalog indicates that the **FIFO Capture timed out**, do the following:

- Make sure all power and USB connections are secure.
- Probe the DCOA signal at RN601 on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

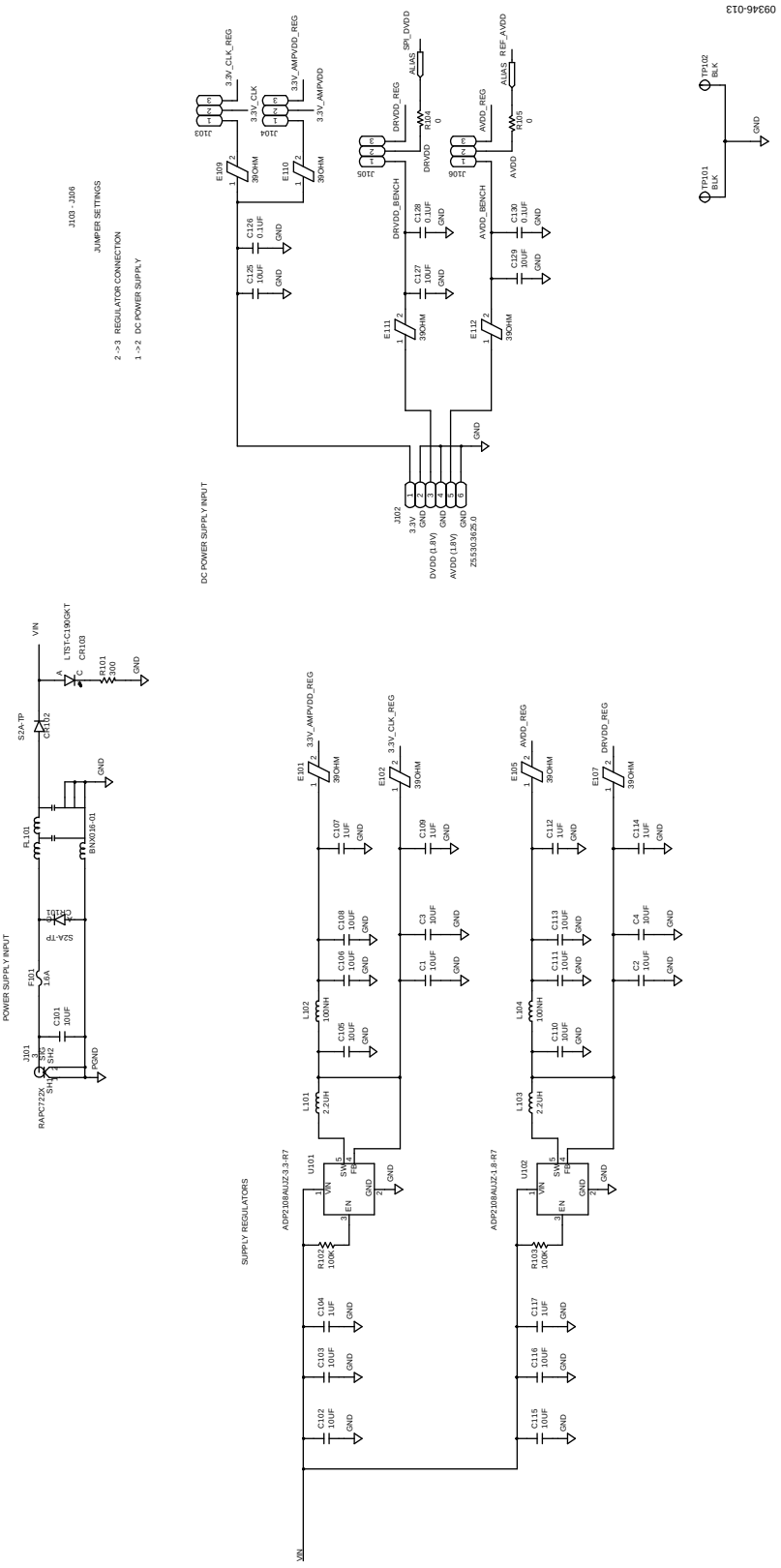

Figure 13. Board Power Input and Supply Circuits

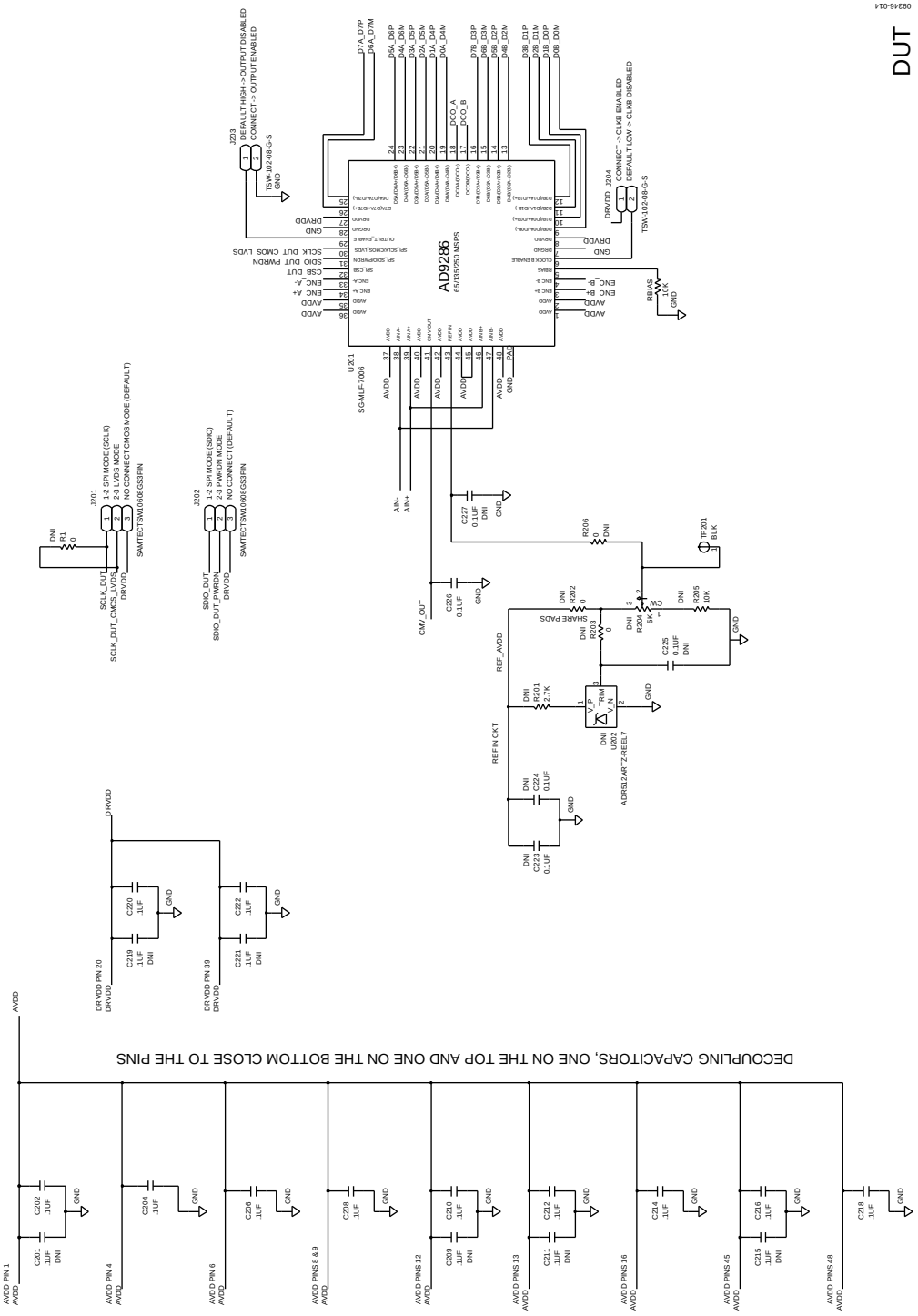

Figure 14. DUT and Related Circuit

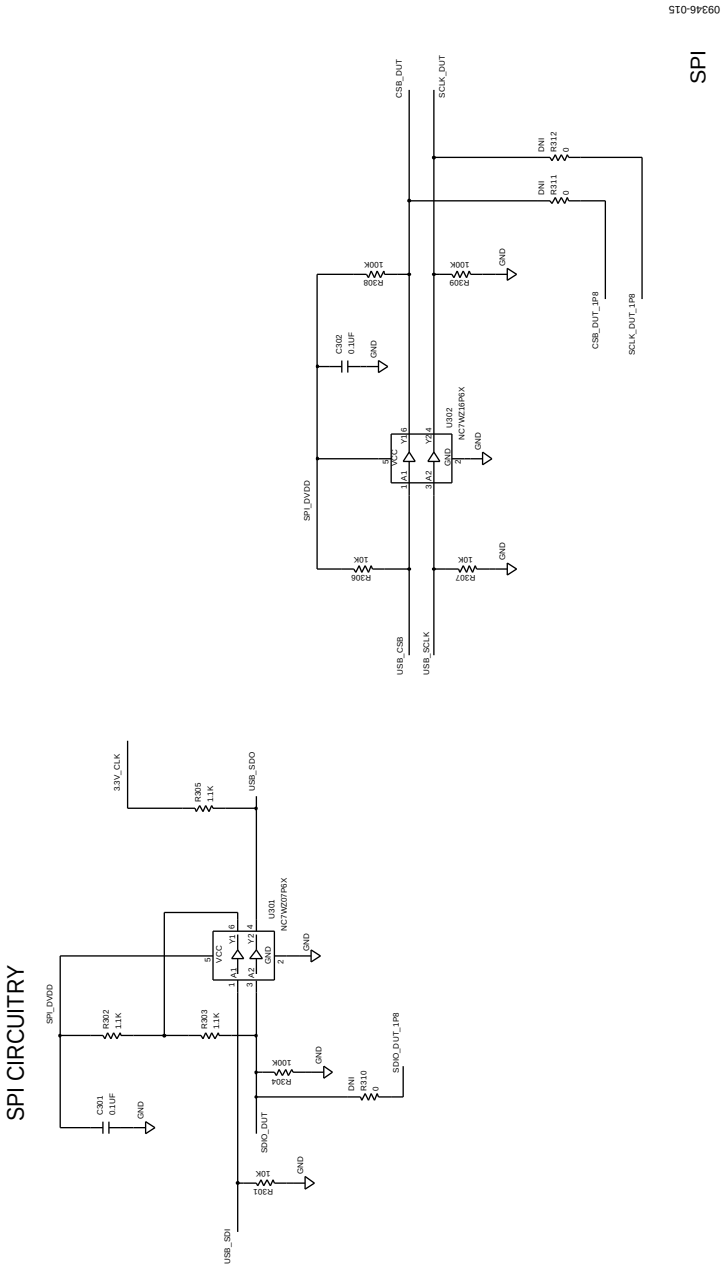

Figure 15. SPI Interface Circuit

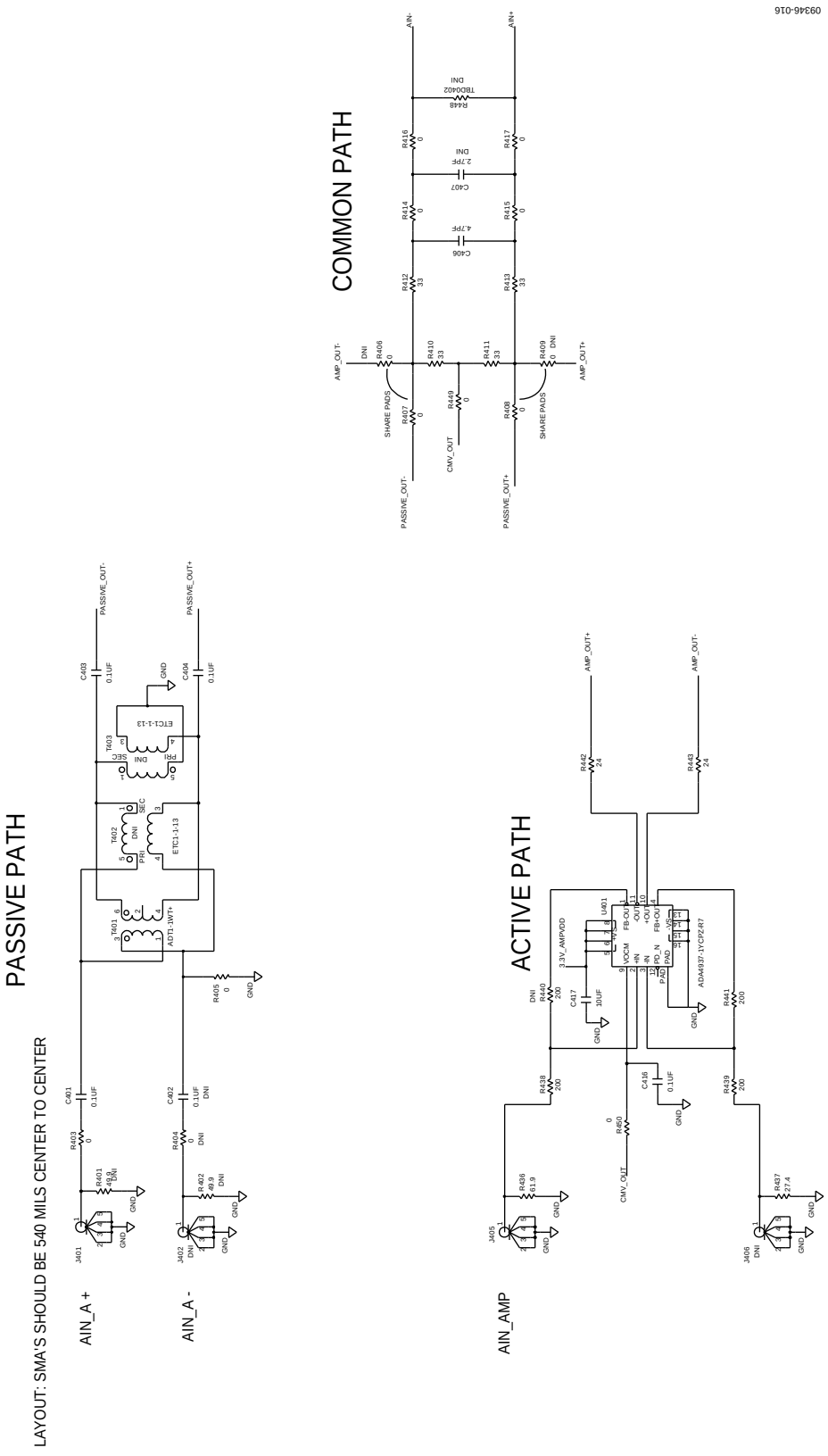

Figure 16. Analog Input Circuits

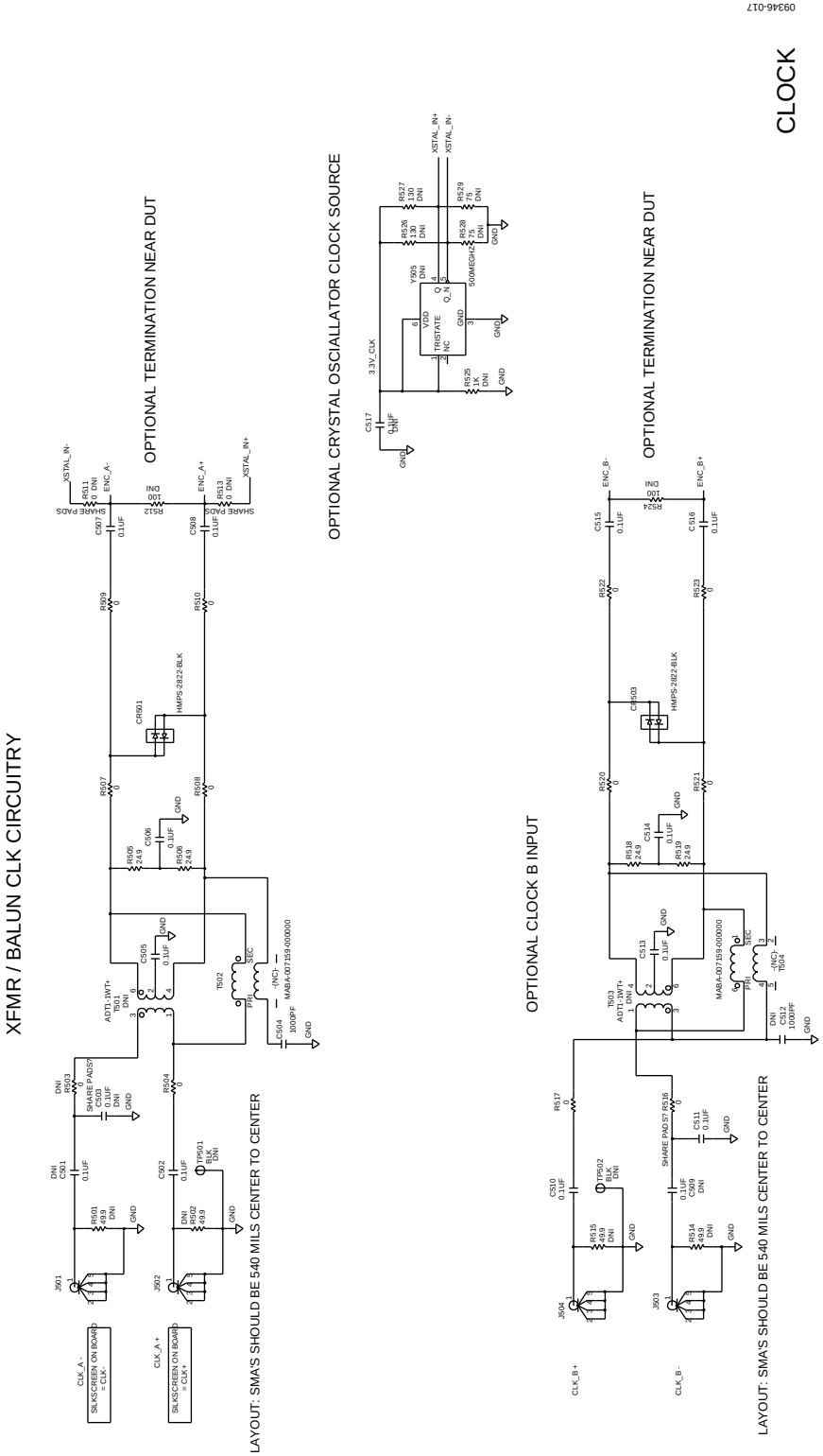

Figure 17. Default Clock Path Input Circuits

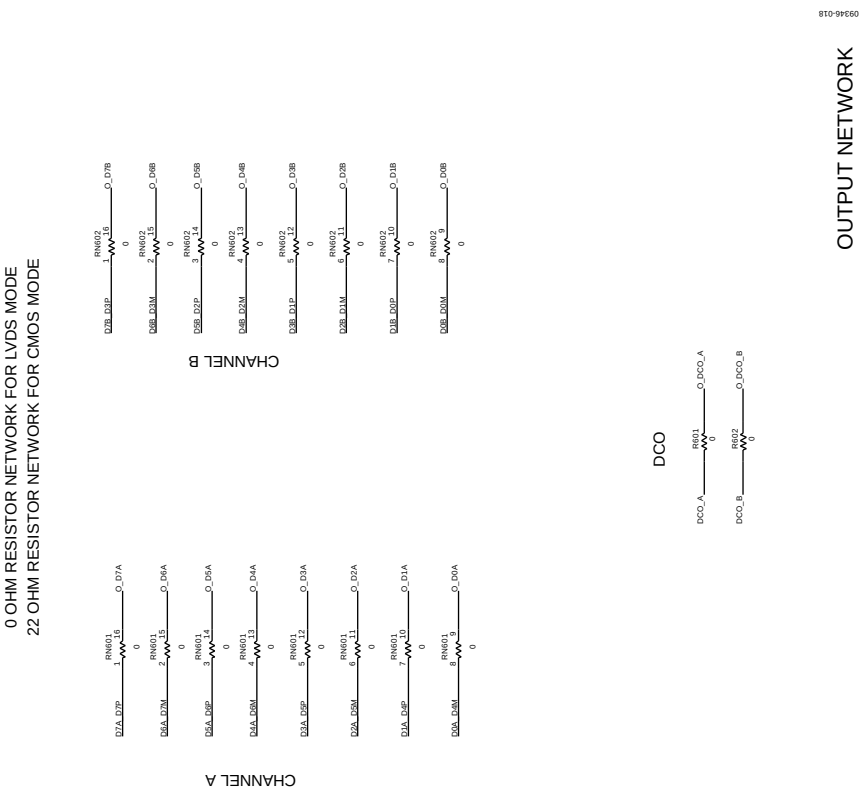

Figure 18. Output Buffer Circuits

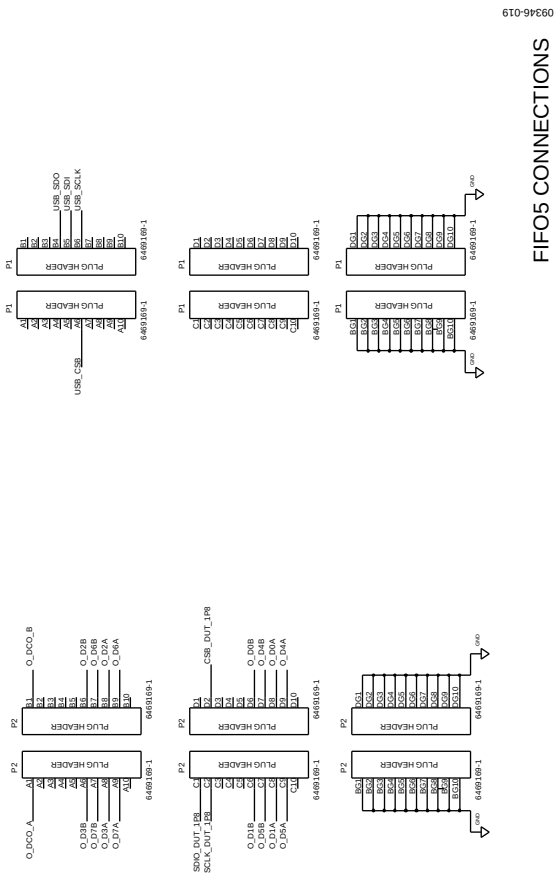

Figure 19. FIFO Board Connector

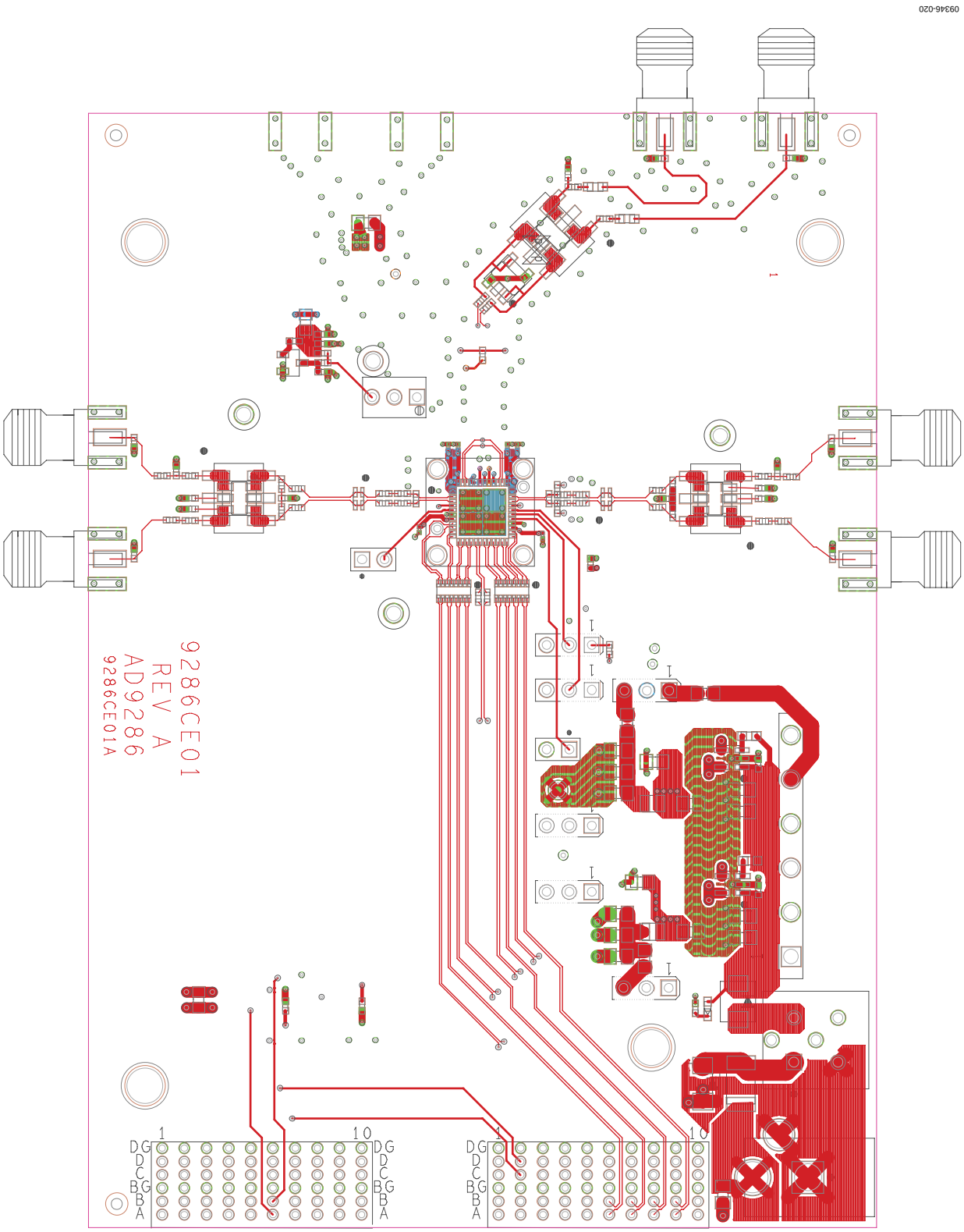

Figure 20. Top Side

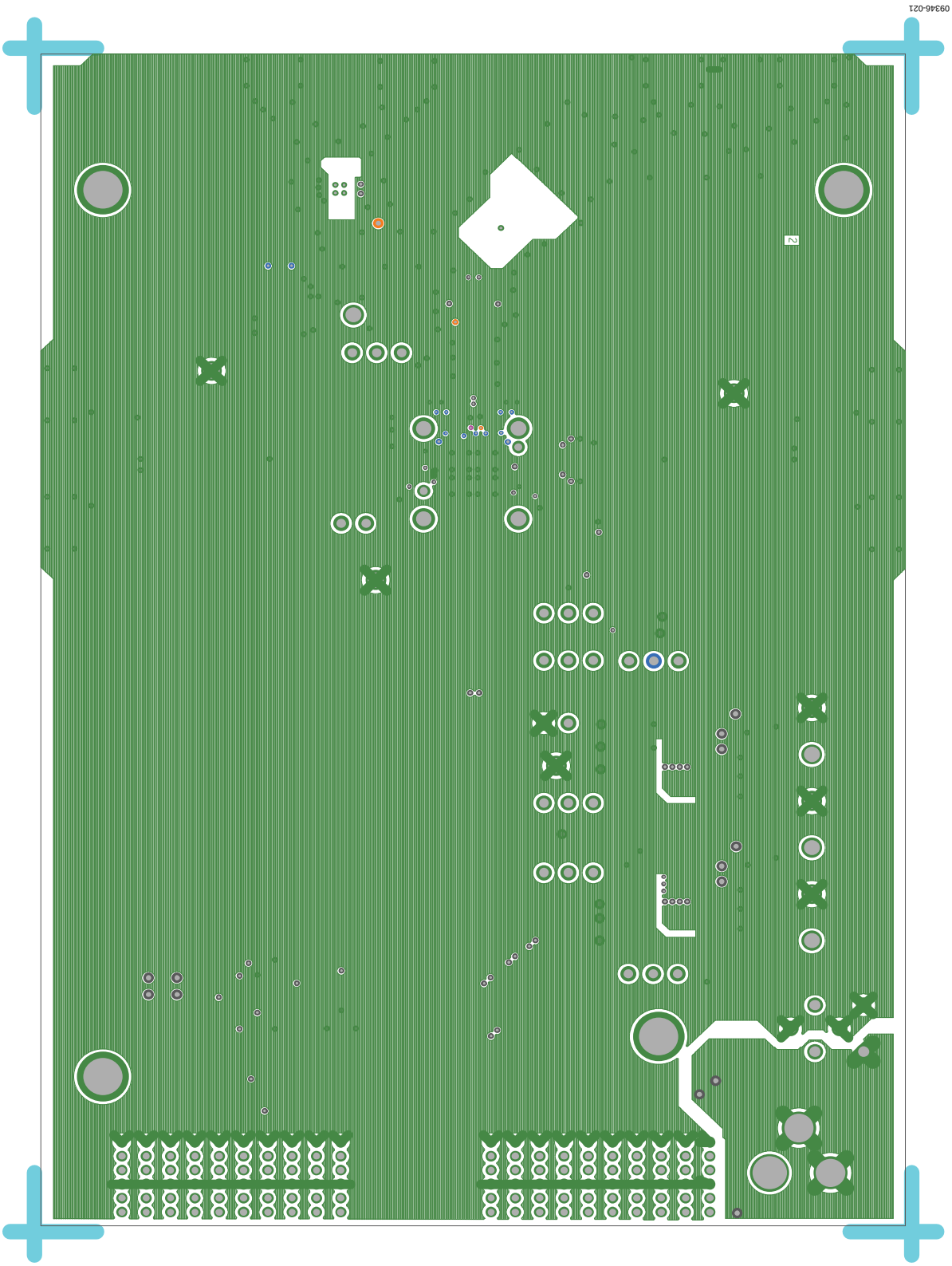

Figure 21. Ground Plane (Layer 2)

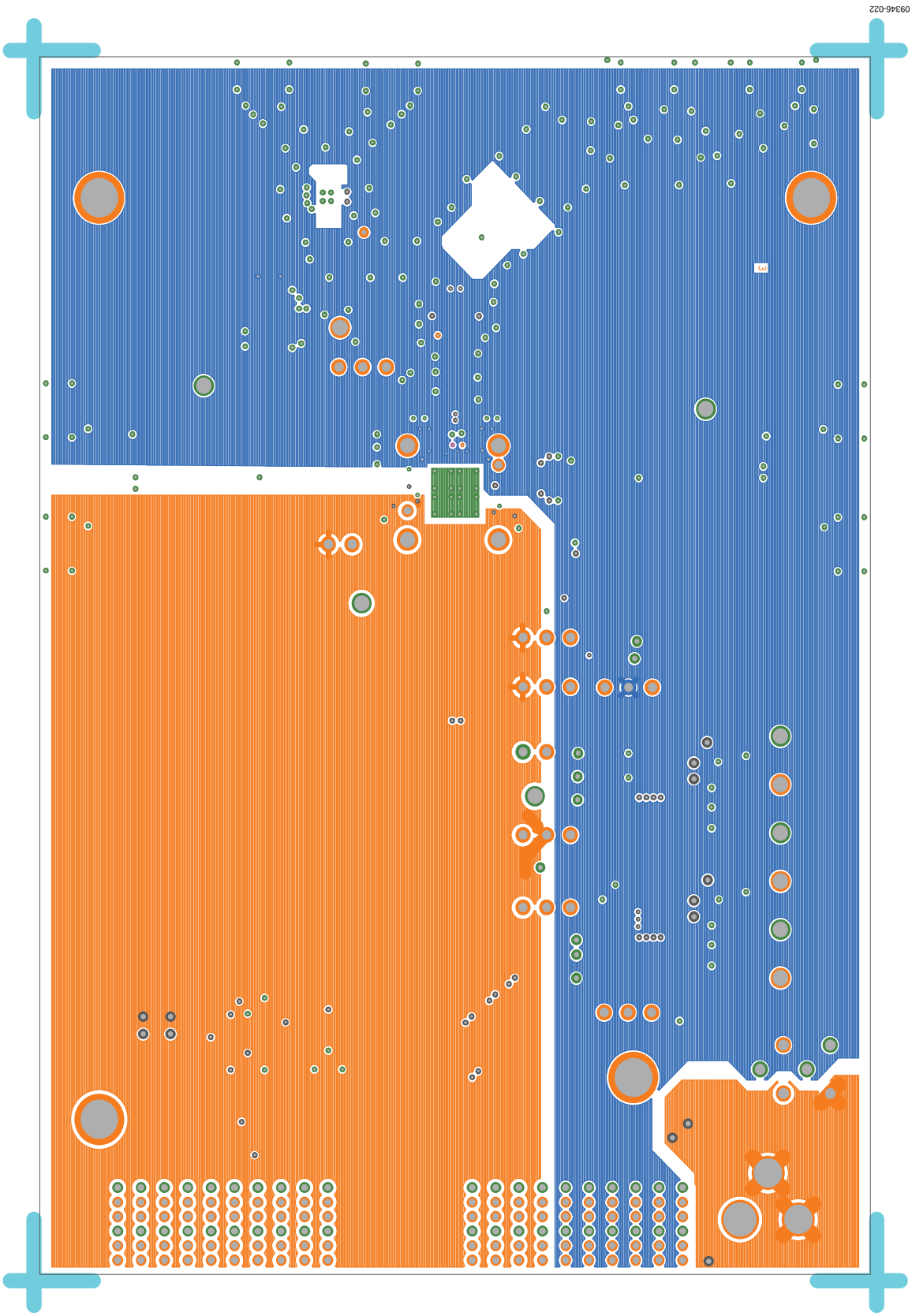

Figure 22. Power Plane (Layer 3)

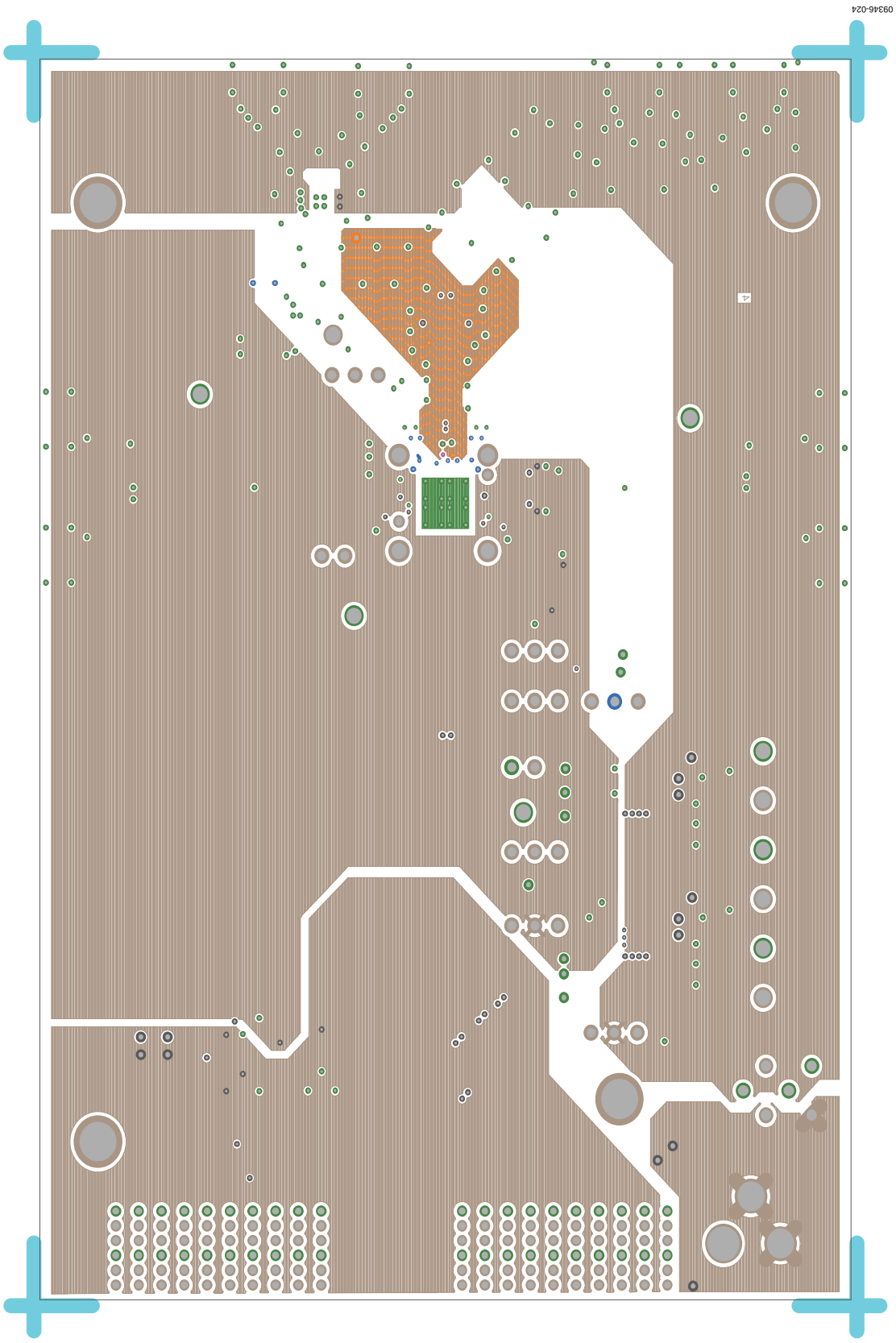

Figure 23. Power Plane (Layer 4)

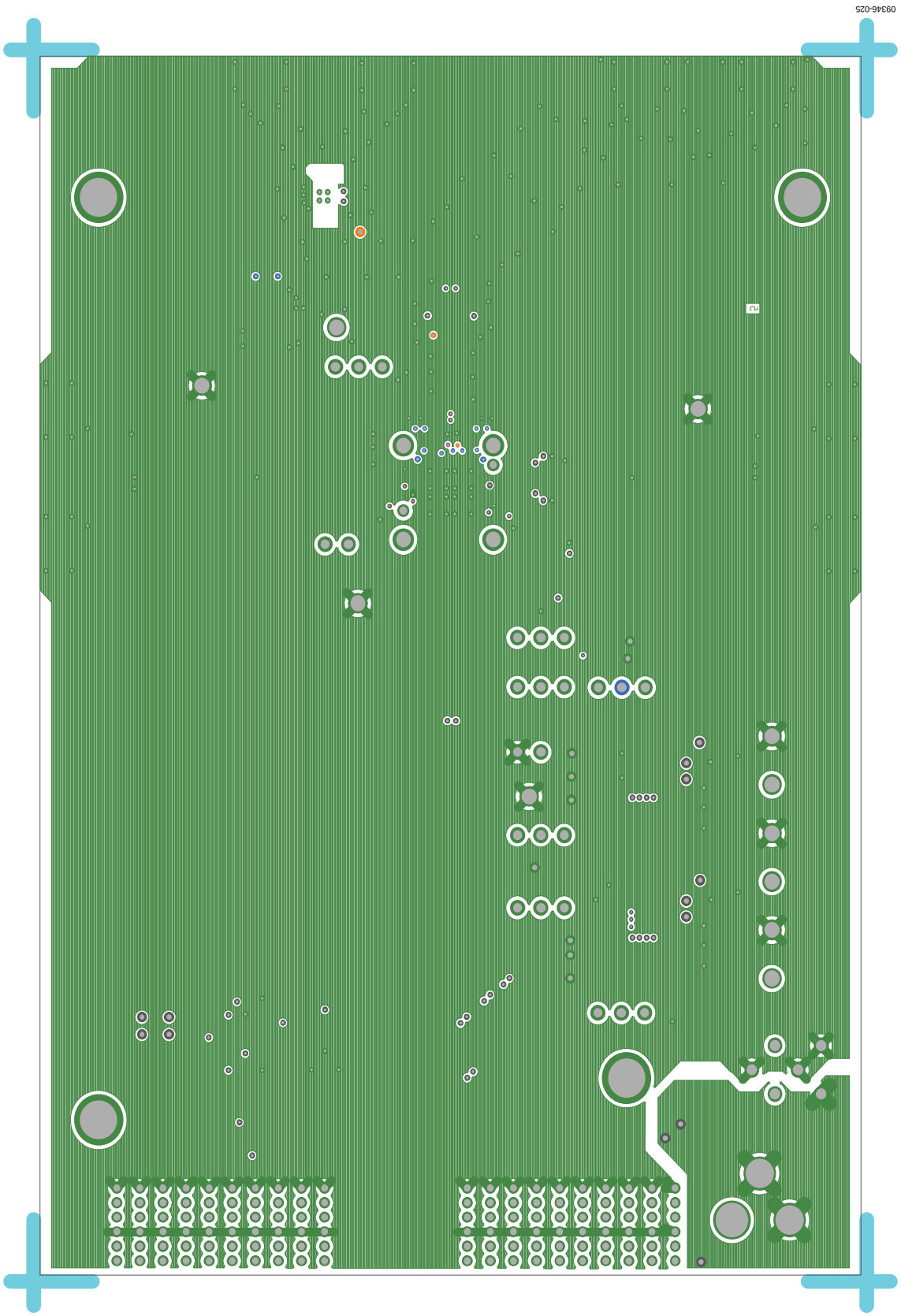

Figure 24. Ground Plane (Layer 5)

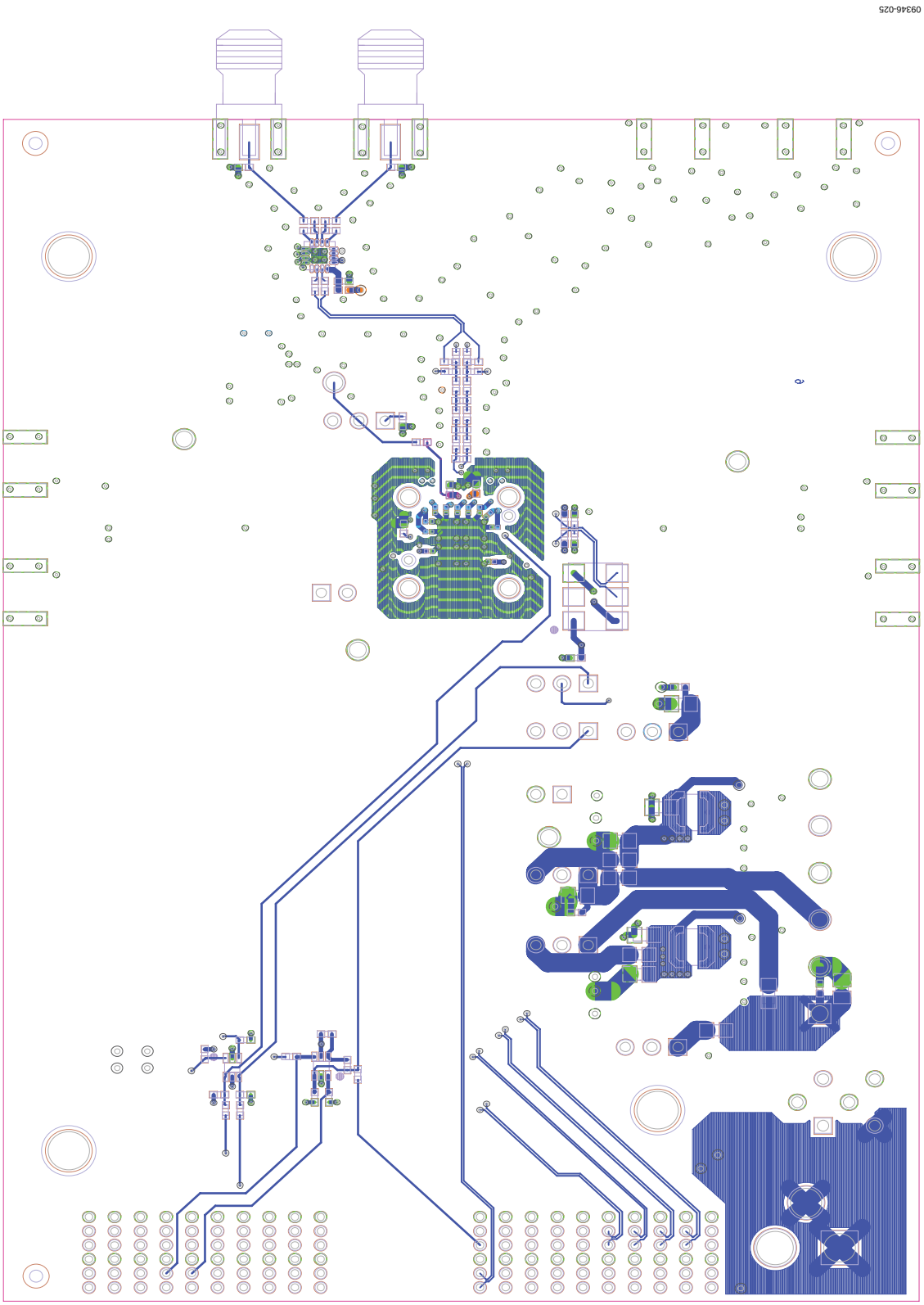

Figure 25. Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference Designator	Description	Value	Manufacturer/Part No.
1	Not applicable	PCB		9286CE01A
19	C1, C2, C3, C4, C101, C102, C103, C105, C106, C108, C110, C111, C113, C115, C116, C125, C127, C129, C417	Ceramic, 0805, monolithic capacitor	10 µF	Murata/GRM21BR61C106KE15L
2	C104, C117	Ceramic, 0402 monolithic capacitor	1 µF	Murata/GRM155R60J105KE19D
4	C107, C109, C112, C114	Ceramic, 0805, X7R capacitor	1 µF	Murata/GRM21BR71H105KA12L
21	C126, C128, C130, C226, C301, C302, C401, C403, C404, C416, C502, C505, C506, C507, C508, C510, C511, C513, C514, C515, C516	Ceramic, +80/−20%, 16 V, Y5V, 0402, capacitor	0.1 µF	Murata/GRM155F51C104ZA01D
11	C202, C204, C206, C208, C210, C212, C214, C216, C218, C220, C222	Ceramic, 6.3 V, Y5V, 0201, capacitor	0.1 µF	Murata/GRM033R60J104KE19D
1	C406	High Q microwave chip NP0 0402 capacitor	4.7 pF	Murata/GRM1555C1H4R7CZ01D
2	C504, C512	Ceramic, 25 V, 5%, C0G, 0402 capacitor	1000 pF	Murata/GRM1555C1E102JA01D
2	CR101, CR102	Recovery rectifier diode, D0214AA3	S2A-TP	Micro Commercial Components Corp/S2A-TP
1	CR103	Green surface-mount 0603 LED	LNJ308G8TRA (green)	Panasonic/LNJ308G8TRA
2	CR501, CR503	RF Schottky diode, MINIPAK1412-2	HSMS-2822-BLK	Avago Technologies/HSMS-2822-BLK
7	E101, E102, E105, E107, E109, E110, E111, E112	Inductor 0805 ferrite bead	100 MHz	Panasonic/EXC-ML20A390U
1	F101	Fuse F1812 polyswitch PTC device	1.6 A	Tyco Electronics/MINISMDC160F-2
1	FL101	Filter noise suppression LC combined type, FLBNX01	BNX016-01	Murata/BNX016-01
1	J101	PCB powerjack mini 0.08 in R/A T/H connector	RAPC722X	Switchcraft/RAPC722X
1	J102	PCB header 6 position connector	Z5.530.3625.0	Wieland/Z5.530.3625.0
6	J103, J104, J105, J106, J201, J202	PCB berg header ST male 3 position connector	SAMTECTSW10608G S3PIN	Samtec/TSW-103-08-G-S
1	J204	PCB header 2 position connector	TSW-102-08-G-S	Samtec/TSW-102-08-G-S
4	J401, J405, J502, J504	PCB SMA ST edge-mount connector	SMA-J-P-X-ST-EM1	Samtec/SMA-J-P-X-ST-EM1
2	L101, L103	Shielded power inductor, LSMSQ154H47	2.2 µH	Coilcraft/LPS4012-222MLC
2	L102, L104	SMD L9075 inductor	100 nH	Bourns/CW201212-R10J
2	P1, P2	CB 60-pin RA connector, CNTYCO1469169-1	6469169-1	Tyco/6469169-1
1	R101	Film SMD 0402 resistor	300 Ω	Panasonic/ERJ-2GEJ301X
2	R102, R103	Precision thick film chip 0603 resistor	100 kΩ	Panasonic/ERJ-3EKF1003V
2	R104, R105	Jumper SMD 0805 (SHRT) resistor	0 Ω	Panasonic/ERJ-6GEYJ0.0
4	R301, R306, R307, RBIAS	Precision thick film chip 0402 resistor	10 kΩ	Panasonic/ERJ-2RKF1002X
3	R302, R303, R305	Film SMD 0402 resistor	1.1 kΩ	Panasonic/ERJ-2GEJ112X
3	R304, R308, R309	Precision thick film chip 0402 resistor	100 kΩ	Panasonic/ERJ-2RKF1003X
1	R403	Film SMD 0603 resistor	0 Ω	Panasonic/ERJ-3GEY0R00V

Qty	Reference Designator	Description	Value	Manufacturer/Part No.
22	R405, R407, R408, R414, R415, R416, R417, R449, R450, R504, R507, R508, R509, R510, R516, R517, R520, R521, R522, R523, R601, R602	Film SMD 0402 resistor	0 Ω	Panasonic/ERJ-2GE0R00X
4	R410, R411, R412, R413	Film SMD 0402 resistor	33 Ω	Panasonic/ERJ-2GEJ330X
1	R436	Precision thick film chip 0402 resistor	61.9 Ω	Panasonic/ERJ-2RKF61R9X
1	R437	Precision thick film chip 0402 resistor	27.4 Ω	Panasonic/ERJ-2RKF27R4X
4	R438, R439, R440, R441	Precision thick film chip 0402 resistor	200 Ω	Panasonic/ERJ-2RKF2000X
2	R442, R443	Film SMD 0402 resistor	24 Ω	Panasonic/ERJ-2GEJ240X
4	R505, R506, R518, R519	Precision thick film chip 0402 resistor	24.9 Ω	Panasonic/ERJ-2RKF24R9X
2	RN601, RN602	Network 16-pin/8res surface-mount resistor	0 Ω	Panasonic/EXB-2HVR000V
1	T401	XFMR RF, MINICD542	ADT1-1WT+	Minicircuits/ADT1-1WT+
2	T502, T504	XFMR RF 1:1 (6-pin special) ETC1-6P	MABA-007159-000000	Macom/MABA-007159-000000
1	U101	Compact, 600 mA, 3 MHz, TSOT-5 step-down dc-to-dc converter	ADP2108AUJZ-3.3-R7	Analog Devices/ ADP2108AUJZ-3.3-R7
1	U102	Compact, 600 mA, 3 MHz, TSOT-5 step-down dc-to-dc converter	ADP2108AUJZ-1.8-R7	Analog Devices/ ADP2108AUJZ-1.8-R7
1	U201	Analog-to-digital converter	AD9286BCPZ-500	Analog Devices/ AD9286BCPZ-500
1	U301	IC tiny logic UHS dual buffer	NC7WZ07P6X	Fairchild/NC7WZ07P6X
1	U302	IC tiny logic UHS dual buffer	NC7WZ16P6X	Fairchild/NC7WZ16P6X
1	U401	Ultralow distortion differential ADC driver	ADA4937-1YCPZ-R7	Analog Devices/ ADA4937-1YCPZ-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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