

PI6C485311

3.3V Low Skew 1-to-2 Differential to LVPECL Fanout Buffer

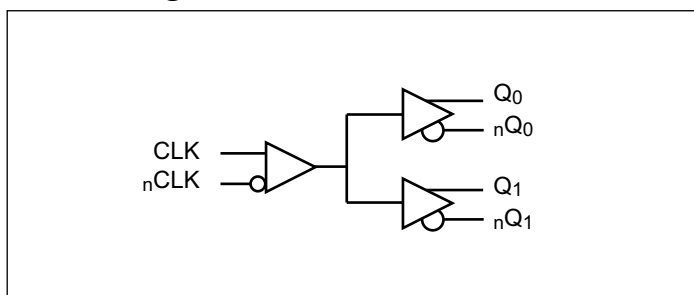
Features

- Pin-to-pin compatible to ICS85311
- Maximum operation frequency: 800MHz
- 2 pair of differential LVPECL outputs
- CLK, nCLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- Output Skew: 100ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V power supply
- Operating Temperature: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green available):
 - ♦ 8-pin SOIC (W)
 - ♦ 8-pin MSOP (U)

Description

The PI6C485311 is a high-performance low-skew LVPECL fanout buffer. PI6C485311 features two selectable differential inputs and translates to four LVPECL ultra-low jitter outputs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LVPECL or LVDS or LVHSTL or SSTL or HCSL signals, and PCLK input accepts LVPECL or SSTL or CML signals. PI6C485311 is ideal for differential to LVPECL translations and/or LVPECL clock distribution. Typical clock translation and distribution applications are data-communications and telecommunications.

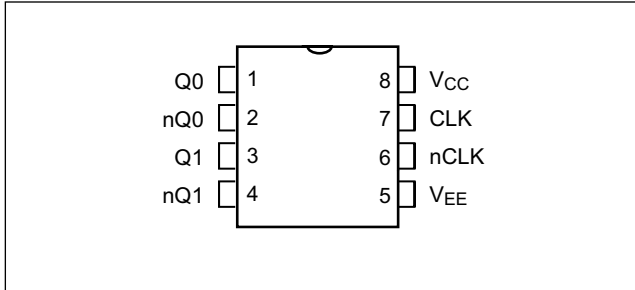
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Name	Pin #	Type	Description
V _{EE}	5	P	Connect to Negative power supply
CLK	7	I_PD	Non-inverting differential clock input
nCLK	6	I_PU	Inverting differential clock input
V _{CC}	8	P	Connect to 3.3V.
Q ₁ , nQ ₁	3,4	O	Differential output pair, LVPECL interface level.
Q ₀ , nQ ₀	1,2	O	Differential output pair, LVPECL interface level.

Note:

1. I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance				4	pF
R _{pullup}	Input Pullup Resistance			50		KΩ
R _{pulldown}	Input Pulldown Resistance			50		

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD} , V_{DDO})	-0.5 to +4.6V
Inputs (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input).....	2000V min (HBM)
Junction Temperature	150 °C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{EE}	Power Supply Current	500 MHz			60	mA

Differential DC Input Characteristics ($T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3.0V$ to $3.6V$ unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.6V$		5	uA
		CLK	$V_{IN} = V_{CC} = 3.6V$		150	uA
I_{IL}	Input Low Current	nCLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-150		uA
		CLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-5		uA
V_{PP}	Peak-to-peak Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage ^(1, 2)		$V_{EE}+0.5$		$V_{CC}-0.85V$	V

Notes:

- For single ended applications, the maximum input voltage for CLK and nCLK is $V_{CC}+0.3V$
- Common mode voltage is defined as V_{IH} .

LVPECL DC Characteristics

($T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3.0V$ to $3.6V$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.6V$		5	μA
		CLK	$V_{IN} = V_{CC} = 3.6V$		150	
I_{IL}	Input Low Current	nCLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-150		μA
		CLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-5		
V_{PP}	Peak-to-peak Voltage		0.3		1	V
V_{CMR}	Common Mode Input Voltage; Note ^(1,2)		$V_{EE}+1.5$		V_{CC}	
V_{OH}	Output High Voltage		$V_{CC}-1.4$		$V_{CC}-0.9$	
V_{OL}	Output Low Voltage		$V_{CC}-2.0$		$V_{CC}-1.6$	
V_{SWING}	Peak-to-peak Output Voltage Swing		0.6		1.0	

Notes:

- For single ended applications, the maximum input voltage for PCLK and nPCLK is $V_{CC}+0.3V$.
- Common mode voltage is defined as V_{IH} .

AC Characteristics⁽¹⁾ ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.0\text{V}$ to 3.6V , $R_L = 50\Omega$ to $V_{CC} - 2\text{V}$, unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{\max}	Output Frequency				800	MHz
t_{pd}	Propagation Delay ⁽²⁾		1.0		2.0	ns
Tsk(o)	Output-to-output Skew ⁽³⁾				100	ps
Tsk(pp)	Part-to-part Skew ⁽⁴⁾				150	
t_r/t_f	Output Rise/Fall time	20% - 80%	75		300	
odc	Output duty cycle		40		60	%

Notes:

1. All parameters are measured at 500MHz unless noted otherwise
2. Measured from the $V_{CC}/2$ of the input to the differential output crossing point
3. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.

Applications Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R1/R2 = 0.609$.

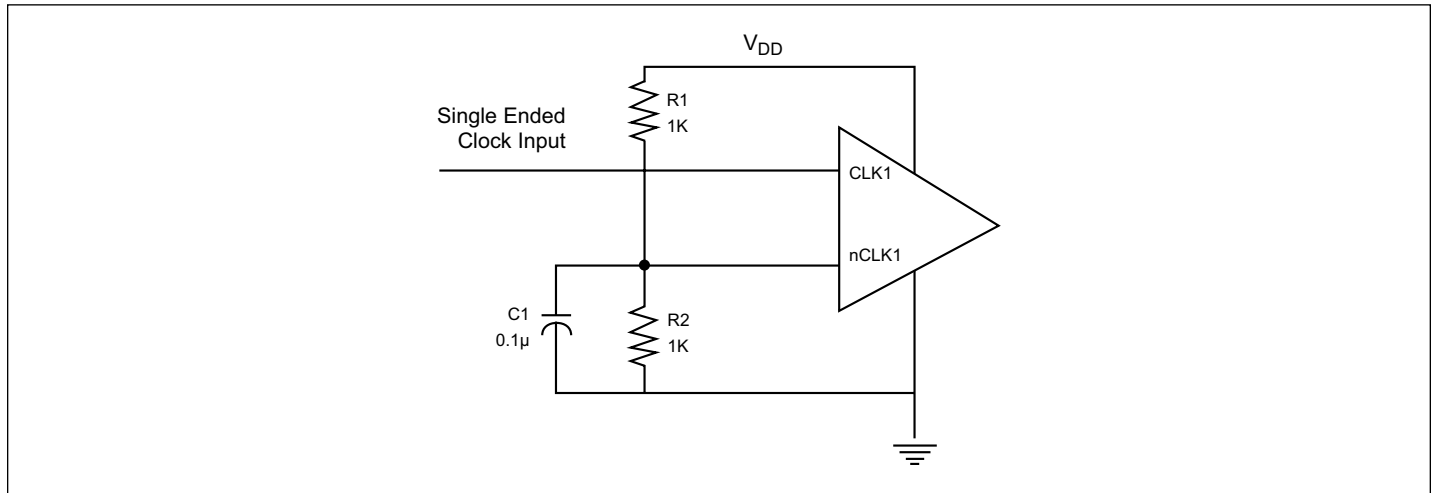


Figure 1: Single-ended Signal Driving Differential Input

Part Marking

W Package



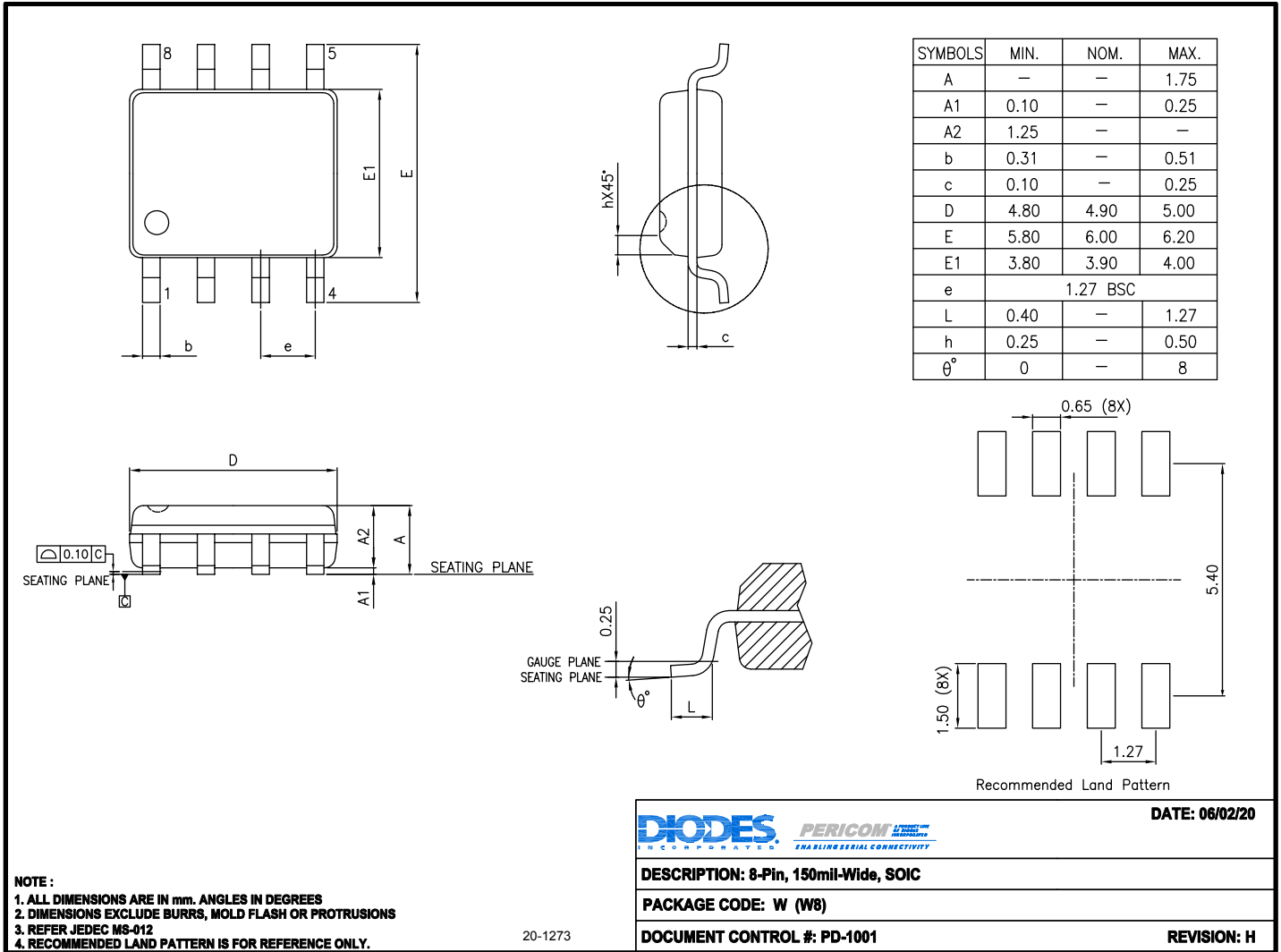
A: Die Rev
YW: Year & Workweek
1st X: Assembly Code
2nd X: Fab Code

U Package

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

PI6C485311

Packaging Mechanical
8-SOIC (W)



PI6C485311

8-MSOP (U)

PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

RECOMMENDED LAND PATTERN(unit:mm)

NOTE:
 1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
 2. REFER JEDEC MO-187F/AA
 3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.
 4. LAND PATTERN REFERENCE DIODES MSOP-8 PACKAGE INFORMATION.

DIODES PERICOM A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY	DATE: 11/04/19
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP	
PACKAGE CODE: U (U8)	
DOCUMENT CONTROL #: PD-1261	REVISION: H

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI6C485311WEX	W	8-pin, 150mil-Wide (SOIC)
PI6C485311UEX	U	8-pin, Mini Small Outline Package (MSOP)

Notes:

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2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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