DEMO CIRCUIT DC1298
QUICK START GUIDE

LTM9002 14 bit Dual Channel IF/Baseband Receiver Subsystem

DESCRIPTION

Demonstration circuit 1298 is an evaluation board featuring Linear Technology Corporation's LTM9002 14-bit Dual Receiver Subsystem. DC1298 demonstrates good circuit layout techniques and recommended external circuitry for optimal system performance.

DC1298 comes with Linear Technology's 14-bit LTM9002 amplifier/ADC subsystem installed. The board includes a wideband input transformer (for evaluation with a single-ended RF signal generator) and output CMOS buffers. DC1298 plugs into the DC890 Data Acquisition demo board and the output can be easily analyzed with Linear Technology's PScope data processing software, which is available for no charge on our website at http://www.linear.com.

Design files for this circuit board are available. Call the LTC factory.

QUICK START PROCEDURE

Validating the performance of the LTM9002 is simple with DC1298, and requires only two input sources, a clock source, a computer, and a lab power supply. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Connect the power supply as shown in Figure 1. There is an on-board low-noise voltage regulator that provide the four supply voltages for the DC1298. The entire board and all components share a common ground. The power supply should be a low-noise lab power supply capable of supplying at least 1 Amp.

2. Provide an encode clock to the ADC via SMA connector J1. Use a low-phase-noise clock source such as a filtered RF signal generator or a high-quality clock oscillator. **Obtain DC1216 for a low-phase-noise ADC clock source that can plug directly into DC1298.**

   NOTE. Similar to having a noisy input, a high-jitter (phase noise) encode clock will degrade the signal-to-noise ratio (SNR) of the system.

Table 1: DC1298 Connectors and Jumpers

REFERENCE	FUNCTION
J1 (+INA)	Board IF Signal Input, channel A single-ended. Impedance-matched to 50Ω for use with lab signal generators.
J2 (-INA)	Board IF Signal Input, channel A. Normally not used, but can be configured as the negative side of a differential input.
J3 (+INB)	Board IF Signal Input, channel B. Normally not used, but can be configured as the negative side of a differential input.
J4 (-INB)	Board IF Signal Input, channel B single-ended. Impedance-matched to 50Ω for use with lab signal generators.
J6 (CLKIN)	Board Clock Input. Impedance-matched to 50Ω. Drive with a low-phase-noise clock oscillator or filtered sine wave signal source.
E1 (EXT REF A)	Reference input to adjust the full-scale range of the FT107, channel A. Connects to the SENSE pin; by default, tied to VDD for internal reference.
E2 (EXT REF B)	Reference input to adjust the full-scale range of the FT107, channel B. Connects to the SENSE pin; by default, tied to VDD for internal reference.
JP1 (DAC I/O)	DAC serial interface.
JP2 (SENSE)	ADC sense voltages, default is VDD.

3. Apply an input signal to the board. For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the receiver.

4. Observe the ADC output with demo circuit DC890B, a USB cable, a Windows computer, and Linear Technology's PScope data processing software.

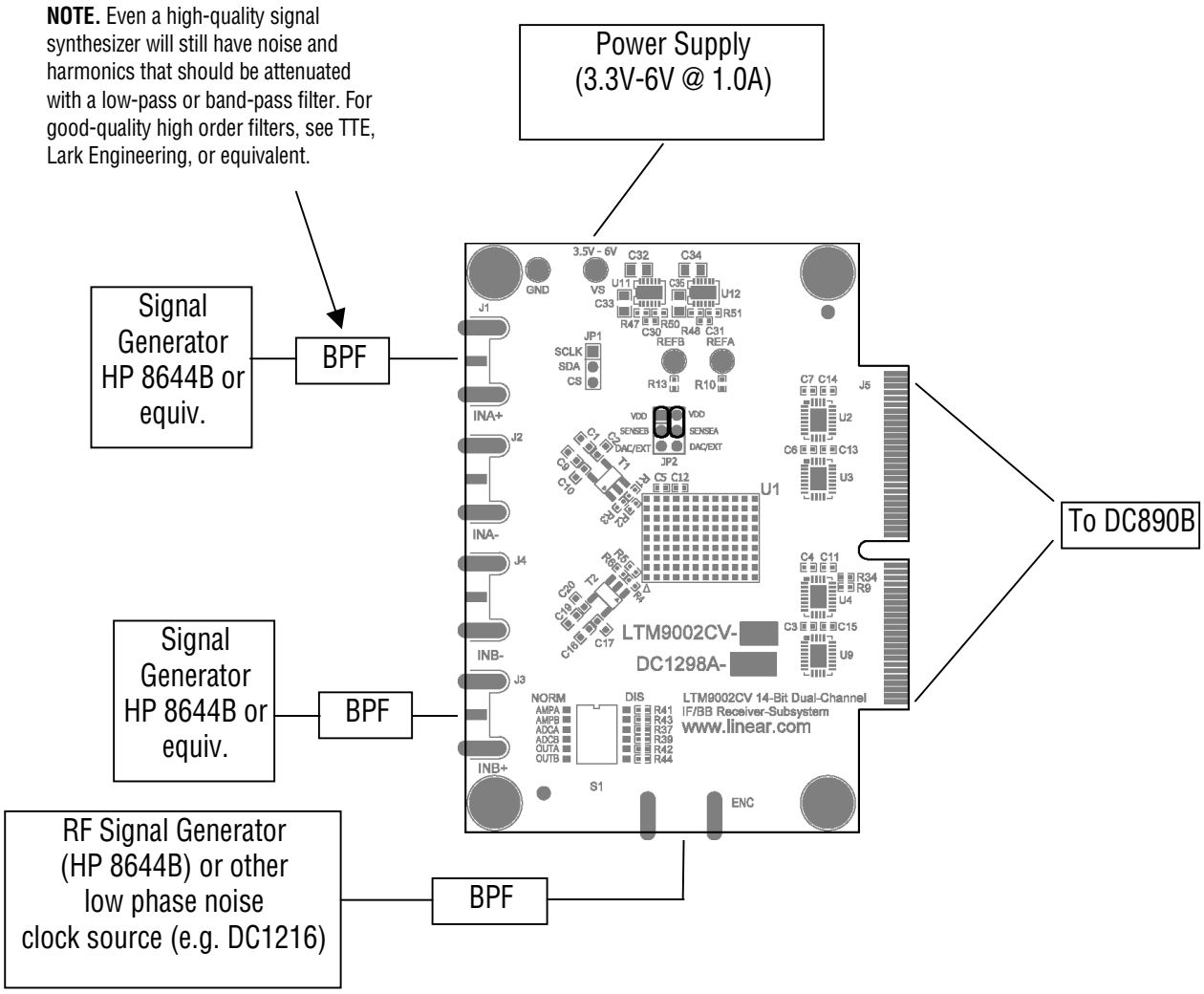

Figure 1. Proper Measurement Equipment Setup

USING PSCOPE SOFTWARE

PScope, downloadable from Linear Technology's website http://www.linear.com/, processes data from the DC890B FastDAACS board and displays FFT and signal analysis information on the computer screen.

The on-board EEPROM U5 should enable automatic board detection and auto-configuration of the software, but if the user wishes to change the settings, they can easily do so.

From the Configure menu in the toolbar, uncheck “Autodetect Device”. The default settings for DC1298 are shown in Figure 2.

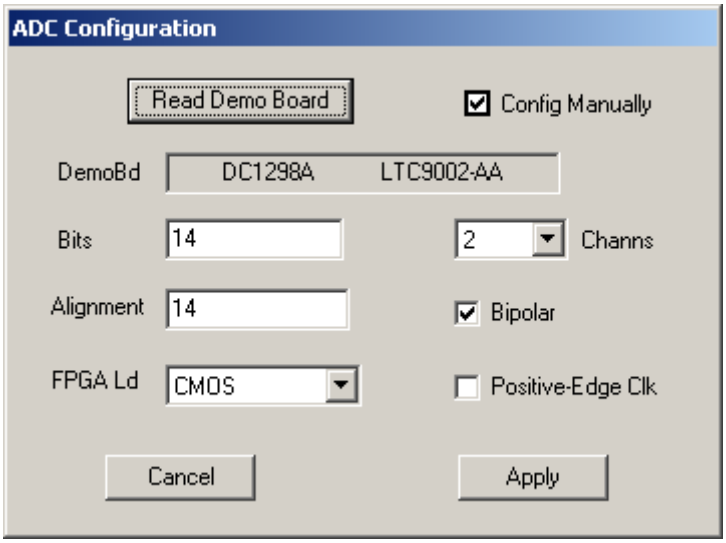

Figure 2. Entering the correct device information for your ADC. Select the correct parameters for the DC1298. Under normal conditions, PScope should automatically recognize the board and adjust the software settings accordingly.

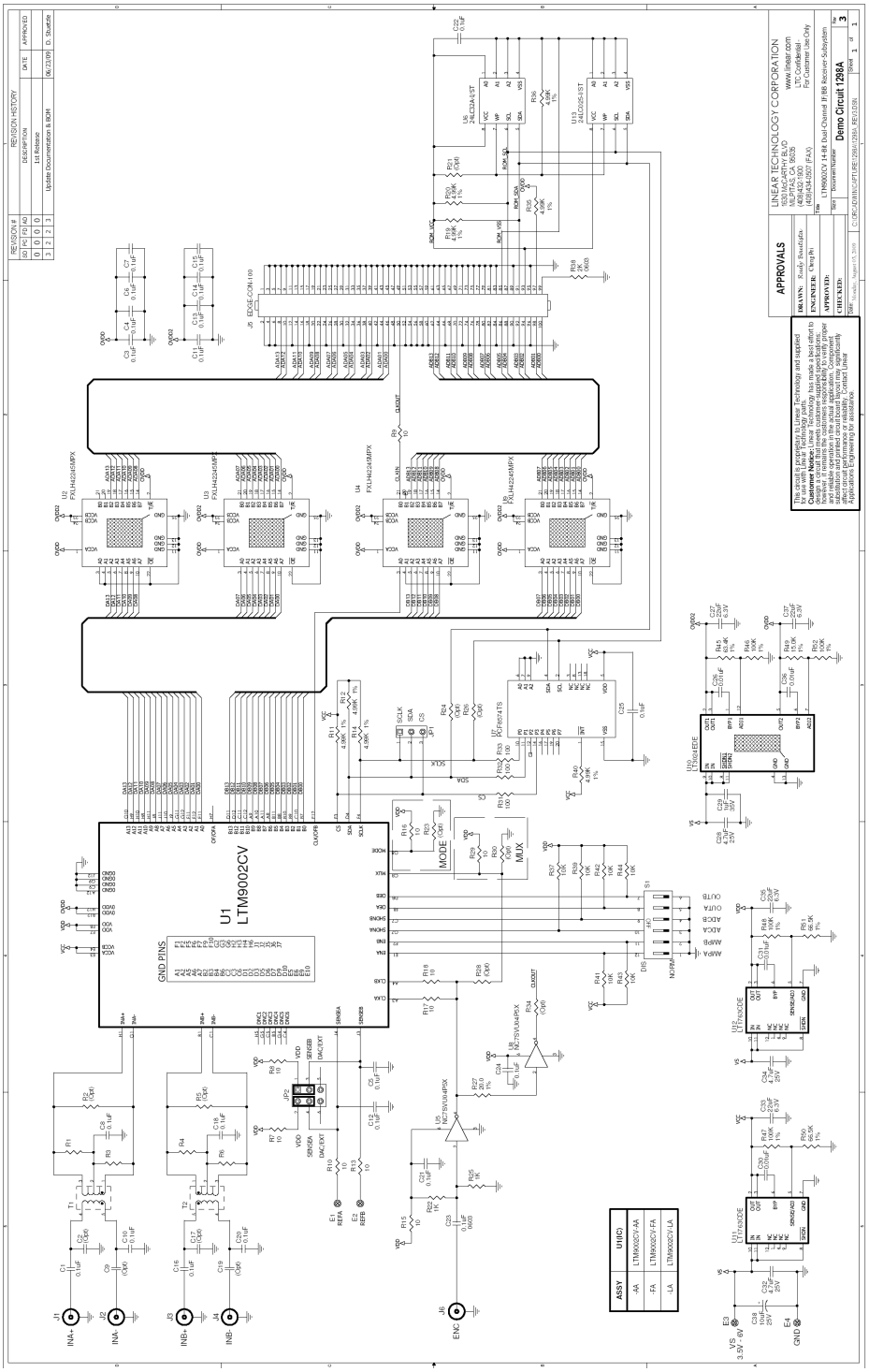

Figure 3. Schematic