Si86S63x/64x/S4x/Q4x/66x: Multi-Channel Digital Isolators

Robust, High Speed Low Power Multi-Channel Digital Isolators

Skyworks' new family of robust, low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. All device versions have CMOS thresholds and Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 150 Mbps are supported, and all devices achieve typical propagation delays of 10 ns. This family includes SPI capable product options and options that support QSPI with a direction control pin. Enable inputs provide a single point control for enabling and disabling outputs. A new sleep mode is included that helps conserve power by shutting down active circuits when enabled. Low-power mode operation options are also included that are optimized for saving power. Other ordering options include a choice of isolation ratings (3.75 and 6.0 kV_{RMS}) and product options for fail-safe operating mode to control the default output state during power loss. All products are safety certified by UL, CSA, VDE, and CQC. Products in wide-body packages support voltages of 6.0 kV_{RMS} with 1 minute withstand capability per UL 1577. These products are certified to the latest IEC 60747-17 reinforced specification and can be safely used in high-power applications like inverters and motor drives.

Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- Industrial automation systems
- Medical electronics
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid Electric Vehicles
- Battery Electric Vehicles

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for 1 minute
- CSA certification conformity
  - IEC 62368-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-17 (reinforced)
  - EN 62368-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1-2011

KEY FEATURES

- High-speed operation: DC to 150 Mbps
- No start-up initialization required
- Wide Supply Voltage: 2.25 – 5.5 V
- Up to 6000 V_{RMS} isolation
- Reinforced IEC 60747-17 rating
- High electromagnetic immunity
- Low power and sleep mode options
- Tri-state outputs with enable
- Schmitt trigger + CMOS threshold inputs
- Selectable fail-safe mode
  - Default high or low output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 3.5 ns pulse width distortion
- Transient Immunity of 100 kV/µs (min)
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - WB SOIC-16
  - NB SOIC-16
  - QSOP-16
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Table of Contents

1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Ordering Guide for 3-Channel Digital Isolators[1, 2, 3, 4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5, 6] Pending Release	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV)	Package
Si86S630BC-IS1	Si86S630BC-AS1	3	0	0	Low	3.75	NB SOIC-16
Si86S630BE-IS2	Si86S630BE-AS2	3	0	0	Low	6.0	WB SOIC-16
Si86S630EC-IS1	Si86S630EC-AS1	3	0	0	High	3.75	NB SOIC-16
Si86S630EE-IS2	Si86S630EE-AS2	3	0	0	High	6.0	WB SOIC-16
Si86S631BC-IS1	Si86S631BC-AS1	2	1	0	Low	3.75	NB SOIC-16
Si86S631BE-IS2	Si86S631BE-AS2	2	1	0	Low	6.0	WB SOIC-16
Si86S631EC-IS1	Si86S631EC-AS1	2	1	0	High	3.75	NB SOIC-16
Si86S631EE-IS2	Si86S631EE-AS2	2	1	0	High	6.0	WB SOIC-16

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125°C.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

Table 1.2. Ordering Guide for 4-Channel Digital Isolators[1, 2, 3, 4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5, 6] Pending Release	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV)	Package
Si86S640BC-IS1	Si86S640BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86S640BB-IU	Si86S640BB-AU	4	0	0	Low	2.5	QSOP-16
Si86S640BE-IS2	Si86S640BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86S640EC-IS1	Si86S640EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86S640EB-IU	Si86S640EB-AU	4	0	0	High	2.5	QSOP-16
Si86S640EE-IS2	Si86S640EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86S641BC-IS1	Si86S641BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86S641BB-IU	Si86S641BB-AU	3	1	0	Low	2.5	QSOP-16
Si86S641BE-IS2	Si86S641BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86S641EC-IS1	Si86S641EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86S641EB-IU	Si86S641EB-AU	3	1	0	High	2.5	QSOP-16
Si86S641EE-IS2	Si86S641EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86S642BC-IS1	Si86S642BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86S642BB-IU	Si86S642BB-AU	2	2	0	Low	2.5	QSOP-16
Si86S642BE-IS2	Si86S642BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86S642EC-IS1	Si86S642EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86S642EB-IU	Si86S642EB-AU	2	2	0	High	2.5	QSOP-16
Si86S642EE-IS2	Si86S642EE-AS2	2	2	0	High	6.0	WB SOIC-16
Si86S640FC-IS1	Si86S640FC-AS1	4	0	36	Low	3.75	NB SOIC-16
Si86S640FE-IS2	Si86S640FE-AS2	4	0	36	Low	6.0	WB SOIC-16
Si86S640HC-IS1	Si86S640HC-AS1	4	0	36	High	3.75	NB SOIC-16
Si86S640HE-IS2	Si86S640HE-AS2	4	0	36	High	6.0	WB SOIC-16
Si86S641FC-IS1	Si86S641FC-AS1	3	1	36	Low	3.75	NB SOIC-16
Si86S641FE-IS2	Si86S641FE-AS2	3	1	36	Low	6.0	WB SOIC-16
Si86S641HC-IS1	Si86S641HC-AS1	3	1	36	High	3.75	NB SOIC-16
Si86S641HE-IS2	Si86S641HE-AS2	3	1	36	High	6.0	WB SOIC-16
Si86S642FC-IS1	Si86S642FC-AS1	2	2	36	Low	3.75	NB SOIC-16
Si86S642FE-IS2	Si86S642FE-AS2	2	2	36	Low	6.0	WB SOIC-16
Si86S642HC-IS1	Si86S642HC-AS1	2	2	36	High	3.75	NB SOIC-16
Si86S642HE-IS2	Si86S642HE-AS2	2	2	36	High	6.0	WB SOIC-16
Low-Power Mode							
Si86SL40BC-IS1	Si86SL40BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86SL40BE-IS2	Si86SL40BE-AS2	4	0	0	Low	6.0	WB SOIC-16

Ordering Part Numbers (OPNs)	Automotive OPNs[5, 6] Pending Release	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV)	Package
Si86SL40EC-IS1	Si86SL40EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86SL40EE-IS2	Si86SL40EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86SL41BC-IS1	Si86SL41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SL41BE-IS2	Si86SL41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SL41EC-IS1	Si86SL41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SL41EE-IS2	Si86SL41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SL42BC-IS1	Si86SL42BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86SL42BE-IS2	Si86SL42BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86SL42EC-IS1	Si86SL42EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86SL42EE-IS2	Si86SL42EE-AS2	2	2	0	High	6.0	WB SOIC-16
Sleep Mode							
Si86SM40BC-IS1	Si86SM40BC-AS1	4	0	0	Low	3.75	NB SOIC-16
Si86SM40BE-IS2	Si86SM40BE-AS2	4	0	0	Low	6.0	WB SOIC-16
Si86SM40EC-IS1	Si86SM40EC-AS1	4	0	0	High	3.75	NB SOIC-16
Si86SM40EE-IS2	Si86SM40EE-AS2	4	0	0	High	6.0	WB SOIC-16
Si86SM41BC-IS1	Si86SM41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SM41BE-IS2	Si86SM41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SM41EC-IS1	Si86SM41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SM41EE-IS2	Si86SM41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SM42BC-IS1	Si86SM42BC-AS1	2	2	0	Low	3.75	NB SOIC-16
Si86SM42BE-IS2	Si86SM42BE-AS2	2	2	0	Low	6.0	WB SOIC-16
Si86SM42EC-IS1	Si86SM42EC-AS1	2	2	0	High	3.75	NB SOIC-16
Si86SM42EE-IS2	Si86SM42EE-AS2	2	2	0	High	6.0	WB SOIC-16
SPI Mode							
Si86SS41BC-IS1	Si86SS41BC-AS1	3	1	0	Low	3.75	NB SOIC-16
Si86SS41BE-IS2	Si86SS41BE-AS2	3	1	0	Low	6.0	WB SOIC-16
Si86SS41EC-IS1	Si86SS41EC-AS1	3	1	0	High	3.75	NB SOIC-16
Si86SS41EE-IS2	Si86SS41EE-AS2	3	1	0	High	6.0	WB SOIC-16
Si86SS51BC-IS1	Si86SS51BC-AS1	4	1	0	Low	3.75	NB SOIC-16
Si86SS51BE-IS2	Si86SS51BE-AS2	4	1	0	Low	6.0	WB SOIC-16
Si86SS51EC-IS1	Si86SS51EC-AS1	4	1	0	High	3.75	NB SOIC-16
Si86SS51EE-IS2	Si86SS51EE-AS2	4	1	0	High	6.0	WB SOIC-16
Custom QSPI Implementation Mode							
Si86SQ44BB-IU	Si86SQ44BB-AU	4	0	0	Low	2.5	QSOP-16
Si86SQ44BE-IS2	Si86SQ44BE-AS2	4	0	0	Low	6.0	WB SOIC-16

Ordering Part Numbers (OPNs)	Automotive OPNs[5, 6] Pending Release	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV)	Package
Si86SQ44EB-IU	Si86SQ44EB-AU	4	0	0	High	2.5	QSOP-16
Si86SQ44EE-IS2	Si86SQ44EE-AS2	4	0	0	High	6.0	WB SOIC-16

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125°C.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

Table 1.3. Ordering Guide for 6-Channel Digital Isolators[1, 2, 3, 4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5, 6] Pending Release	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV)	Package
Si86S660BC-IS1	Si86S660BC-AS1	6	0	0	Low	3.75	NB SOIC-16
Si86S660BB-IU	Si86S660BB-AU	6	0	0	Low	2.5	QSOP-16
Si86S660BE-IS2	Si86S660BE-AS2	6	0	0	Low	6.0	WB SOIC-16
Si86S660EC-IS1	Si86S660EC-AS1	6	0	0	High	3.75	NB SOIC-16
Si86S660EB-IU	Si86S660EB-AU	6	0	0	High	2.5	QSOP-16
Si86S660EE-IS2	Si86S660EE-AS2	6	0	0	High	6.0	WB SOIC-16
Si86S661BC-IS1	Si86S661BC-AS1	5	1	0	Low	3.75	NB SOIC-16
Si86S661BB-IU	Si86S661BB-AU	5	1	0	Low	2.5	QSOP-16
Si86S661BE-IS2	Si86S661BE-AS2	5	1	0	Low	6	WB SOIC-16
Si86S661EC-IS1	Si86S661EC-AS1	5	1	0	High	3.75	NB SOIC-16
Si86S661EB-IU	Si86S661EB-AU	5	1	0	High	2.5	QSOP-16
Si86S661EE-IS2	Si86S661EE-AS2	5	1	0	High	6	WB SOIC-16
Si86S662BC-IS1	Si86S662BC-AS1	4	2	0	Low	3.75	NB SOIC-16
Si86S662BB-IU	Si86S662BB-AU	4	2	0	Low	2.5	QSOP-16
Si86S662BE-IS2	Si86S662BE-AS2	4	2	0	Low	6	WB SOIC-16
Si86S662EC-IS1	Si86S662EC-AS1	4	2	0	High	3.75	NB SOIC-16
Si86S662EB-IU	Si86S662EB-AU	4	2	0	High	2.5	QSOP-16
Si86S662EE-IS2	Si86S662EE-AS2	4	2	0	High	6	WB SOIC-16
Si86S663BC-IS1	Si86S663BC-AS1	3	3	0	Low	3.75	NB SOIC-16
Si86S663BB-IU	Si86S663BB-AU	3	3	0	Low	2.5	QSOP-16
Si86S663BE-IS2	Si86S663BE-AS2	3	3	0	Low	6.0	WB SOIC-16
Si86S663EC-IS1	Si86S663EC-AS1	3	3	0	High	3.75	NB SOIC-16
Si86S663EB-IU	Si86S663EB-AU	3	3	0	High	2.5	QSOP-16
Si86S663EE-IS2	Si86S663EE-AS2	3	3	0	High	6.0	WB SOIC-16

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125°C.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

2. Functional Description

2.1 Theory of Operation

The operation of an Si86Sx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86Sx channel is shown in the figure below.

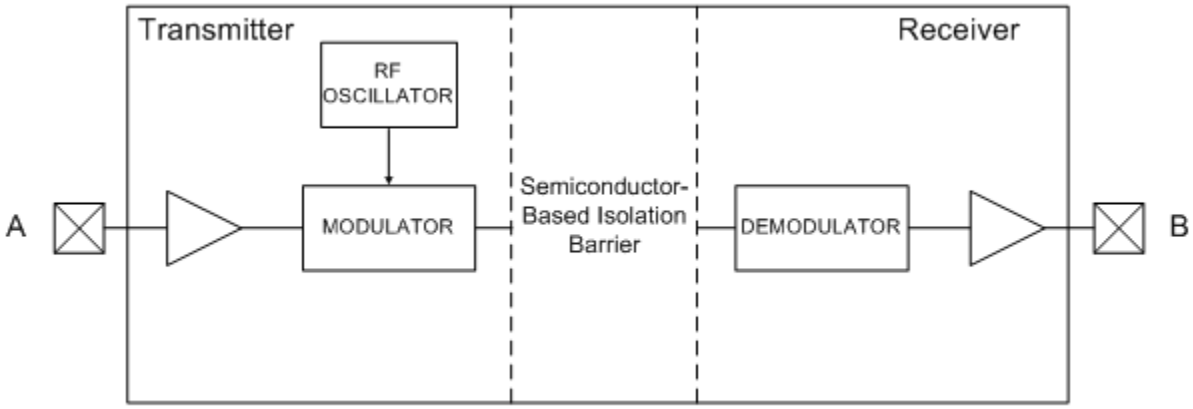

Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields. See the following figure for more details.

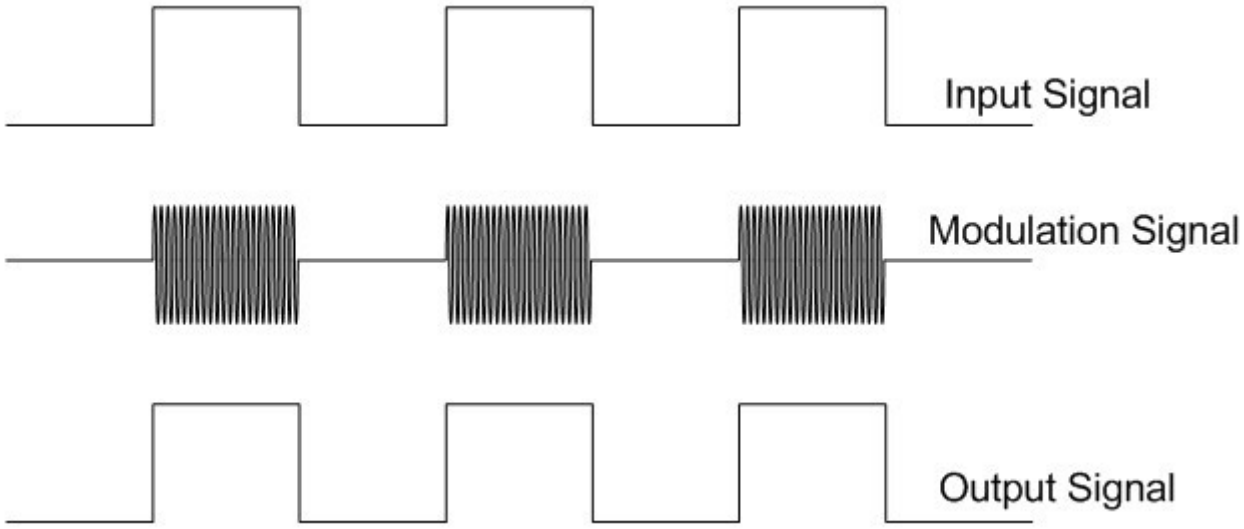

Figure 2.2. Modulation Scheme

3. Device Operation and System Overview

Device behavior during start-up, normal operation, and shutdown is shown in Figure 3.1 Device Behavior during Startup on page 11, where UVLO+ and UVLO– are the respective positive-going and negative-going thresholds. Refer to the following tables to determine outputs when power supply (VDD) is not present and for logic conditions when enable pins are used.

Table 3.1. Si86S6x/Lx/Mx Logic Operation

V_I Input[1, 2]	EN/SMb[3]	VDDI State[1, 4, 5, 6]	VDDO State[1, 4, 5, 6]	V_O Output[1, 2]	Comments
H	H or open	P	P	H	Normal operation
L	H or open	P	P	L	
X	L	P	P	Hi-Z	
X	X	UP	P	L[6]	Default low options
				H[6]	Default high options
X	X	P	UP	UD[7]	Upon transition of VDDO from un-powered to powered, V_O returns to correct state.[7]

Note:

1. VI and VO are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the input and output sides respectively.
2. X = Not Applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance; UD = Undetermined
3. EN1/EN2 enable pins control the state of all outputs on the same side as the pin as stated in table above. For options with sleep mode 1, EN1/EN2 enable pins also turn off circuits on that side, allowing for a low power mode. The SMb pin controls the state of all outputs on the device, including ones on the isolated side, as well as allowing the device to be in low power mode as described in Features Description Section 3.4 Device Features and System Overview.
4. “Powered” state (P) is defined as 2.25 V < VDD < 5.5 V.
5. “Unpowered” state (UP) is defined as VDD <2.25V.
6. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
7. UD =Undetermined. Refer to Figure 3.1 Device Behavior during Startup on page 11, the start-up time from unpowered state, below 1.7 V (RSTb) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in Figure 3.1) but stays above RSTb level, the start-up time is 1 µs.

Table 3.2. Si86SS Logic Operation

V_I Input[1, 2]	VDDI State	VDDO State[1, 3, 4]	V_I Output[1, 2]	Comments
H	P	P	H	Normal operation
L	P	P	L	
X	UP	P	L	Default low options
			H	Default high options
X	P	UP	UD[5]	Upon transition of VDDO from unpowered to powered, V_O returns to correct state.[5]

Note:

1. VI and VO are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the input and output sides respectively.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. "Powered" state (P) is defined as 2.25 V < VDD < 5.5 V.
4. "Unpowered" state (UP) is defined as VDD <2.25 V.
5. UD =Undetermined. Refer to Figure 3.1 Device Behavior during Startup on page 11, the start-up time from unpowered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in Figure 3.1) but stays above RSTB level, the start-up time is 1 µs.

Table 3.3. Si86SQx Logic Operation

Ax[1]	Bx[1]	DIR[1]	ISO_DIR[1]	EN_A[1]	EN_B[1]	VDD1 State[2, 3]	VDD2 State[2, 3]	Notes
X	Hi-Z	H	H	X	L	P	P	Direction is set as input = A; output = B
L	L	H	H	X	H	P	P	Direction is set as input = A; output = B
H	H	H	H	X	H	P	P	Direction is set as input = A; output = B
Hi-Z	X	L	L	L	X	P	P	Direction is set as input = B; output = A
L	L	L	L	H	X	P	P	Direction is set as input = B; output = A
H	H	L	L	H	X	P	P	Direction is set as input = B; output = A
UD	X	X	L	X	X	UP	P	Direction is not set properly if any supply is UP[4]
X	UD	X	L	X	X	P	UP	Direction is not set properly if any supply is UP[4]

Note:

1. X = Not Applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance; UD = Undetermined.
2. "Powered" state (P) is defined as 2.25 V < VDD < 5.5 V.
3. "Unpowered" state (UP) is defined as VDD <2.25 V.
4. 100 kΩ weak pulldown on I/O when the VDD is UP.

3.1 Device Startup, UVLO, and Reset Functionality

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs. The start-up time of the device is estimated to be 0.3 ms due to the device initialization time. During this time, the outputs will have a 100 kΩ pulldown resistor that will pull the outputs low. After stabilization, the outputs will transition to the default output state indicated by the particular product option.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, referring to the figure below, Side A unconditionally enters UVLO when VDD1 falls below VDD1(UVLO–) and exits UVLO when VDD1 rises above VDD1(UVLO+). Side B operates the same as Side A with respect to its VDD2 supply.

Along with UVLO, each side has its own self biased circuitry that can detect supply going low enough and issue a complete reset of the part. This is done to avoid loss of device configuration for the particular product option. Referring to the figure below, Side A goes into reset as soon as VDD1 goes below RSTB- (~1.7 V) and comes out of reset when VDD1 goes above RSTB+. When the supply voltage is above RSTB+ the device configuration is re-loaded. Side B operates the same as Side A with respect to its VDD2 supply.

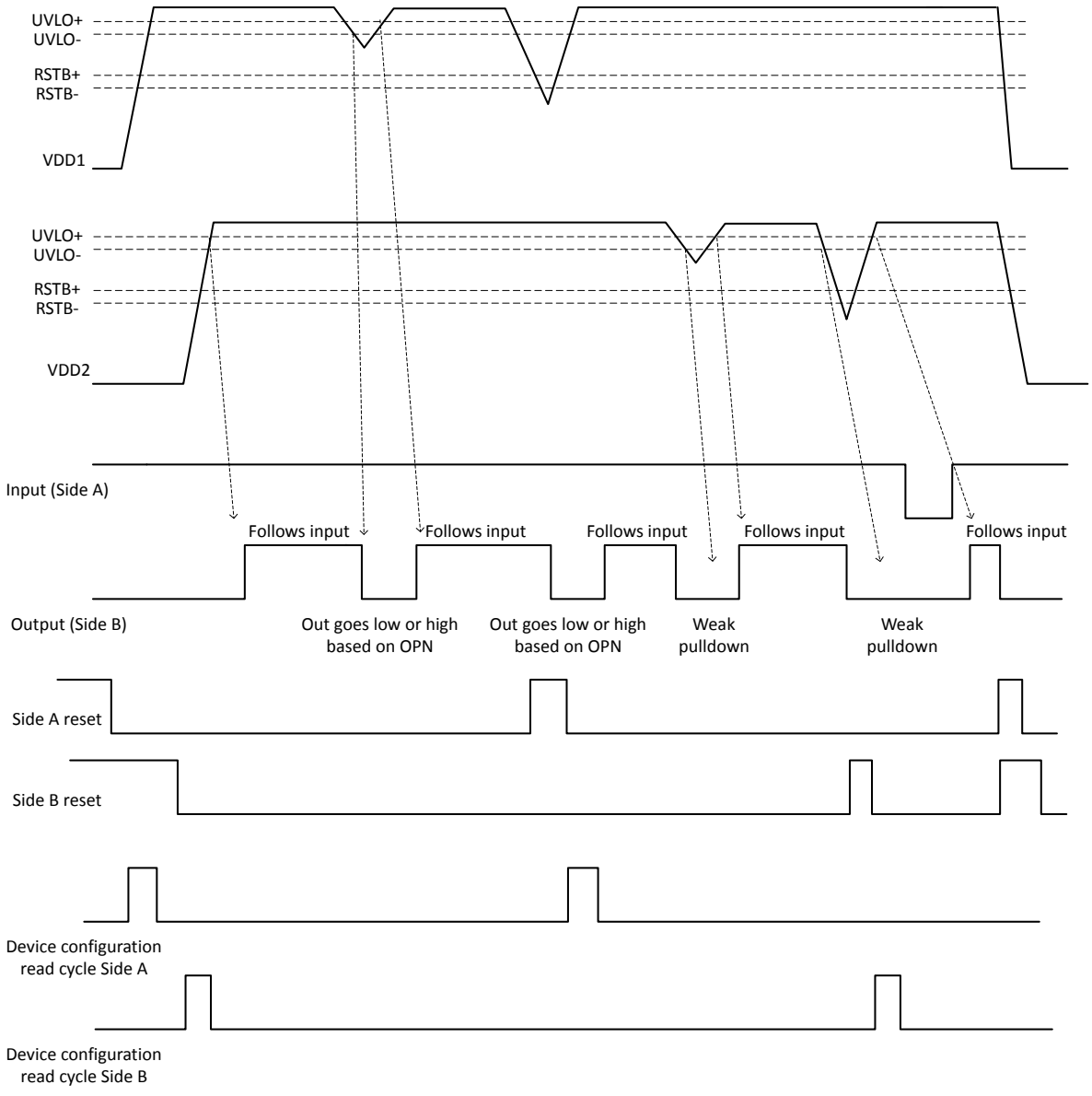

Figure 3.1. Device Behavior during Startup

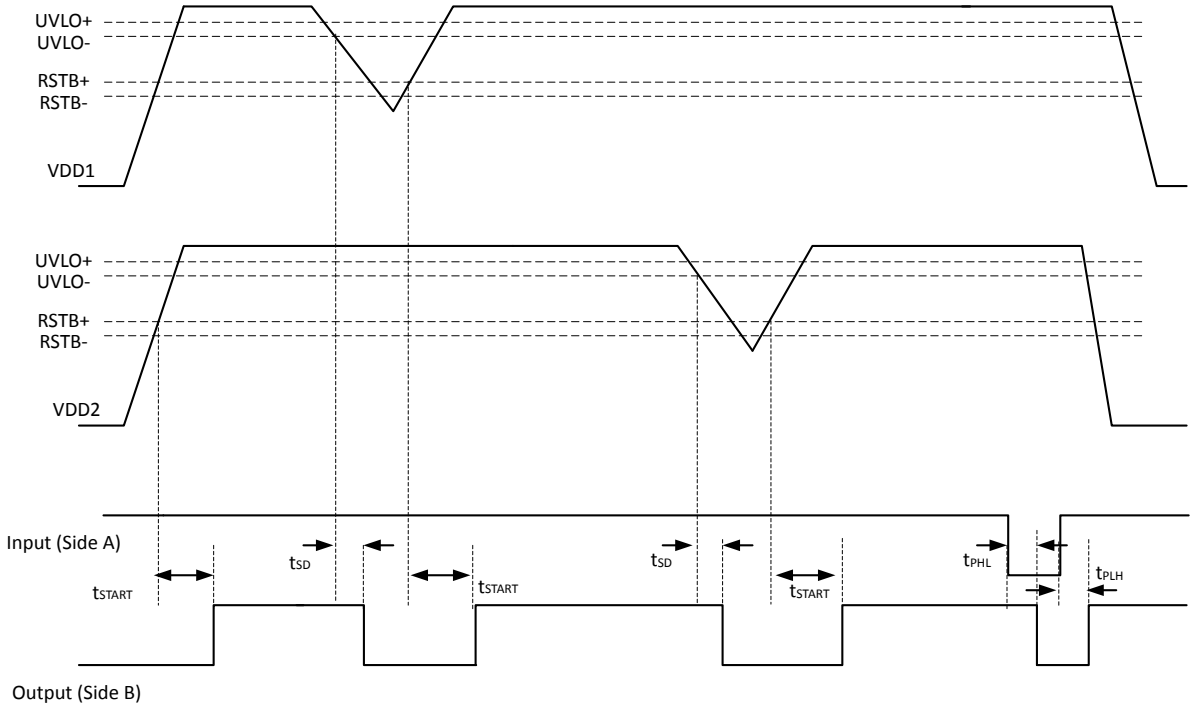

Figure 3.2. Device Behavior during Normal Operation

3.2 Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4.7 Insulation and Safety-Related Specifications on page 51 and Table 4.9 IEC 60747-17 Insulation Characteristics for Si86Sx [1] on page 52 detail the working voltage and creepage/clearance capabilities of the Si86Sx. These tables also detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 62368-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.2.1 Supply Bypass

The Si86Sx family requires a 0.1 µF bypass capacitor between VDD1 and GND1 and VDD2 and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.2.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

3.3 Fail-Safe Operating Mode

Si86Sx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 3.1 Si86S6x/Lx/Mx Logic Operation on page 9 and Section 1. Ordering Guide for more information.

3.4 Device Features and System Overview

3.4.1 Low Power Mode Operation

The Si86SLx devices are optimized for lower-power operation compared to the Si86S6x options. Typically, they consume 0.25 mA per channel less current in quiescent mode. The pinouts are no different than the Si86S6x options. This mode is always turned on for these devices. The architecture is tuned in favor of power savings rather than higher performance in terms of timing specifications.

3.4.2 Sleep Mode Operation

This new feature is very useful for power savings without compromising on performance. Instead of trading off data rate or CMTI performance for power savings, these options provide an SMb pin that can be used to put the device in sleep mode when not in operation. For example, the Si86SM42 is a four-channel device with two forward channels and two reverse channels. The left, “A”, side of the device has an SMb pin which when driven high (or left unconnected) enables the device but when driven low puts the device into sleep mode with 750 µA per side. In this mode, one isolation channel is always active to read the status of the SMb pin and to restart the entire device when SMb is driven high or left open, including the isolated side.

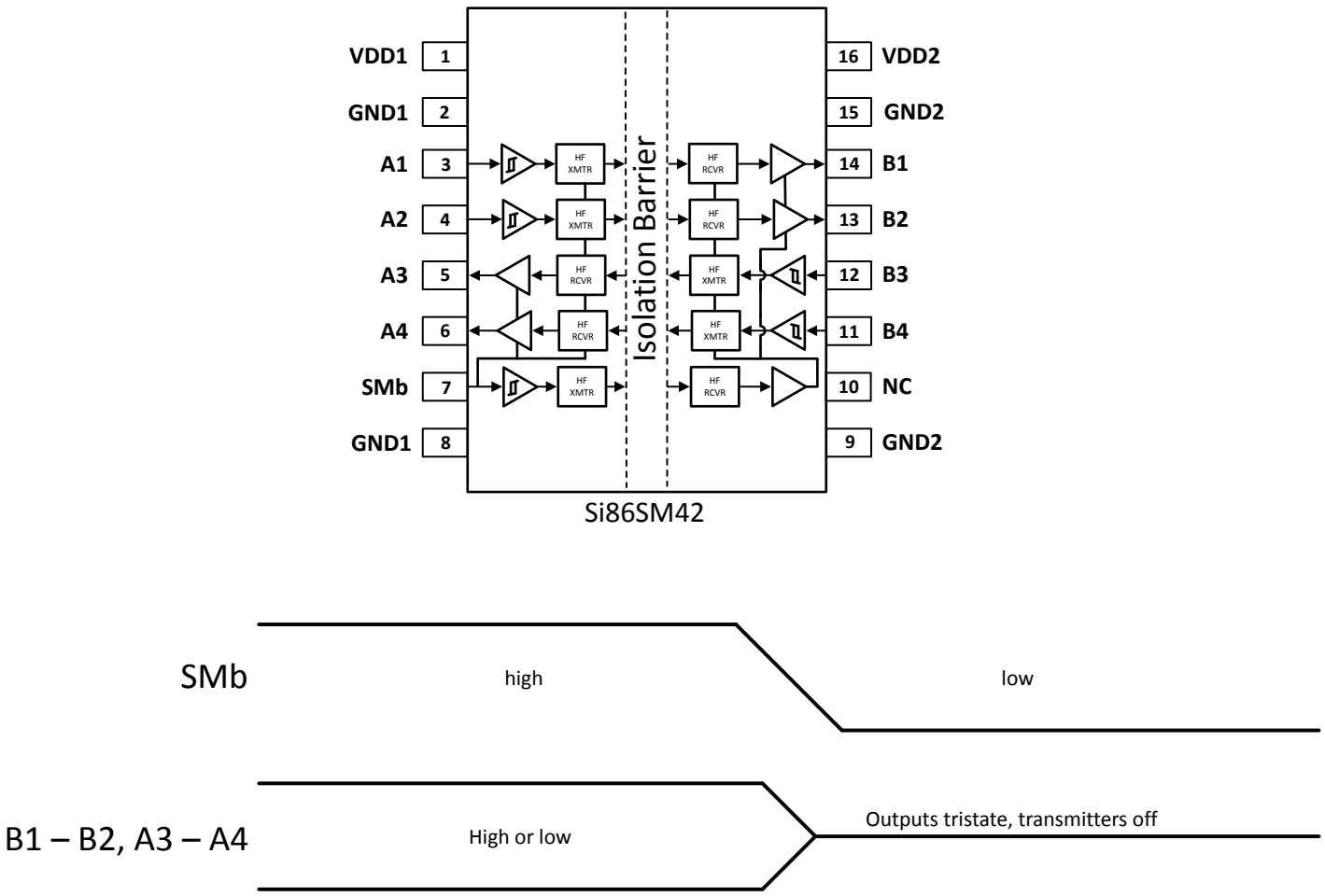

Figure 3.3. Sleep Mode Operation

3.4.3 SPI Operation for Si86SSx

The Si86SS41 is a four-channel device with three forward channels and one reverse channel. The non-isolated or main (controller) side input pins are MCSb (main side SPI chip select), MCLK (main side SPI clock), and MO (main side SPI MOSI). The non-isolated or main side output pin is MI (main side SPI MISO). The isolated or secondary (peripheral) side output pin is SCSb (secondary side SPI chip select), SCLK (secondary side SPI clock), and SI (secondary side SPI MOSI). The isolated or secondary side input pin is SO (secondary side SPI MISO). The Si86SS51 has an extra isolated digital channel that can be used for signals, such as Interrupt or Reset. For details, refer to "AN1359: Design Considerations for the Si86Sx Family".

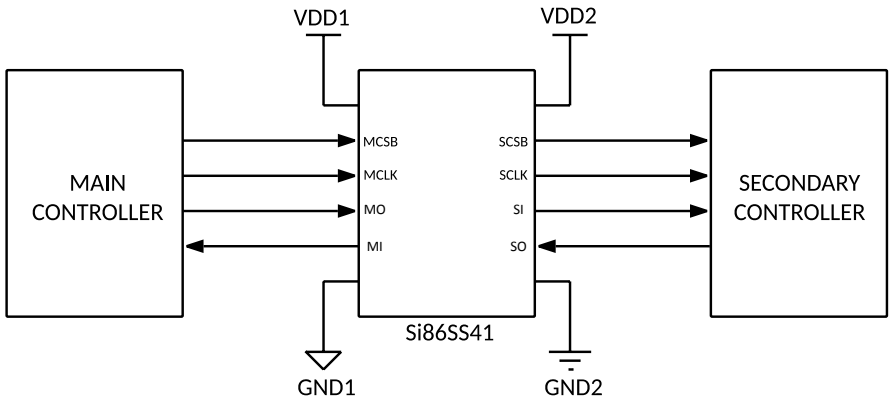

Figure 3.4. Basic SPI

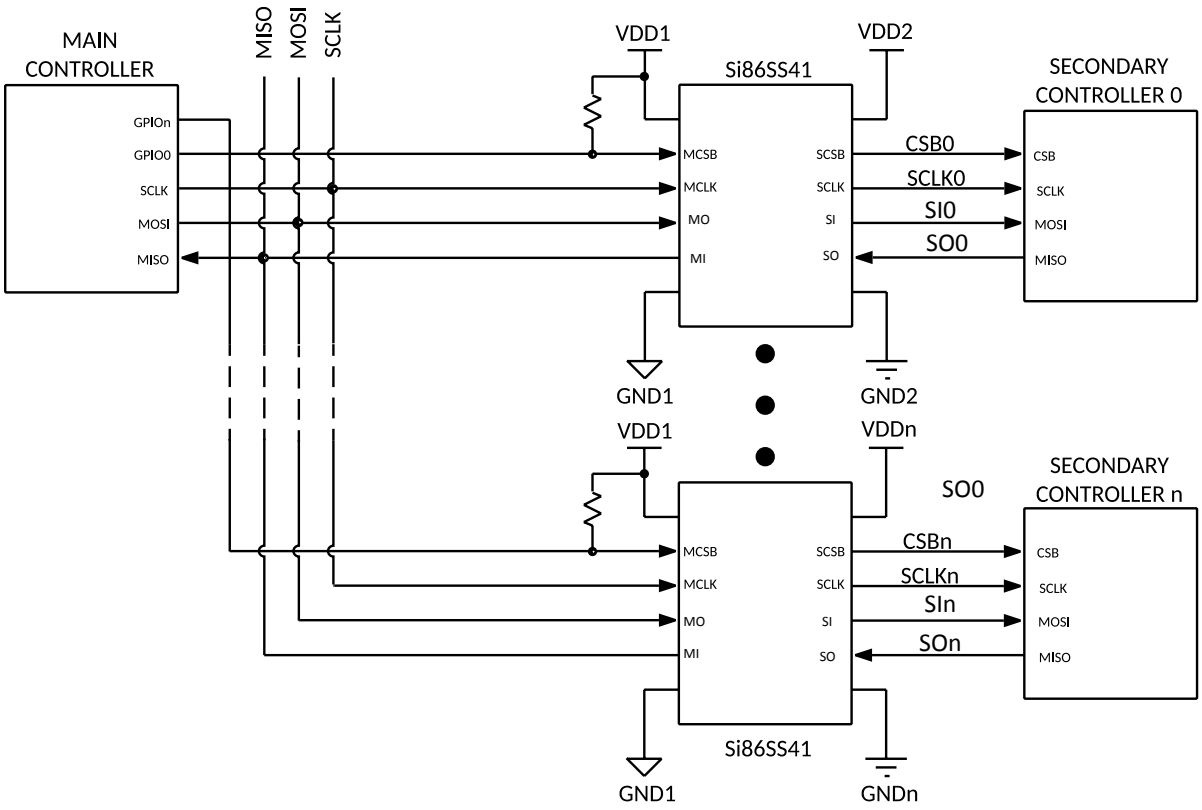

Figure 3.5. SPI Arrangement with Buffered MI

3.4.4 Custom QSPI Implementation Mode

The Si86SQ44 is a five-channel device with four reversible channels and one forward direction channel (DIR_IN). The DIR_IN pin when driven high configures the device for signal flow from Side A to Side B. The DIR_OUT pin provides an isolated copy of the DIR_IN state. The DIR_IN pin when driven low configures the device for signal flow from B to A. Each side of the device also has an enable pin (EN_A, EN_B) which when driven high enables the transmitter and receiver circuits, and when driven low configures the outputs as tristate. A 10 kΩ pull up resistor to the corresponding VDD is recommended for each enable pin.

The direction control feature of the Si86SQ44 can be useful in implementing a bi-directional (reversible) isolated bus.

Quad SPI is commonly used for faster data transfer from low pin count external memory. It is similar to SPI, but it has four data lines instead of two (MOSI and MISO), and the data lines operates in half-duplex mode with all four lines either reading or writing four bits of data on the same clock edge. Because QSPI operates in half-duplex, the Si86SQ44 can be used for the data lines as it provides direction control of four isolated channels.

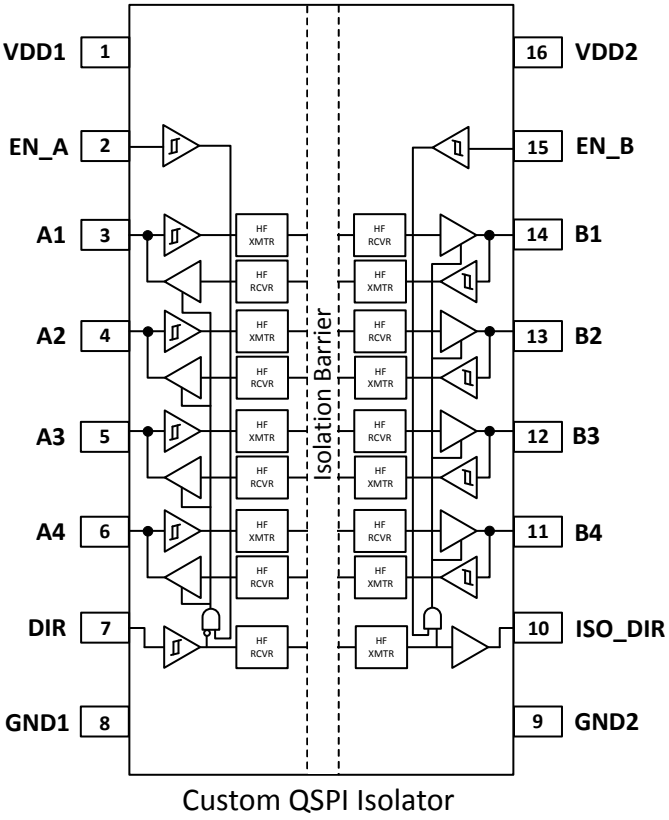

Figure 3.6. Si86SQ44 Configuration

3.4.5 Input Noise Filters with Deglitch Times of 36 ns

This product family is orderable with input deglitch filters which have delay times of 36 ns. These filters remove undesirable noise pulses (glitches) from the input signal so that the isolator only produces an output for a valid input. Any input pulse which lasts less than the deglitch time will not be passed by the filter. Any other input pulse will be passed by the filter and delayed by the filter delay time. Please see figures below.

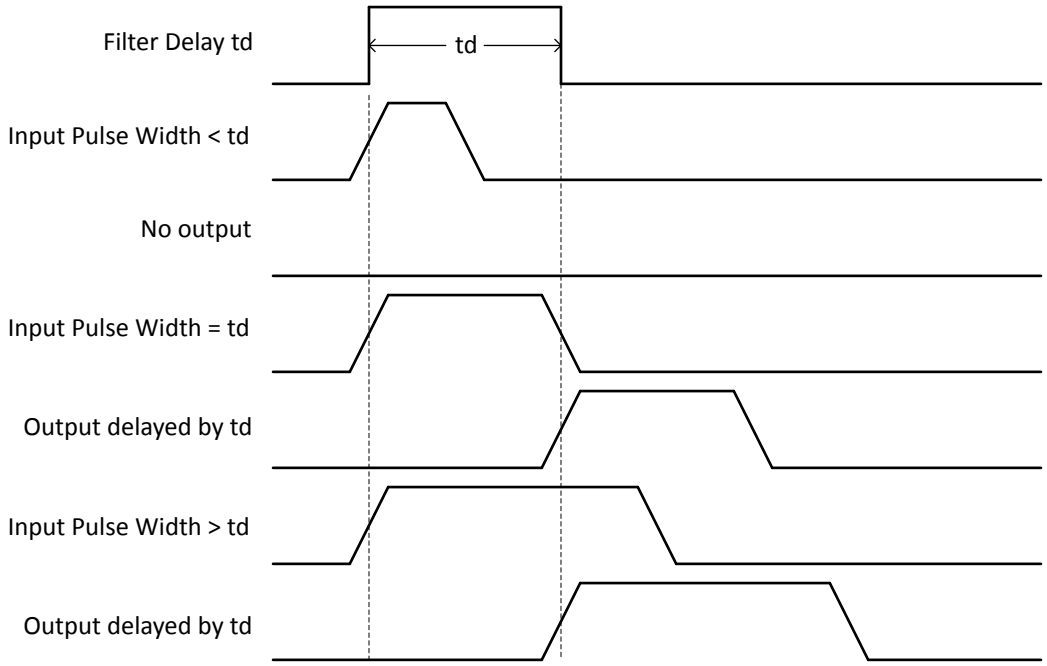

Figure 3.7. Input Noise Filter Functionality

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction Operating Temperature	T_J	—	—	150	°C
Ambient Operating Temperature[1]	T_A	–40	25	125	°C
Supply Voltage	VDD1, VDD2	2.25	—	5.5	V

Note:

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 4.2. Electrical Characteristics

T_A = –40 to 125°C; VDD1, VDD2 as specified in Recommended Operating Conditions Table above.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDD_{UV+}	VDD1, VDD2 rising	2.14	2.18	2.25	V
VDD Undervoltage Threshold	VDD_{UV-}	VDD1, VDD2 falling	2.01	2.05	2.10	V
VDD Undervoltage Hysteresis	VDD_{HYS}		105	131	150	mV
Input Hysteresis	V_{HYS}		0.15*VDDx	—	—	V
High Level Input Voltage	V_{IH}		0.7*VDDx	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3*VDDx	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	VDD1, VDD2–0.4	—	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	—	0.4	V
Output Impedance	Z_O		—	50	—	Ω

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Table 4.3. Electrical Characteristics

VDD1 = 5.0 V ±10%, VDD2 = 5.0 V ±10%, T_A = –40 to 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.70	0.85	
IDD2		VI = 0(Bx), 1(Ex)	—	2.19	2.76	mA
IDD1		VI = 1(Bx), 0(Ex)		2.47	3.03	
IDD2		VI = 1(Bx), 0(Ex)		2.29	2.83	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	1.58	1.93	mA
IDD2				2.26	2.82	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	1.59	1.93	
IDD2				3.58	4.28	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	1.59	1.93	
IDD2				14.85	19.30	
Si86S631Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.28	1.56	
IDD2		VI = 0(Bx), 1(Ex)	—	1.84	2.27	mA
IDD1		VI = 1(Bx), 0(Ex)		2.54	3.00	
IDD2		VI = 1(Bx), 0(Ex)		2.25	3.02	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	1.92	2.29	mA
IDD2				2.20	2.66	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.36	2.82	
IDD2				3.02	3.73	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	6.11	7.78	
IDD2				10.53	13.65	
Si86S640Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.84	1.02	
IDD2		VI = 0(Bx), 1(Ex)	—	2.83	3.56	mA
IDD1		VI = 1(Bx), 0(Ex)		3.24	3.95	
IDD2		VI = 1(Bx), 0(Ex)		2.96	3.64	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	2.04	2.48	mA
IDD2				2.93	3.65	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.07	2.48	
IDD2				4.59	5.79	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.07	2.48	
IDD2				19.77	25.83	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.32	1.68	
IDD2		VI = 0(Bx), 1(Ex)	—	2.29	2.96	mA
IDD1		VI = 1(Bx), 0(Ex)		3.17	4.04	
IDD2		VI = 1(Bx), 0(Ex)		3.00	3.79	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.26	2.87	
IDD2				2.66	3.40	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.80	3.40	mA
IDD2				4.06	5.00	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.59	8.41	
IDD2				15.45	20.03	
Si86S642Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.86	2.41	
IDD2		VI = 0(Bx), 1(Ex)	—	1.89	2.44	mA
IDD1		VI = 1(Bx), 0(Ex)		3.12	3.97	
IDD2		VI = 1(Bx), 0(Ex)		3.12	3.97	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.53	3.23	
IDD2				2.55	3.26	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.43	4.30	mA
IDD2				3.43	4.33	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	11.02	14.32	
IDD2				11.02	14.35	
Si86S640Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.08	1.23	
IDD2		VI = 0(Bx), 1(Ex)	—	3.05	3.81	mA
IDD1		VI = 1(Bx), 0(Ex)		3.53	4.13	
IDD2		VI = 1(Bx), 0(Ex)		3.18	3.89	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.31	2.67	
IDD2				3.15	3.91	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.07	2.67	mA
IDD2				4.59	6.05	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.07	2.67	
IDD2				19.77	26.09	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.55	1.87	
IDD2		VI = 0(Bx), 1(Ex)	—	2.52	3.14	mA
IDD1		VI = 1(Bx), 0(Ex)		3.42	4.11	
IDD2		VI = 1(Bx), 0(Ex)		3.32	3.94	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.51	3.01	
IDD2				2.90	3.56	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.80	3.54	mA
IDD2				4.06	5.16	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.59	8.55	
IDD2				15.45	20.19	
Si86S642Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		2.12	2.57	
IDD2		VI = 0(Bx), 1(Ex)	—	2.14	2.60	mA
IDD1		VI = 0(Bx), 1(Ex)		3.41	4.07	
IDD2		VI = 0(Bx), 1(Ex)		3.42	4.09	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.80	3.36	
IDD2				2.81	3.37	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.43	4.44	mA
IDD2				3.43	4.44	
VDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	11.02	14.46	
IDD2				11.02	14.46	
Si86SL40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.79	0.96	
IDD2		VI = 0(Bx), 1(Ex)	—	2.07	2.63	mA
IDD1		VI = 0(Bx), 1(Ex)		2.89	3.54	
IDD2		VI = 0(Bx), 1(Ex)		2.13	2.67	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.85	2.24	
IDD2				2.14	2.71	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.87	2.24	mA
IDD2				3.74	4.85	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.87	2.24	
IDD2				18.62	24.49	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SL41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.07	1.35	
IDD2		VI = 0(Bx), 1(Ex)	—	1.69	2.18	mA
IDD1		VI = 0(Bx), 1(Ex)		2.63	3.25	
IDD2		VI = 0(Bx), 1(Ex)		2.25	2.83	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.87	2.31	mA
IDD2				1.99	2.53	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.44	2.84	
IDD2				3.37	4.13	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.16	7.76	
IDD2				14.53	18.87	
Si86SL42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.46	1.85	
IDD2		VI = 0(Bx), 1(Ex)	—	1.48	1.86	mA
IDD1		VI = 1(Bx), 0(Ex)		2.54	3.15	
IDD2		VI = 1(Bx), 0(Ex)		2.56	3.17	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.04	2.54	mA
IDD2				2.04	2.53	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.91	3.61	
IDD2				2.91	3.61	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	10.35	13.43	
IDD2				10.35	13.43	
Si86SM40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.51	1.85	
IDD2		VI = 0(Bx), 1(Ex)		3.50	4.47	
IDD1		VI = 1(Bx), 0(Ex)	—	3.95	4.89	mA
IDD2		VI = 1(Bx), 0(Ex)		3.63	4.57	
IDD1		SMb = 0 (sleep mode)		0.78	0.95	
IDD2		SMb = 0 (sleep mode)		1.19	1.68	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.73	3.36	mA
IDD2				3.59	4.56	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.67	3.36	
IDD2				5.53	6.70	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.67	3.36	
IDD2				20.30	26.74	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SM41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.07	2.62	
IDD2		VI = 0(Bx), 1(Ex)		2.93	3.73	
IDD1		VI = 1(Bx), 0(Ex)	—	3.91	4.92	mA
IDD2		VI = 1(Bx), 0(Ex)		3.64	4.53	
IDD1		SMb = 0 (sleep mode)		0.77	0.97	
IDD2		SMb = 0 (sleep mode)		1.20	1.53	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	3.01	3.78	
IDD2				3.30	4.16	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.40	4.31	mA
IDD2				4.99	5.76	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	7.20	9.32	
IDD2				15.97	20.79	
Si86SM42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.62	3.36	
IDD2		VI = 0(Bx), 1(Ex)		2.52	3.23	
IDD1		VI = 1(Bx), 0(Ex)	—	3.89	4.92	mA
IDD2		VI = 1(Bx), 0(Ex)		3.78	4.77	
IDD1		SMb = 0 (sleep mode)		0.77	0.98	
IDD2		SMb = 0 (sleep mode)		1.20	1.54	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	3.29	4.18	
IDD2				3.17	4.02	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.03	5.25	mA
IDD2				4.36	5.09	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	11.62	15.27	
IDD2				11.55	15.11	
Si86SS41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.37	1.76	
IDD2		VI = 0(Bx), 1(Ex)	—	2.43	3.15	mA
IDD1		VI = 1(Bx), 0(Ex)		3.12	4.01	
IDD2		VI = 1(Bx), 0(Ex)		3.13	3.95	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.26	2.88	mA
IDD2				2.80	3.58	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb =0	—	2.80	3.41	mA
IDD2				4.06	4.65	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.39	2.88	mA
IDD2				4.06	4.65	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 0	—	6.59 11.25	8.42 14.67	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.39 11.25	2.88 14.67	mA
Si86SQ44Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex), DIR = 1		3.82	4.85	
IDD2		VI = 0(Bx), 1(Ex), DIR = 1		3.47	4.45	
IDD1		VI = 1(Bx), 0(Ex), DIR = 1		6.87	8.51	
IDD2		VI = 1(Bx), 0(Ex), DIR = 1	—	3.60	4.51	mA
IDD1		VI = 0(Bx), 1(Ex), DIR = 0		3.05	3.91	
IDD2		VI = 0(Bx), 1(Ex), DIR = 0		3.76	4.83	
IDD1		VI = 1(Bx), 0(Ex), DIR = 0		3.19	3.99	
IDD2		VI = 1(Bx), 0(Ex), DIR = 0		6.81	8.48	
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.51 3.55	6.84 4.49	mA
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	2.40 3.89	3.18 4.97	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.30 5.34	6.84 6.63	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	5.53 5.17	6.75 6.52	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.14 20.52	6.84 26.67	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	20.58 5.17	26.79 6.52	mA
Si86S660Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.96	1.16	
IDD2		VI = 0(Bx), 1(Ex)	—	4.05	5.09	mA
IDD1		VI = 1(Bx), 0(Ex)		4.55	5.56	
IDD2		VI = 1(Bx), 0(Ex)		4.24	5.23	
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.75 4.21	3.33 5.35	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.77 6.48	3.33 8.56	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.77 28.35	3.33 37.43	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S661Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.53	1.87	
IDD2		VI = 0(Bx), 1(Ex)	—	3.51	4.47	mA
IDD1		VI = 1(Bx), 0(Ex)		4.61	5.52	
IDD2		VI = 1(Bx), 0(Ex)		4.28	5.31	
IDD1		All Inputs = 500 kHz Square Wave, CI = 15 pF on All Outputs	—	3.09	3.70	mA
IDD2				3.93	4.93	
IDD1		All Inputs = 5 MHz Square Wave, CI = 15 pF on All Outputs	—	3.49	4.24	mA
IDD2				5.96	7.60	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	7.13	9.05	mA
IDD2				24.19	31.66	
Si86S662Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.99	2.38	
IDD2		VI = 0(Bx), 1(Ex)	—	2.93	3.66	mA
IDD1		VI = 1(Bx), 0(Ex)		4.47	5.24	
IDD2		VI = 1(Bx), 0(Ex)		4.27	5.13	
IDD1		All Inputs = 500 kHz Square Wave, CI = 15 pF on All Outputs	—	3.25	3.83	mA
IDD2				3.62	4.41	
IDD1		All Inputs = 5 MHz Square Wave, CI = 15 pF on All Outputs	—	4.11	4.89	mA
IDD2				5.34	6.55	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	11.39	15.52	mA
IDD2				19.92	25.79	
Si86S663Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.59	3.40	
IDD2		VI = 0(Bx), 1(Ex)	—	2.59	3.40	mA
IDD1		VI = 1(Bx), 0(Ex)		4.55	5.79	
IDD2		VI = 1(Bx), 0(Ex)		4.55	5.79	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	3.56	4.53	mA
IDD2				3.56	4.53	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.73	6.13	mA
IDD2				4.73	6.13	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	15.66	20.57	mA
IDD2				15.66	20.57	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Data Rate Si86Sx (with 36 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse Width Si86S6x (with 36 ns deglitch)		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	7	9	14	ns
Pulse Width Distortion (no deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	2	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	0.8	2	ns
Propagation Delay (36 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	32	36	42	ns
Pulse Width Distortion (36 ns deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	2	ns
Propagation Delay Skew (36 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (36 ns deglitch)	t_{PSK}		—	1.5	4	ns
Propagation Delay Skew (Si86SLx, low power mode)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	8.5	11.5	18	ns
Pulse Width Distortion (Si86SLx, low power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	7	ns
Propagation Delay Skew (Si86SLx, low power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (Si86SLx, low power mode)	t_{PSK}		—	1.5	7	ns
Direction Transition Delay (Si86SQx)	t_{DIR}		36	55	80	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity Si86Sx (no deglitch) Si86Sx (with 36 ns deglitch)	CMTI	See Figure 4.4 Common-Mode Transient Immunity Test Circuit on page 47. VI = VDD or 0 V VCM = ±1500 V	100 150	— —	— —	kV/µs
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 45.	—	12	20	ns
SMb to Sleep Mode Delay (Si86SMx)	t_{SM}	See Figure 4.3 SMb Timing on page 46.	—	14	23	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 45.	—	11	17	ns
SMb to Wake-Up from Sleep Mode	t_{WU}	See Figure 4.3 SMb Timing on page 46.	—	700	1500	ns
Input power loss to valid default output	t_{SD}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	8.0	12	ns
Start-up Time	t_{START}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	—	300	µs
Input Leakage Current	I_L		—	—	±8	µA
EN, SMb, MCSb, DIR Input Current	I_{ENH}, I_{ENL}	$V_{ENx} = V_{IH}$ or V_{IL}	—	—	90	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

Table 4.4. Electrical Characteristics

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.66	0.81	
IDD2		VI = 0(Bx), 1(Ex)	—	2.16	2.72	mA
IDD1		VI = 1(Bx), 0(Ex)		2.43	2.98	
IDD2		VI = 1(Bx), 0(Ex)		2.25	2.78	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	1.54	1.87	mA
IDD2				2.21	2.76	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	1.54	1.87	mA
IDD2				3.06	3.77	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	1.54	1.87	mA
IDD2				10.46	13.54	
Si86S631Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.25	1.51	
IDD2		VI = 0(Bx), 1(Ex)	—	1.8	2.22	mA
IDD1		VI = 1(Bx), 0(Ex)		2.5	2.95	
IDD2		VI = 1(Bx), 0(Ex)		2.48	2.97	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	1.88	2.23	mA
IDD2				2.15	2.6	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.15	2.54	mA
IDD2				2.66	3.21	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	4.62	5.49	mA
IDD2				7.59	9.13	
Si86S640Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.81	0.97	
IDD2		VI = 0(Bx), 1(Ex)	—	2.8	3.51	mA
IDD1		VI = 1(Bx), 0(Ex)		3.2	3.89	
IDD2		VI = 1(Bx), 0(Ex)		2.92	3.64	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	2	2.4	mA
IDD2				2.88	3.57	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.01	2.40	mA
IDD2				3.92	4.92	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	2.01	2.40	mA
IDD2				13.79	17.94	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.28	1.64	
IDD2		VI = 0(Bx), 1(Ex)	—	2.26	2.91	mA
IDD1		VI = 1(Bx), 0(Ex)		3.13	3.97	
IDD2		VI = 1(Bx), 0(Ex)		2.96	3.73	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.22	2.8	mA
IDD2				2.61	3.33	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.59	3.14	mA
IDD2				3.54	4.34	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	5.06	6.39	mA
IDD2				10.95	14.11	
Si86S642Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.83	2.37	
IDD2		VI = 0(Bx), 1(Ex)	—	1.85	2.39	mA
IDD1		VI = 1(Bx), 0(Ex)		3.08	3.91	
IDD2		VI = 1(Bx), 0(Ex)		3.08	3.91	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.48	3.15	mA
IDD2				2.5	3.19	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.07	3.82	mA
IDD2				3.07	3.86	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	8.00	10.34	mA
IDD2				8.00	10.38	
Si86S640Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.04	1.18	
IDD2		VI = 0(Bx), 1(Ex)	—	3.01	3.76	mA
IDD1		VI = 1(Bx), 0(Ex)		3.49	4.06	
IDD2		VI = 1(Bx), 0(Ex)		3.14	3.85	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.26	2.61	mA
IDD2				3.1	3.83	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.01	2.61	mA
IDD2				3.92	5.18	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.01	2.61	mA
IDD2				13.79	18.20	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.51	1.83	
IDD2		VI = 0(Bx), 1(Ex)	—	2.49	3.09	mA
IDD1		VI = 1(Bx), 0(Ex)		3.38	4.05	
IDD2		VI = 1(Bx), 0(Ex)		3.19	3.88	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.46	2.94	mA
IDD2				2.85	3.5	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.59	3.28	mA
IDD2				3.54	4.51	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	5.06	6.53	mA
IDD2				10.95	14.28	
Si86S642Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		2.09	2.52	
IDD2		VI = 0(Bx), 1(Ex)	—	2.11	2.55	mA
IDD1		VI = 1(Bx), 0(Ex)		3.37	4.02	
IDD2		VI = 1(Bx), 0(Ex)		3.38	4.03	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.75	3.29	mA
IDD2				2.76	3.3	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.07	3.97	mA
IDD2				3.07	3.97	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	8.00	10.49	mA
IDD2				8.00	10.49	
Si86SL40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.76	0.91	
IDD2		VI = 0(Bx), 1(Ex)	—	2.04	2.59	mA
IDD1		VI = 1(Bx), 0(Ex)		2.85	3.47	
IDD2		VI = 1(Bx), 0(Ex)		2.09	2.62	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.8	2.17	mA
IDD2				2.08	2.63	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.81	2.17	mA
IDD2				3.08	3.98	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.81	2.17	mA
IDD2				12.96	17.00	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SL41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.04	1.3	
IDD2		VI = 0(Bx), 1(Ex)	—	1.65	2.13	mA
IDD1		VI = 1(Bx), 0(Ex)		2.59	3.2	
IDD2		VI = 1(Bx), 0(Ex)		2.21	2.78	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.82	2.25	mA
IDD2				1.94	2.46	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.22	2.59	mA
IDD2				2.86	3.47	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.69	5.84	mA
IDD2				10.27	13.24	
Si86SL42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.43	1.81	
IDD2		VI = 0(Bx), 1(Ex)	—	1.44	1.82	mA
IDD1		VI = 1(Bx), 0(Ex)		2.5	3.08	
IDD2		VI = 1(Bx), 0(Ex)		2.52	3.11	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.99	2.47	mA
IDD2				1.99	2.47	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.54	3.14	mA
IDD2				2.54	3.14	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	7.48	9.66	mA
IDD2				7.48	9.66	
Si86SM40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.48	1.81	
IDD2		VI = 0(Bx), 1(Ex)		3.46	4.41	
IDD1		VI = 1(Bx), 0(Ex)	—	3.91	4.81	mA
IDD2		VI = 1(Bx), 0(Ex)		3.59	4.5	
IDD1		SMb = 0 (sleep mode)		0.73	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.61	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.69	3.29	mA
IDD2				3.54	4.48	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.61	3.29	mA
IDD2				4.70	5.83	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.61	3.29	mA
IDD2				14.31	18.85	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SM41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.03	2.57	
IDD2		VI = 0(Bx), 1(Ex)		2.9	3.68	
IDD1		VI = 1(Bx), 0(Ex)	—	3.86	4.85	mA
IDD2		VI = 1(Bx), 0(Ex)		3.6	3.68	
IDD1		SMb = 0 (sleep mode)		0.72	0.90	
IDD2		SMb = 0 (sleep mode)		1.17	1.47	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.96	3.71	mA
IDD2				3.25	4.08	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.19	4.05	mA
IDD2				4.32	5.09	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	5.65	7.30	mA
IDD2				11.47	14.86	
Si86SM42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.58	3.31	
IDD2		VI = 0(Bx), 1(Ex)		2.49	3.19	
IDD1		VI = 1(Bx), 0(Ex)	—	3.85	4.85	mA
IDD2		VI = 1(Bx), 0(Ex)		3.74	4.71	
IDD1		SMb = 0 (sleep mode)		0.72	0.91	
IDD2		SMb = 0 (sleep mode)		1.16	1.49	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	3.23	4.09	mA
IDD2				3.12	3.95	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.66	4.76	mA
IDD2				3.84	4.62	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	8.60	11.28	mA
IDD2				8.52	11.14	
Si86SS41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.31	1.69	
IDD2		VI = 0(Bx), 1(Ex)	—	3.09	3.1	mA
IDD1		VI = 1(Bx), 0(Ex)		3.08	3.95	
IDD2		VI = 1(Bx), 0(Ex)		3.09	3.9	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.22	2.81	mA
IDD2				2.75	3.51	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 0	—	2.49	3.04	mA
IDD2				3.31	3.98	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.30	2.79	mA
IDD2				3.31	3.98	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 0	—	4.36	5.51	mA
IDD2				6.86	8.93	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.30	2.79	mA
IDD2				6.86	8.93	
Si86SQ44Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex), DIR = 1		3.78	4.08	
IDD2		VI = 0(Bx), 1(Ex), DIR = 1		3.44	4.41	
IDD1		VI = 1(Bx), 0(Ex), DIR = 1		6.81	8.42	
IDD2		VI = 1(Bx), 0(Ex), DIR = 1	—	3.57	4.47	mA
IDD1		VI = 0(Bx), 1(Ex), DIR = 0		3.00	3.84	
IDD2		VI = 0(Bx), 1(Ex), DIR = 0		3.72	4.78	
IDD1		VI = 1(Bx), 0(Ex), DIR = 0		3.13	3.92	
IDD2		VI = 1(Bx), 0(Ex), DIR = 0		6.75	7.46	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.41	6.71	mA
IDD2				3.51	4.44	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	2.57	3.36	mA
IDD2				3.82	4.88	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.20	6.71	mA
IDD2				4.66	5.79	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	4.84	5.73	mA
IDD2				5.08	6.45	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.14	6.71	mA
IDD2				14.53	18.81	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	14.67	18.75	mA
IDD2				5.08	6.45	
Si86S660Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.93	1.11	
IDD2		VI = 0(Bx), 1(Ex)	—	4.01	5.03	mA
IDD1		VI = 1(Bx), 0(Ex)		4.5	5.48	
IDD2		VI = 1(Bx), 0(Ex)		4.2	5.18	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.71	3.27	mA
IDD2				4.14	5.14	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.70	3.27	mA
IDD2				5.53	7.16	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.70	3.27	mA
IDD2				20.33	26.70	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S661Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.50	1.82	
IDD2		VI = 0(Bx), 1(Ex)	—	3.48	4.42	mA
IDD1		VI = 1(Bx), 0(Ex)		4.56	5.44	
IDD2		VI = 1(Bx), 0(Ex)		4.24	5.25	
IDD1		All Inputs = 500 kHz Square Wave, CI = 15 pF on All Outputs	—	3.04	3.62	mA
IDD2				3.87	4.85	
IDD1		All Inputs = 5 MHz Square Wave, CI = 15 pF on All Outputs	—	3.27	3.96	mA
IDD2				5.16	6.53	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	5.74	7.21	mA
IDD2				17.49	22.82	
Si86S662Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.95	2.34	
IDD2		VI = 0(Bx), 1(Ex)	—	2.89	3.61	mA
IDD1		VI = 1(Bx), 0(Ex)		4.42	5.17	
IDD2		VI = 1(Bx), 0(Ex)		4.23	5.07	
IDD1		All Inputs = 500 kHz Square Wave, CI = 15 pF on All Outputs	—	3.20	3.75	mA
IDD2				3.57	4.35	
IDD1		All Inputs = 5 MHz Square Wave, CI = 15 pF on All Outputs	—	3.74	4.42	mA
IDD2				4.68	5.69	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	8.67	10.94	mA
IDD2				14.55	18.73	
Si86S663Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.53	3.35	
IDD2		VI = 0(Bx), 1(Ex)	—	2.53	3.35	mA
IDD1		VI = 1(Bx), 0(Ex)		4.47	5.71	
IDD2		VI = 1(Bx), 0(Ex)		4.47	5.71	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	3.49	4.48	mA
IDD2				3.49	4.48	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	4.21	5.49	mA
IDD2				4.21	5.49	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	11.62	15.26	mA
IDD2				11.62	15.26	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Data Rate Si86Sx (with 36 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse Width Si86S6x (with 36 ns deglitch)		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	6	9	15	ns
Pulse Width Distortion (no deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	3	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	0.9	3	ns
Propagation Delay (36 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	31	36	42	ns
Pulse Width Distortion (36 ns deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	3	ns
Propagation Delay Skew (36 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (36 ns deglitch)	t_{PSK}		—	1.5	3.5	ns
Propagation Delay (Si86SLx low-power mode)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	7	12	18	ns
Pulse Width Distortion (Si86SLx, low-power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	7	ns
Propagation Delay Skew (Si86SLx, low-power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (Si86SLx, low-power mode)	t_{PSK}		—	1.5	5.5	ns
Direction Transition Delay (Si86SQx)	t_{DIR}		37	57	83	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity		See Figure 4.4 Common-Mode Transient Immunity Test Circuit on page 47				
Si86Sx (no deglitch)	CMTI	VI = VDD or 0 V	100	—	—	kV/µs
Si86Sx (with 36 ns deglitch)		VCM = ±1500 V	150	—	—	
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 45	—	17	27	ns
SMb to Sleep Mode Delay (Si86SMx)	t_{SM}	See Figure 4.3 SMb Timing on page 46	—	15	25	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 45	—	12	19	ns
SMb to Wake-Up from Sleep Mode	t_{WU}	See Figure 4.3 SMb Timing on page 46	—	1100	1800	ns
Input power loss to valid default output	t_{SD}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	8.0	12	ns
Start-up Time	t_{START}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	—	300	µs
Input Leakage Current	I_L		—	—	±6	µA
EN, SMb, MCSb, DIR Input Current	I_{ENH}, I_{ENL}	VENx = VIH or VIL	—	—	60	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

Table 4.5. Electrical Characteristics

VDD1 = 2.5 V ±10%, VDD2 = 2.5 V ±10%, T_A = –40 to 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S630Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.64	0.79	
IDD2		VI = 0(Bx), 1(Ex)	—	2.14	2.7	mA
IDD1		VI = 1(Bx), 0(Ex)		2.41	2.96	
IDD2		VI = 1(Bx), 0(Ex)		2.23	2.76	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.52	1.85	mA
IDD2				2.19	2.74	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.51	1.85	mA
IDD2				2.82	3.49	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.51	1.85	mA
IDD2				8.44	10.91	
Si86S631Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.23	1.5	
IDD2		VI = 0(Bx), 1(Ex)	—	1.78	2.19	mA
IDD1		VI = 1(Bx), 0(Ex)		2.48	2.93	
IDD2		VI = 1(Bx), 0(Ex)		2.46	2.95	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.85	2.21	mA
IDD2				2.13	2.58	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.05	2.46	mA
IDD2				2.49	3.08	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.00	4.93	mA
IDD2				6.60	8.03	
Si86S640Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.79	0.96	
IDD2		VI = 0(Bx), 1(Ex)	—	2.77	3.49	mA
IDD1		VI = 1(Bx), 0(Ex)		3.17	3.86	
IDD2		VI = 1(Bx), 0(Ex)		2.9	3.58	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.97	2.38	mA
IDD2				2.85	3.54	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.98	2.38	mA
IDD2				3.62	4.50	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.98	2.38	mA
IDD2				11.11	14.39	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.27	1.62	
IDD2		VI = 0(Bx), 1(Ex)	—	2.23	2.89	mA
IDD1		VI = 1(Bx), 0(Ex)		3.1	3.95	
IDD2		VI = 1(Bx), 0(Ex)		2.93	3.72	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.19	2.77	mA
IDD2				2.59	3.3	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.49	3.02	mA
IDD2				3.31	4.05	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.36	5.49	mA
IDD2				8.93	11.47	
Si86S642Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.81	2.35	
IDD2		VI = 0(Bx), 1(Ex)	—	1.83	2.37	mA
IDD1		VI = 1(Bx), 0(Ex)		3.06	3.88	
IDD2		VI = 1(Bx), 0(Ex)		3.06	3.88	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.45	3.12	mA
IDD2				2.45	3.12	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.90	3.65	mA
IDD2				2.90	3.65	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.64	8.60	mA
IDD2				6.64	8.60	
Si86S640Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.02	1.17	
IDD2		VI = 0(Bx), 1(Ex)	—	2.99	3.74	mA
IDD1		VI = 1(Bx), 0(Ex)		3.46	4.03	
IDD2		VI = 1(Bx), 0(Ex)		3.12	3.82	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.24	2.58	mA
IDD2				3.07	3.8	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.98	2.58	mA
IDD2				3.62	4.80	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.98	2.58	mA
IDD2				11.11	14.69	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S641Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		1.49	1.81	
IDD2		VI = 0(Bx), 1(Ex)	—	2.46	3.07	mA
IDD1		VI = 1(Bx), 0(Ex)		3.36	4.03	
IDD2		VI = 1(Bx), 0(Ex)		3.16	3.86	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.44	2.92	mA
IDD2				2.82	3.48	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.49	3.17	mA
IDD2				3.31	4.23	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.36	5.64	mA
IDD2				8.93	11.65	
Si86S642Fx, Hx						
IDD1		VI = 0(Bx), 1(Ex)		2.07	2.51	
IDD2		VI = 0(Bx), 1(Ex)	—	2.09	2.53	mA
IDD1		VI = 1(Bx), 0(Ex)		3.35	3.99	
IDD2		VI = 1(Bx), 0(Ex)		3.35	4.01	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.72	3.26	mA
IDD2				2.73	3.27	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.90	3.77	mA
IDD2				2.90	3.77	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.64	8.72	mA
IDD2				6.64	8.72	
Si86SL40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.74	0.89	
IDD2		VI = 0(Bx), 1(Ex)	—	2.02	2.57	mA
IDD1		VI = 1(Bx), 0(Ex)		2.83	3.45	
IDD2		VI = 1(Bx), 0(Ex)		2.08	2.6	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.78	2.15	mA
IDD2				2.06	2.6	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.87	2.24	mA
IDD2				3.74	4.85	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	1.87	2.24	mA
IDD2				18.62	24.49	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SL41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.02	1.29	
IDD2		VI = 0(Bx), 1(Ex)	—	1.63	2.11	mA
IDD1		VI = 1(Bx), 0(Ex)		2.57	3.17	
IDD2		VI = 1(Bx), 0(Ex)		2.19	2.76	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.8	2.22	mA
IDD2				1.92	2.44	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.44	2.84	mA
IDD2				3.37	4.13	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	6.16	7.76	mA
IDD2				14.53	18.87	
Si86SL42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.41	1.79	
IDD2		VI = 0(Bx), 1(Ex)	—	1.42	1.8	mA
IDD1		VI = 1(Bx), 0(Ex)		2.48	3.07	
IDD2		VI = 1(Bx), 0(Ex)		2.49	3.08	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	1.96	2.44	mA
IDD2				1.97	2.44	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.91	3.61	mA
IDD2				2.91	3.61	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	10.35	13.43	mA
IDD2				10.35	13.43	
Si86SM40Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.45	1.78	
IDD2		VI = 0(Bx), 1(Ex)		3.44	4.38	
IDD1		VI = 1(Bx), 0(Ex)	—	3.87	4.78	mA
IDD2		VI = 1(Bx), 0(Ex)		3.57	4.47	
IDD1		SMb = 0 (sleep mode)		0.70	0.86	
IDD2		SMb = 0 (sleep mode)		1.14	1.58	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.66	3.26	mA
IDD2				3.51	4.44	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.57	3.26	mA
IDD2				4.32	5.44	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.57	3.26	mA
IDD2				11.62	15.33	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86SM41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.01	2.55	
IDD2		VI = 0(Bx), 1(Ex)		2.87	3.66	
IDD1		VI = 1(Bx), 0(Ex)	—	3.84	4.82	mA
IDD2		VI = 1(Bx), 0(Ex)		3.57	4.45	
IDD1		SMb = 0 (sleep mode)		0.69	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.46	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.93	3.67	mA
IDD2				3.23	4.06	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.08	3.92	mA
IDD2				4.01	4.81	
IDD1		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	4.95	6.39	mA
IDD2				9.44	12.23	
Si86SM42Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.56	3.29	
IDD2		VI = 0(Bx), 1(Ex)		2.47	3.16	
IDD1		VI = 1(Bx), 0(Ex)	—	3.82	4.83	mA
IDD2		VI = 1(Bx), 0(Ex)		3.72	4.68	
IDD1		SMb = 0 (sleep mode)		0.69	0.88	
IDD2		SMb = 0 (sleep mode)		1.15	1.48	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	3.2	4.06	mA
IDD2				3.1	3.92	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	3.49	4.56	mA
IDD2				3.60	4.42	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	7.23	9.51	mA
IDD2				7.16	9.37	
Si86SS41Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.29	1.66	
IDD2		VI = 0(Bx), 1(Ex)	—	2.38	3.08	mA
IDD1		VI = 1(Bx), 0(Ex)		3.06	3.93	
IDD2		VI = 1(Bx), 0(Ex)		3.07	3.88	
IDD1		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.21	2.79	mA
IDD2				2.73	3.48	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 0	—	2.49	3.04	mA
IDD2				3.31	3.98	
IDD1		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.30	2.79	mA
IDD2				3.31	3.98	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 0	—	4.36 6.86	5.51 8.93	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, MCSb = 1	—	2.30 6.86	2.79 8.93	mA
Si86SQ44Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex), DIR = 1		3.76	4.77	
IDD2		VI = 0(Bx), 1(Ex), DIR = 1		3.42	4.39	
IDD1		VI = 1(Bx), 0(Ex), DIR = 1		6.75	8.36	
IDD2		VI = 1(Bx), 0(Ex), DIR = 1	—	3.55	4.45	mA
IDD1		VI = 0(Bx), 1(Ex), DIR = 0		2.97	3.81	
IDD2		VI = 0(Bx), 1(Ex), DIR = 0		3.70	4.76	
IDD1		VI = 1(Bx), 0(Ex), DIR = 0		3.10	3.88	
IDD2		VI = 1(Bx), 0(Ex), DIR = 0		6.70	8.33	
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.34 3.49	6.63 4.42	mA
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	2.64 3.77	3.45 4.83	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.14 4.35	6.63 5.42	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 0	—	4.53 5.02	5.32 6.42	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs, DIR = 1	—	5.14 11.84	6.63 15.31	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs, DIR = 0	—	12.03 5.02	15.21 6.42	mA
Si86S660Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.91	1.10	
IDD2		VI = 0(Bx), 1(Ex)	—	3.99	5.01	mA
IDD1		VI = 1(Bx), 0(Ex)		4.46	5.45	
IDD2		VI = 1(Bx), 0(Ex)		4.18	5.16	
IDD1 IDD2		All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs	—	2.68 4.1	3.23 5.1	mA
IDD1 IDD2		All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.67 5.10	3.23 6.60	mA
IDD1 IDD2		All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs	—	2.67 16.34	3.23 21.44	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S661Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.48	1.80	
IDD2		VI = 0(Bx), 1(Ex)	—	3.46	4.40	mA
IDD1		VI = 1(Bx), 0(Ex)		4.53	5.41	
IDD2		VI = 1(Bx), 0(Ex)		4.22	5.23	
IDD1		All Inputs = 500 kHz Square Wave, CI = 15 pF on All Outputs	—	3.00	3.59	mA
IDD2				3.84	4.82	
IDD1		All Inputs = 5 MHz Square Wave, CI = 15 pF on All Outputs	—	3.17	3.80	mA
IDD2				4.79	6.07	
IDD1		All Inputs = 50 MHz Square Wave, CI = 15 pF on All Outputs	—	5.04	6.31	mA
IDD2				14.16	18.43	
Si86S662Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.93	2.32	
IDD2		VI = 0(Bx), 1(Ex)	—	2.88	3.59	mA
IDD1		VI = 1(Bx), 0(Ex)		4.39	5.14	
IDD2		VI = 1(Bx), 0(Ex)		4.21	5.05	
IDD1		All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs	—	3.17	3.73	mA
IDD2				3.54	4.32	
IDD1		All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs	—	3.58	4.23	mA
IDD2				4.38	5.32	
IDD1		All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs	—	7.32	9.18	mA
IDD2				11.88	15.21	
Si86S663Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		2.5	3.31	
IDD2		VI = 0(Bx), 1(Ex)	—	2.5	3.31	mA
IDD1		VI = 1(Bx), 0(Ex)		4.42	5.66	
IDD2		VI = 1(Bx), 0(Ex)		4.42	5.66	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	3.47	4.42	mA
IDD2				3.46	4.42	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	3.98	5.17	mA
IDD2				3.98	5.17	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	9.60	12.59	mA
IDD2				9.60	12.59	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Data Rate Si86Sx (with 36 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)		Minimum pulse width guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse Width Si86S6X (with 36 ns deglitch)		Minimum pulse width guaranteed to be transmitted to output.	100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	8	11	18	ns
Pulse Width Distortion (no deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	2	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	1.1	3	ns
Propagation Delay (36 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	33	39	45	ns
Pulse Width Distortion (36 ns deglitch) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	2	ns
Propagation Delay Skew (36 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (36 ns deglitch)	t_{PSK}		—	1.7	3	ns
Propagation Delay (Si86SLx, low-power mode)	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 46.	9	14	21	ns
Pulse Width Distortion (Si86SLx, low-power mode) $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 46.	—	—	7	ns
Propagation Delay Skew (Si86SLx, low-power mode)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (Si86SLx, low-power mode)	t_{PSK}		—	1.6	6	ns
Direction Transition Delay (Si86SQx)	t_{DIR}	.	40	64	95	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.2 Propagation Delay Timing on page 46.	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity Si86Sx (no deglitch) Si86Sx (with 36 ns deglitch)	CMTI	See Figure 4.4 Common-Mode Transient Immunity Test Circuit on page 47 VI = VDD or 0 V VCM = ±1500 V	100 150	— —	— —	kV/µs
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 45	—	29	44	ns
SMb to Sleep Mode Delay (Si86SMx)	t_{SM}	See Figure 4.3 SMb Timing on page 46	—	19	30	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 45	—	16	27	ns
SMb to Wake-Up from Sleep Mode	t_{WU}	See Figure 4.3 SMb Timing on page 46	—	1400	2100	ns
Input power loss to valid default output	t_{SD}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	8.0	12	ns
Start-up Time	t_{START}	See Figure 3.2 Device Behavior during Normal Operation on page 12.	—	—	300	µs
Input Leakage Current	I_L		—	—	±6	µA
EN, SMb, MCSb, DIR Input Current	I_{ENH}, I_{ENL}	VENx = V_{IH} or V_{IL}	—	—	45	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The OTP initialization time is included in the 300 µs specification.

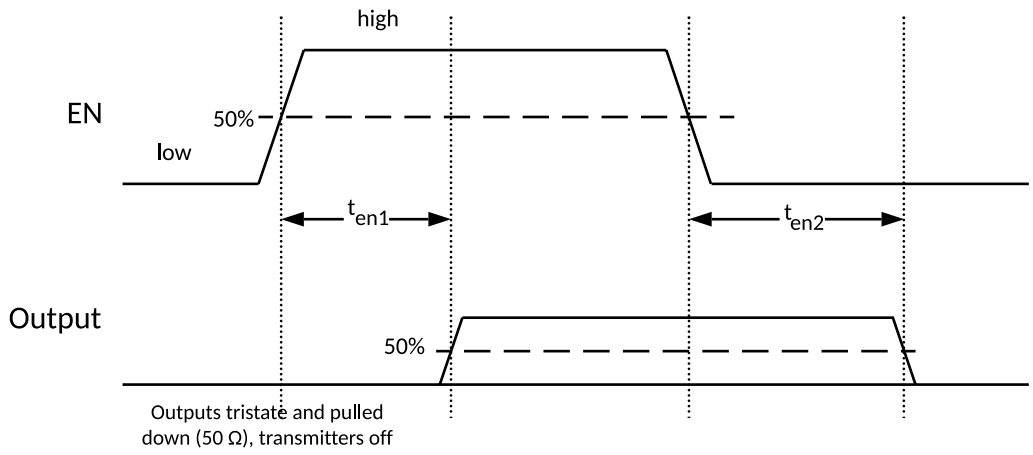

Figure 4.1. ENABLE Timing Diagram

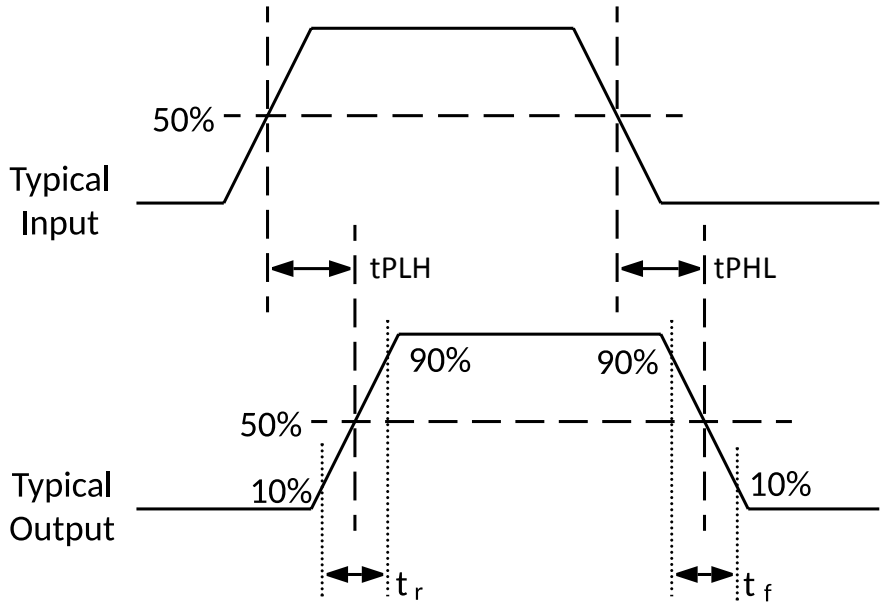

Figure 4.2. Propagation Delay Timing

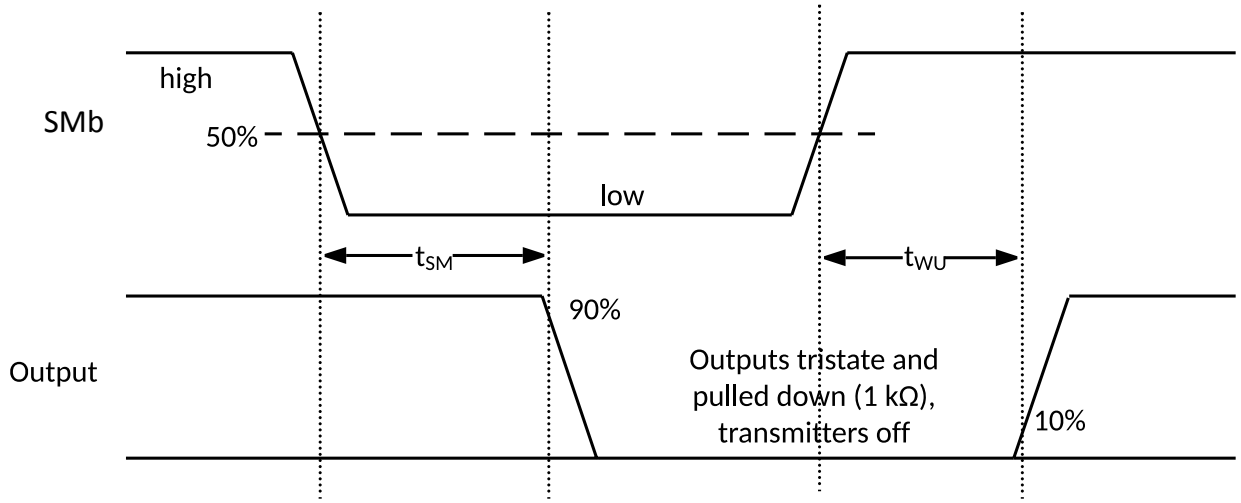

Figure 4.3. SMb Timing

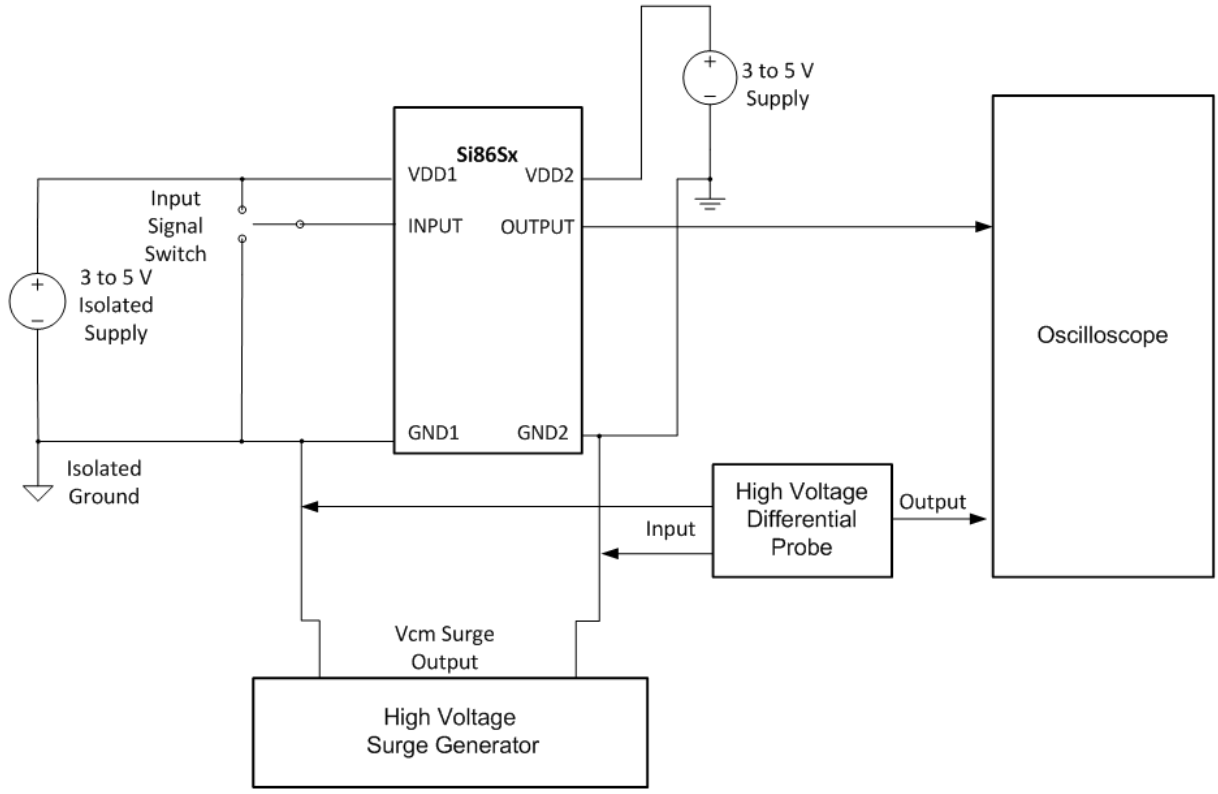

Figure 4.4. Common-Mode Transient Immunity Test Circuit

Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Electrical Characteristics tables for actual specification limits. All typical characteristics data is valid for nominal VDD and ambient temperature of 25°C.

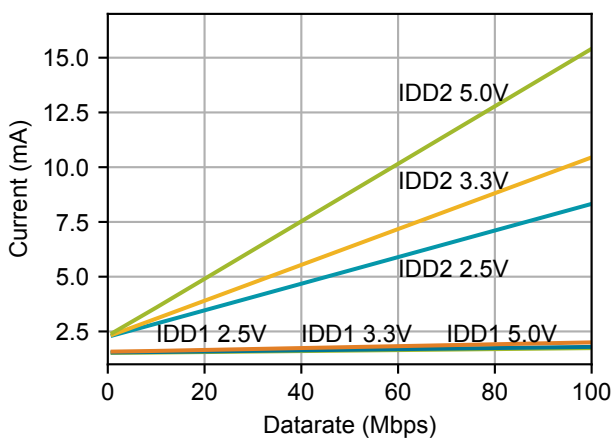

Figure 4.5. Si86S630 Typical Supply Current vs. Data Rate

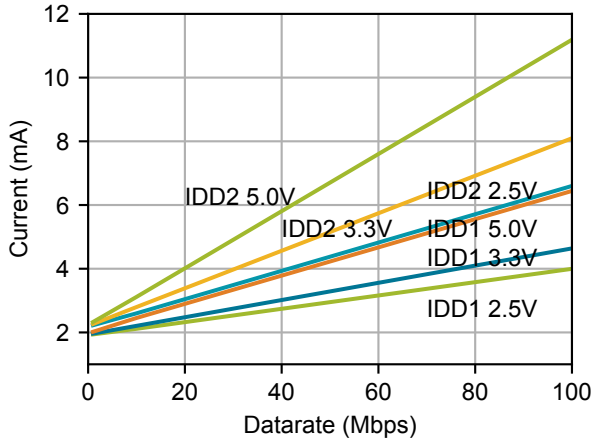

Figure 4.6. Si86S631 Typical Supply Current vs. Data Rate

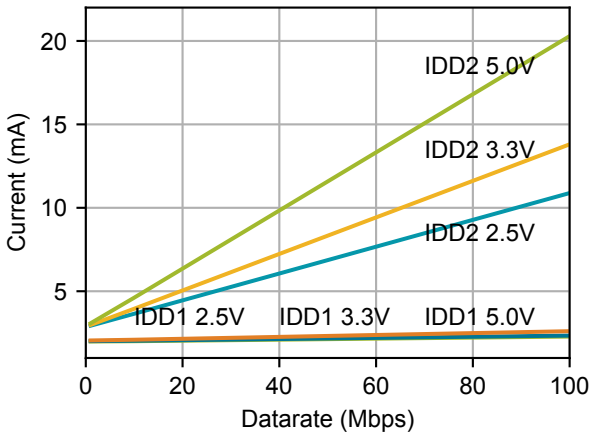

Figure 4.7. Si86S6/L/M/40 Typical Supply Current vs. Data Rate

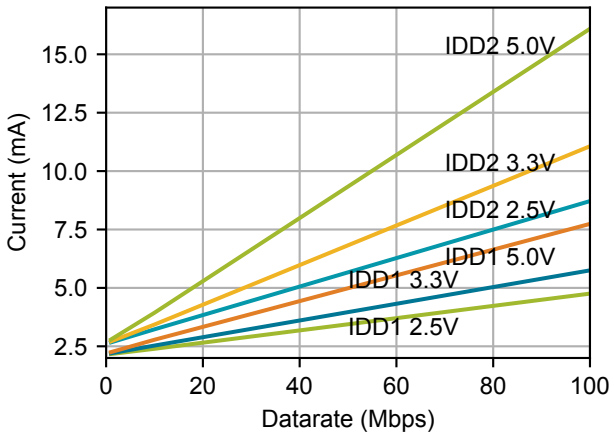

Figure 4.8. Si86S6/L/M/41 Typical Supply Current vs. Data Rate

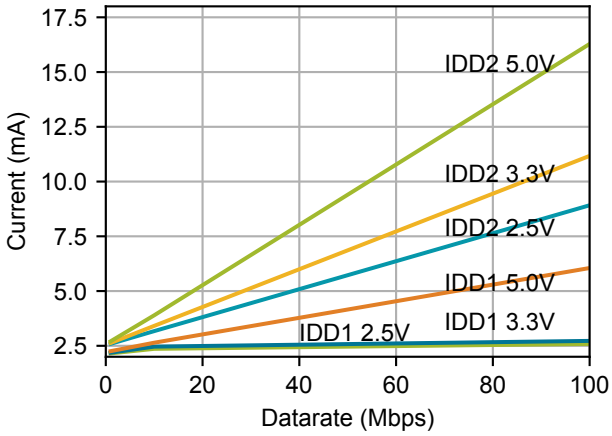

Figure 4.9. Si86SS41 Typical Supply Current vs. Data Rate

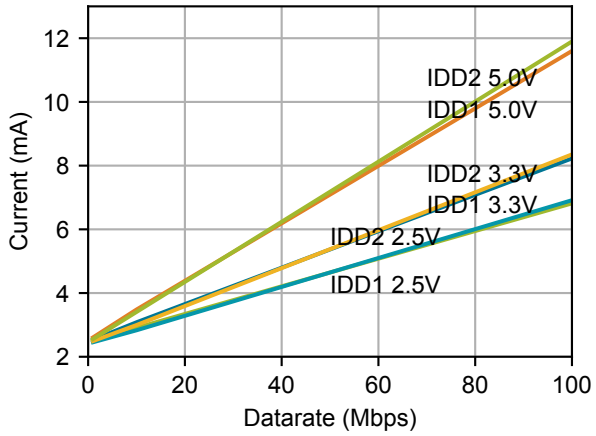

Figure 4.10. Si86S6/L/M/42 Typical Supply Current vs. Data Rate

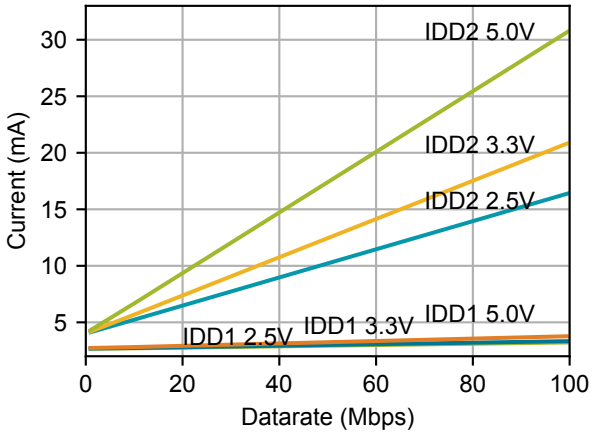

Figure 4.11. Si86S660 Typical Supply Current vs. Data Rate

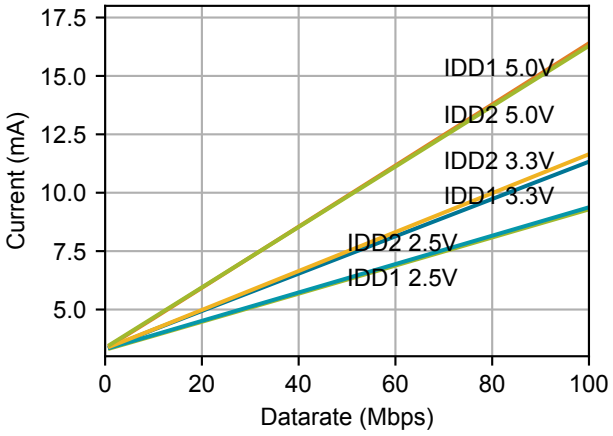

Figure 4.12. Si86S663 Typical Supply Current vs. Data Rate

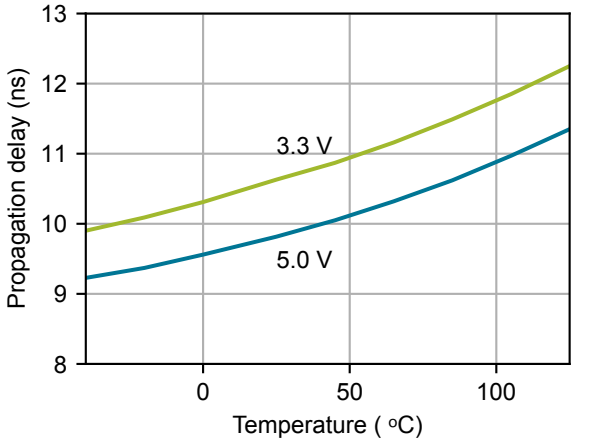

Figure 4.13. Si86S6x Propagation Delay vs. Temperature

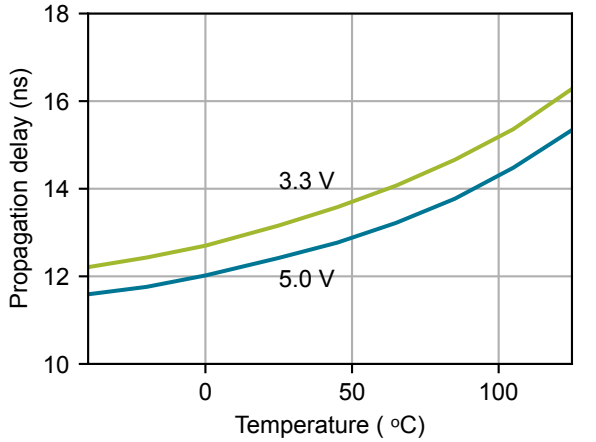

Figure 4.14. Si86SLx Propagation Delay vs. Temperature

Table 4.6. Regulatory Information[1]

CSA
The Si86Sx is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si86Sx is certified under VDE. For more details, see File 5028467.
IEC60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si86Sx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS}, V_{ISO} isolation voltage for basic protection.
CQC
The Si86Sx is certified under GB4943.1-2011.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.
Note: 1. Regulatory Certifications apply to >2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 6.0 kV_{RMS} rated devices which are production tested to 7.2 kV_{RMS} for 1 sec. For more information, see Section1. Ordering Guide.

Table 4.7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Nominal External Air Gap (Clearance)	CLR		8.0	3.9	3.6	mm
Nominal External Tracking (Creepage)	CRP		8.0	3.9	3.6	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	0.036	0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.031	mm
Resistance (Input-Output) [1]	RIO	Test voltage = 500 V	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output) [1]	CIO	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance [2]	CI		4.0	4.0	4.0	pF

Note:

1. To determine resistance and capacitance, the Si86Sx is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 4.8. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-16	NB SOIC-16	QSOP-16
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV	I-III	I-III
	Rated Mains Voltages < 600 V_{RMS}	I-IV	I-II	I-II
	Rated Mains Voltages < 1000 V_{RMS}	I-III	I	I

Table 4.9. IEC 60747-17 Insulation Characteristics for Si86Sx [1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Maximum Working Insulation Voltage	V_{IOWM}		1500	1500	1500	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}	Method b1 (VIORM x 1.875 = VPR, 100% Production Test, tm = 1 sec, Partial Discharge < 5 pC)	2121	2121	2121	V_{peak}
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, tm = 1 sec, Partial Discharge < 5 pC)	3976	3976	3976	V_{peak}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 60 s	8000	4000	4000	V_{peak}
Maximum Surge Isolation Voltage	V_{IOSM}	Tested with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	10400	V_{peak}
Maximum Impulse Voltage	V_{IMP}		8000	5514	5090	V_{peak}
Pollution Degree		DIN VDE 0110	2	2	2	
Insulation Resistance	R_S	TAMB = T_S, V_{IO} = 500 V	>10^9	>10^9	>10^9	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si86Sx provides a climate classification of 40/125/21.

Table 4.10. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Safety Temperature	T_S		150	150	150	°C
Safety Input, Output, or Supply Current	I_S	Refer to θ_{JA} in Table 4.11 Thermal Characteristics on page 53,	350	339	316	mA
Safety Input, Output, or Total Power	P_S	V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	1894	1865	1712	mW

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.15 (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Current on page 53.
2. The Si86Sx is tested with IDD1 = IDD2 = 5.5 V; T_J = 150ºC; CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 4.11. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16	QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	66	67	73	°C/W
IC Junction-to-board Thermal Resistance	θ_{JB}	35	30	43	
IC Junction-to-Case Thermal Resistance	θ_{JC}	24	20	31	
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board	Ψ_{JB}	33	29	43	

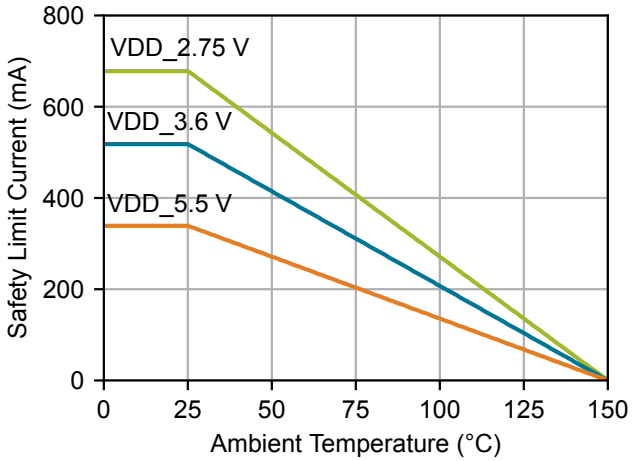

Figure 4.15. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Current

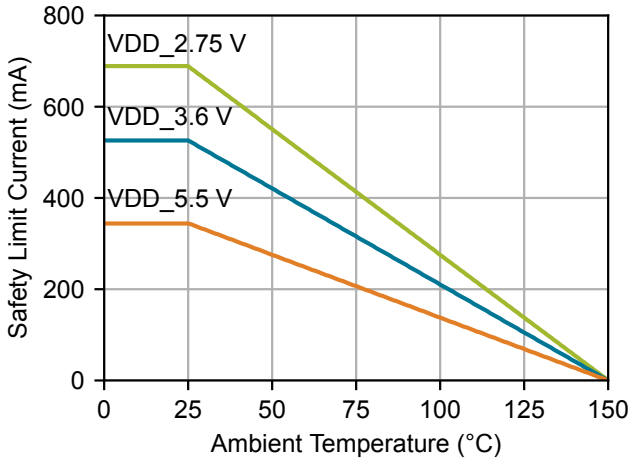

Figure 4.16. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Current

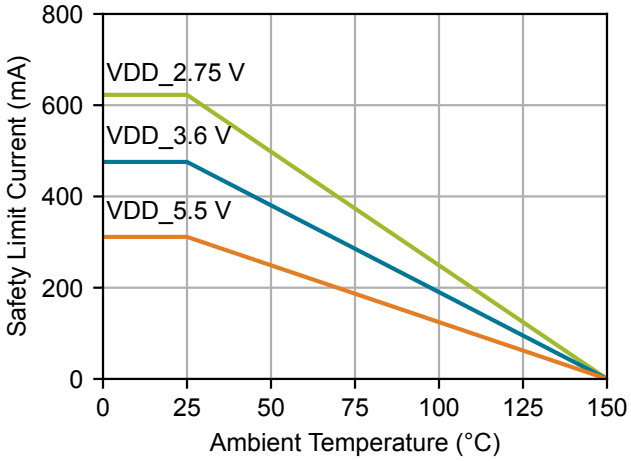

Figure 4.17. (QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Current

Table 4.12. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TSTG	–65	150	°C
Operating Temperature	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	VDD1, VDD2	–0.5	7.0	V
Supply Voltage Ramp-up	VDD1, VDD2	-	1	V/µs
Input Voltage	VI	–0.5	VDD + 0.5	V
Output Voltage	VO	–0.5	VDD + 0.5	V
Output Current Drive Channel	IO	—	10	mA
ESD	HBM	—	6	kV
ESD	CDM	—	0.5	kV
ESD[2]	IEC 61000-4-2 contact discharge	—	8000	V
Lead Solder Temperature (10 s)		—	260	°C

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.
2. This test is performed across the isolation barrier with device in a two terminal configuration, with pins on each side shorted together. Tested per IEC 61000-4-2 contact discharge.

5. Pin Descriptions

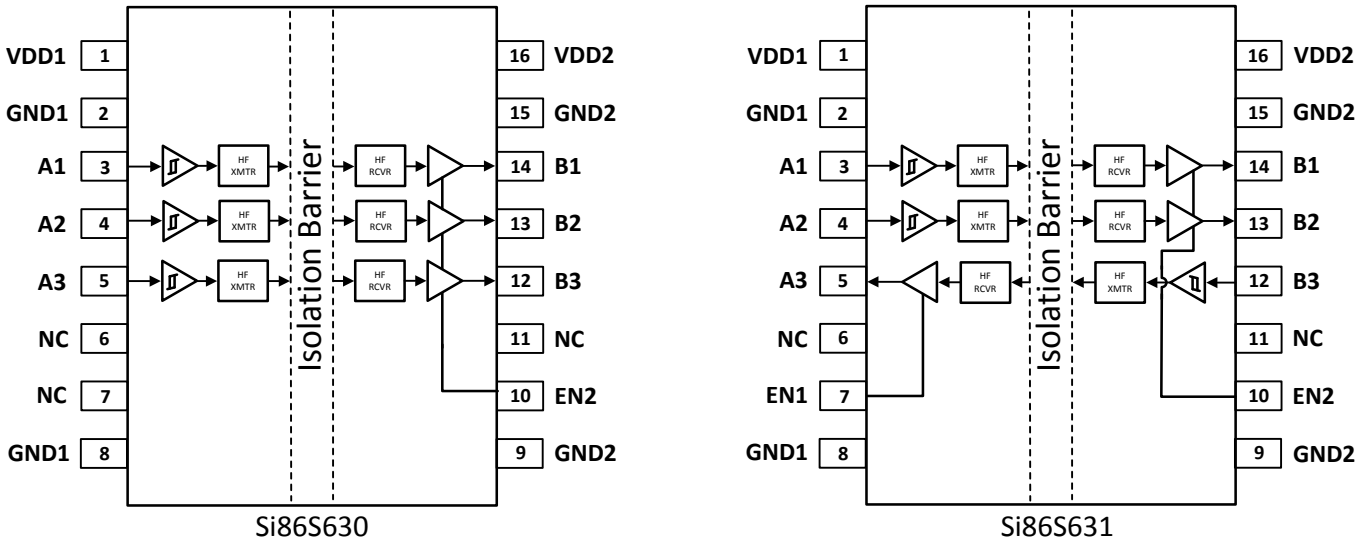

Figure 5.1. Si86S63x Pinouts

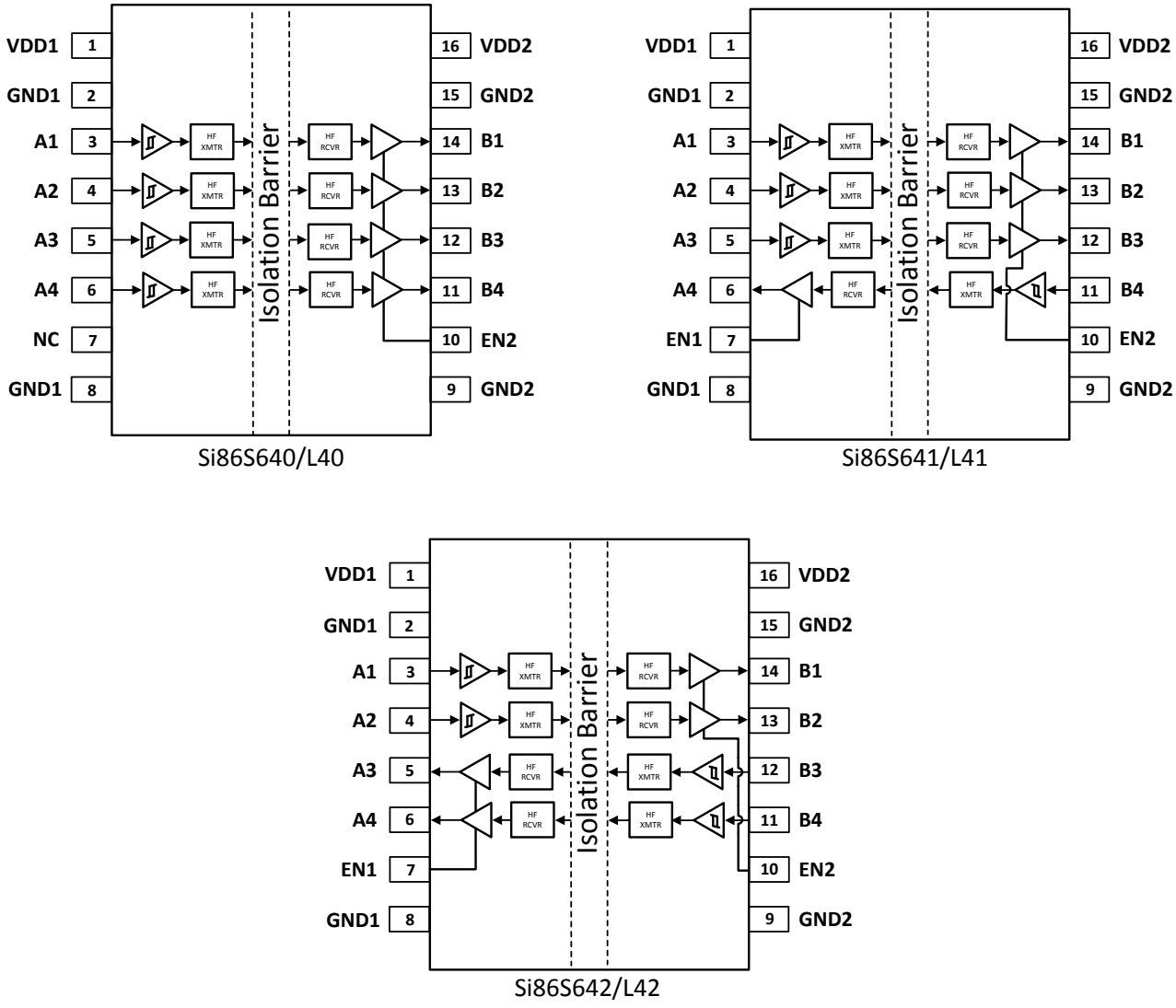

Figure 5.2. Si86S64x/L4x Pinouts

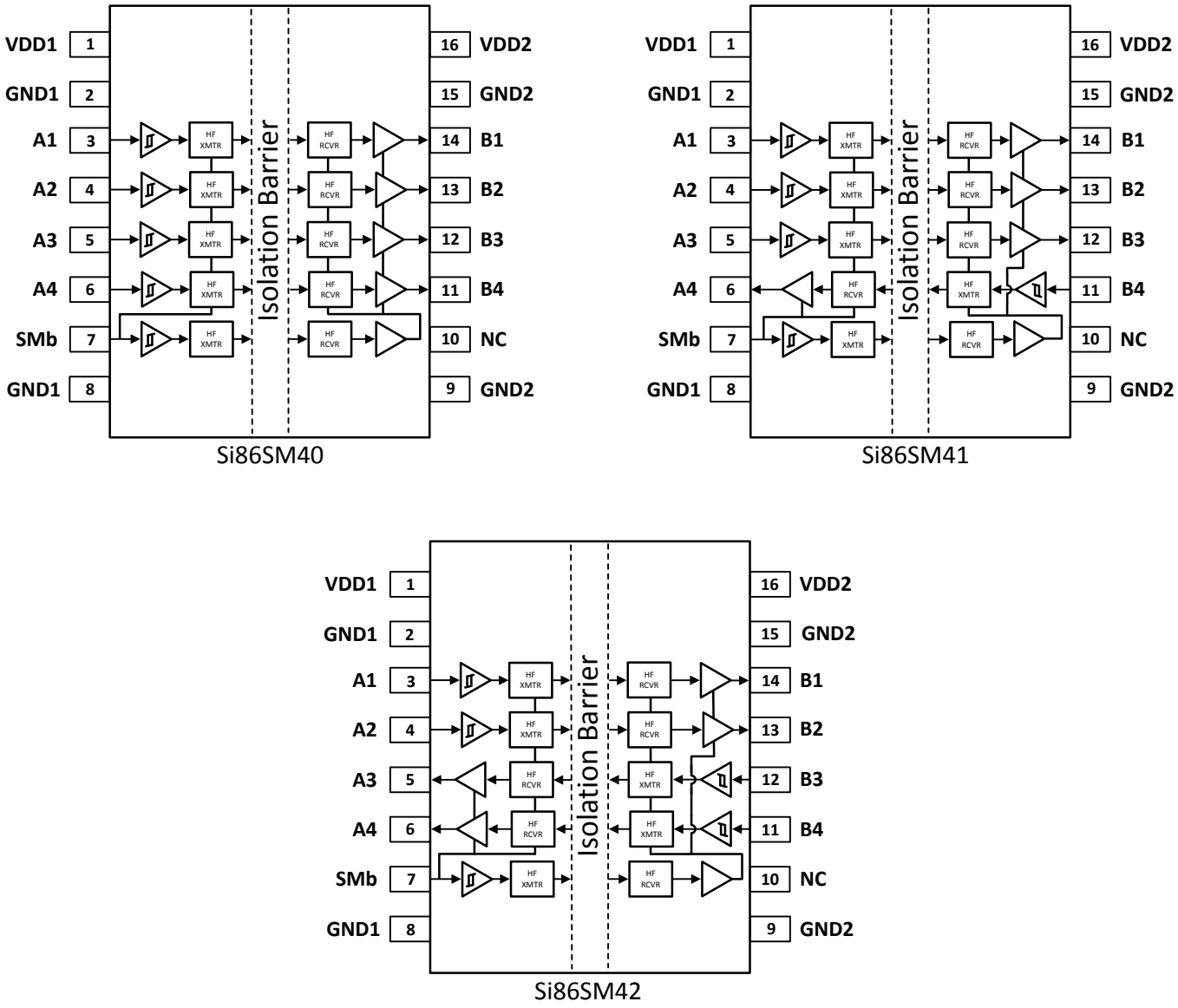

Figure 5.3. Si86SM4x Pinouts

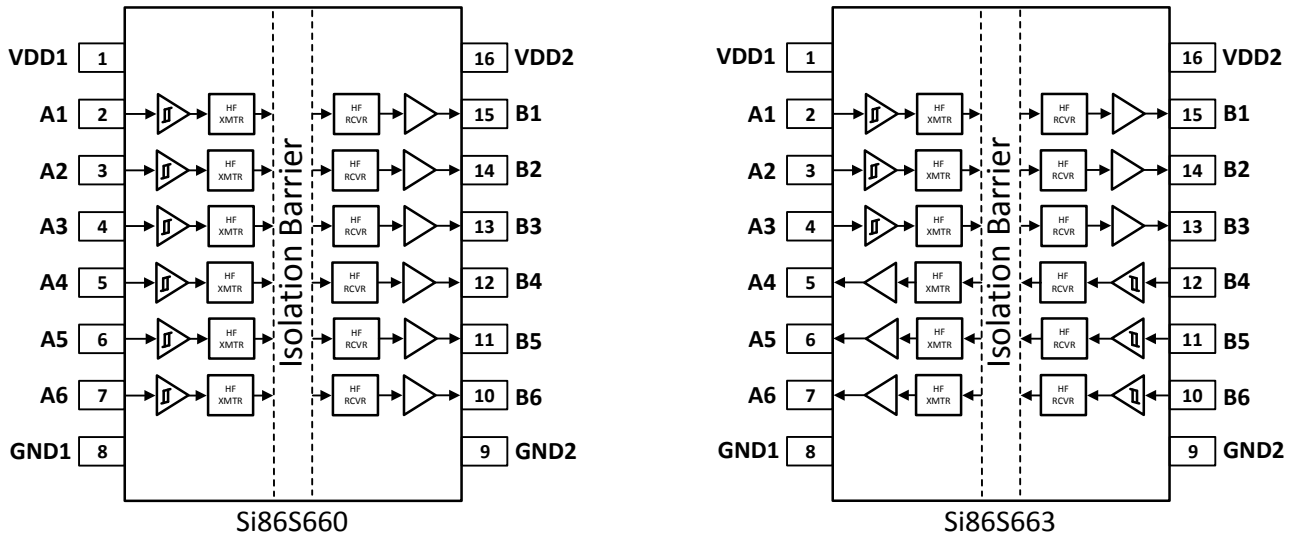

Figure 5.4. Si86S66x Pinout

Table 5.1. Si86S6x/Lx/Mx Pin Description

Name	Type	Description
VDD1	Supply	Side A power supply
GND1	Ground	Side A ground
A1 – A6	Digital I/O	Side A digital I/O
EN1/EN2	Digital Input	Side A/B active high output enable
SMb	Digital Input	Sleep mode active high for OPNs Si86SMx
NC	-	Not connected
GND2	Ground	Side B ground
B1 – B6	Digital I/O	Side B digital I/O
VDD2	Supply	Side B power supply

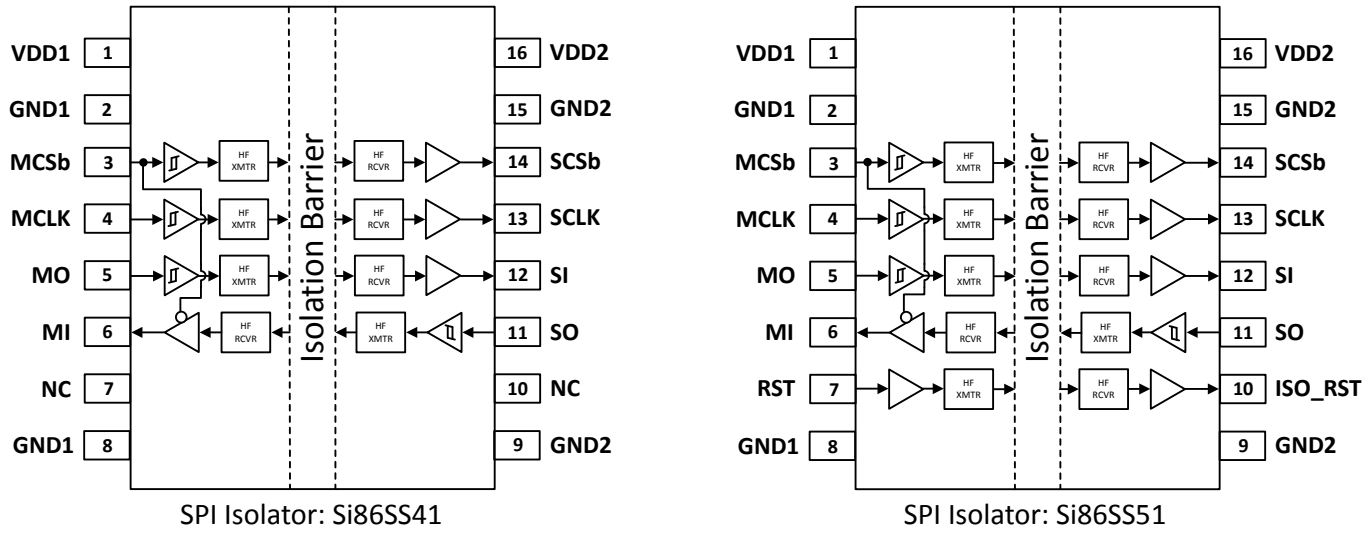

Figure 5.5. Si86SS41/51 Pinout

Table 5.2. Si86SS41/51 Pinout Description

Name	Type	Description
VDD1	Supply	Main side (Side A) power supply pin
GND1	Ground	Main side supply ground pin
MCSb	Digital Input	Main side SPI bus chip select, active low input pin
MCLK	Digital Input	Main side SPI CLK input pin
MO	Digital Input	Main side input pin
MI	Digital Output	Main side output pin
NC (Si86SS41)	—	Not connected
RST (Si86SS51)	Digital Input	Reset
ISO_RST (Si86SS51)	Digital Output	Isolated Reset
GND2	Ground	Secondary side supply ground pin
SI	Digital Output	Secondary side output pin
SO	Digital Input	Secondary side input pin
SCLK	Digital Output	Secondary side SPI CLK isolated output pin
SCSb	Digital Output	Secondary side SPI bus chip select, isolated output pin
VDD2	Supply	Secondary side power supply pin

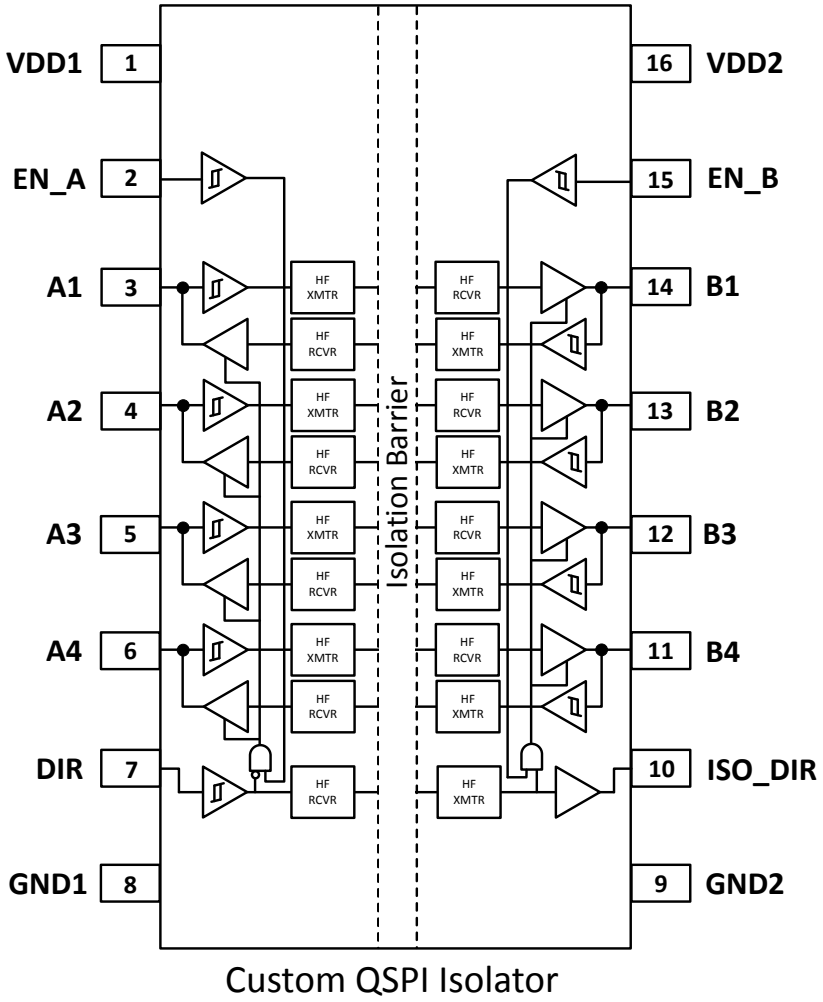

Figure 5.6. Si86SQ44 Pinout

Table 5.3. Si86SQ44 Pinout Description

Name	Type	Description
VDD1	Supply	Main side (Side A) power supply pin
EN_A	Digital Input	Output enable for side A
Ax	Digital I/O	I/O pins for side A
DIR	Digital Input	Input pin, sets channel direction for all channels
GND1	Ground	Main side (Side A) supply ground
GND2	Ground	Secondary side (Side B) supply ground
ISO_DIR	Digital Output	Isolated DIR signal output
Bx	Digital I/O	I/O pins for side B
EN_B	Digital Input	Output enable for side B
VDD2	Supply	Secondary side (Side B) power supply pin

6. Package Outline

6.1 Package Outline (WB SOIC-16)

The figure below illustrates the package details for the the Si86Sx digital isolator in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

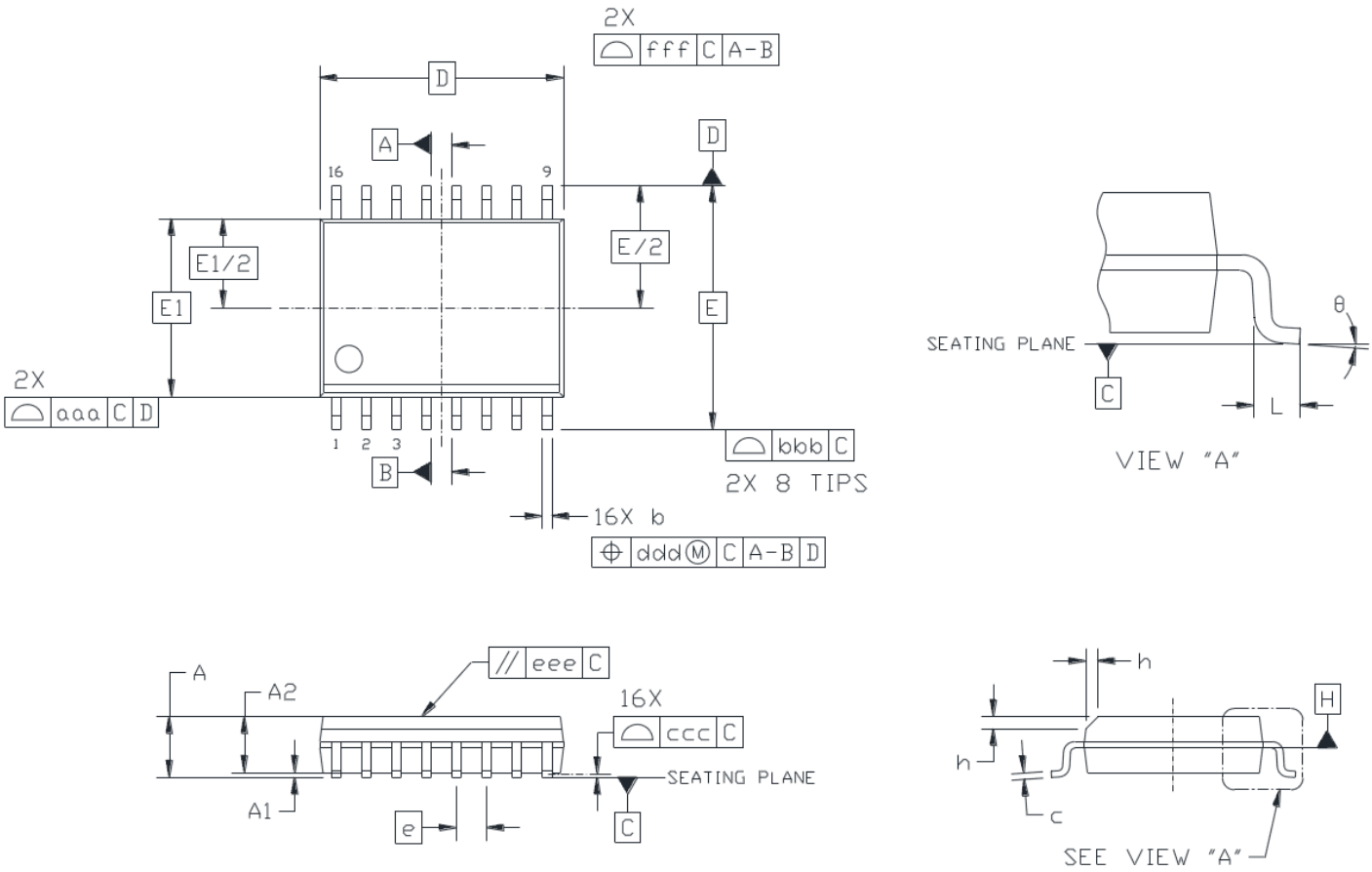

Figure 6.1. WB SOIC-16

Table 6.1. WB SOIC-16 Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75

Dimension	Min	Max
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

6.2 Package Outline (NB SOIC-16)

The figure below illustrates the package details for the Si86Sx in a 16-pin narrow-body SOIC package. The table lists the values for the dimensions shown in the illustration.

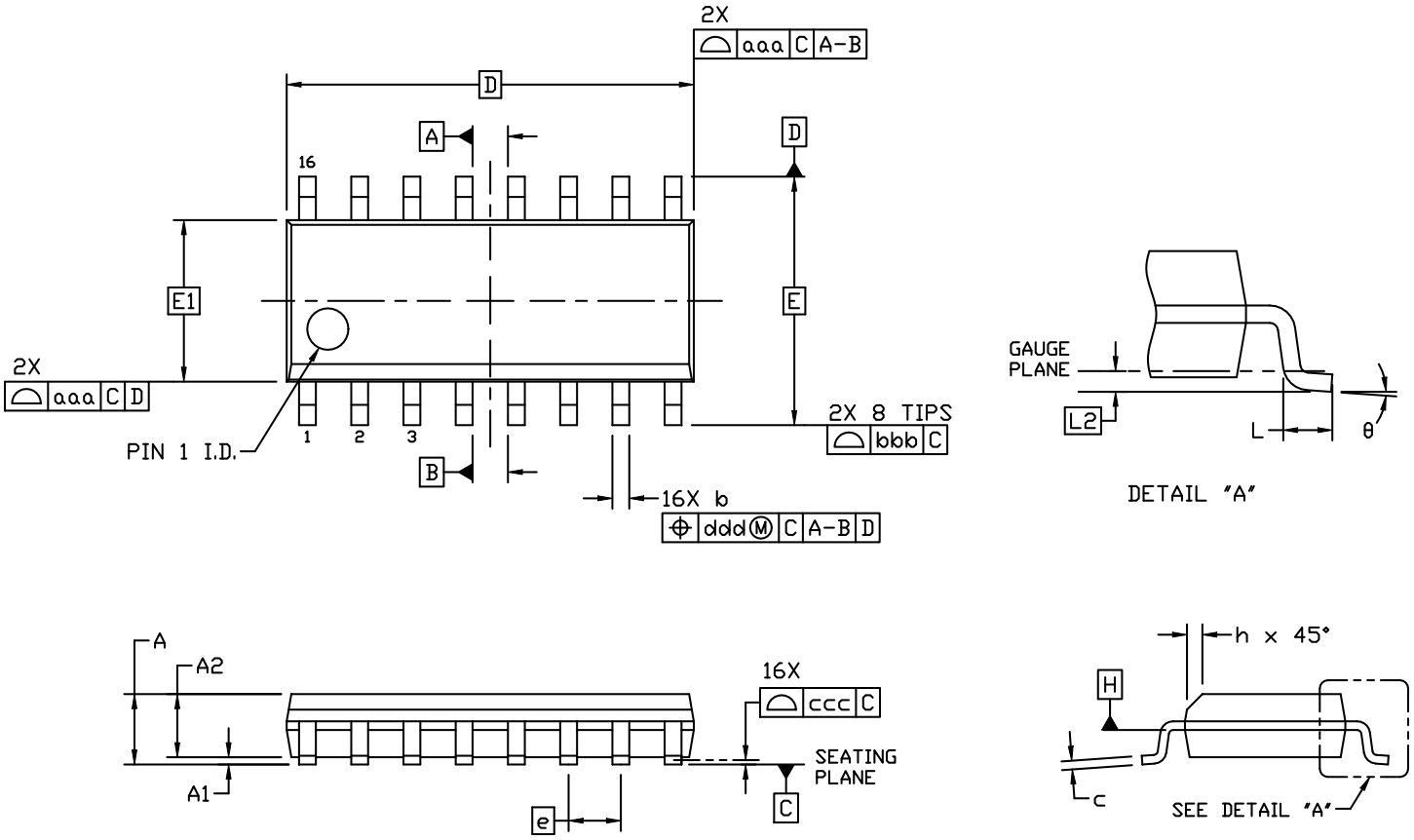

Figure 6.2. NB SOIC-16

Table 6.2. NB SOIC-16 Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	

Dimension	Min	Max
bbb	0.20	
ccc	0.10	
ddd	0.25	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 Package Outline (QSOP-16)

The figure below illustrates the package details for the Si86Sx in a 16-pin QSOP package. The table lists the values for the dimensions shown in the illustration.

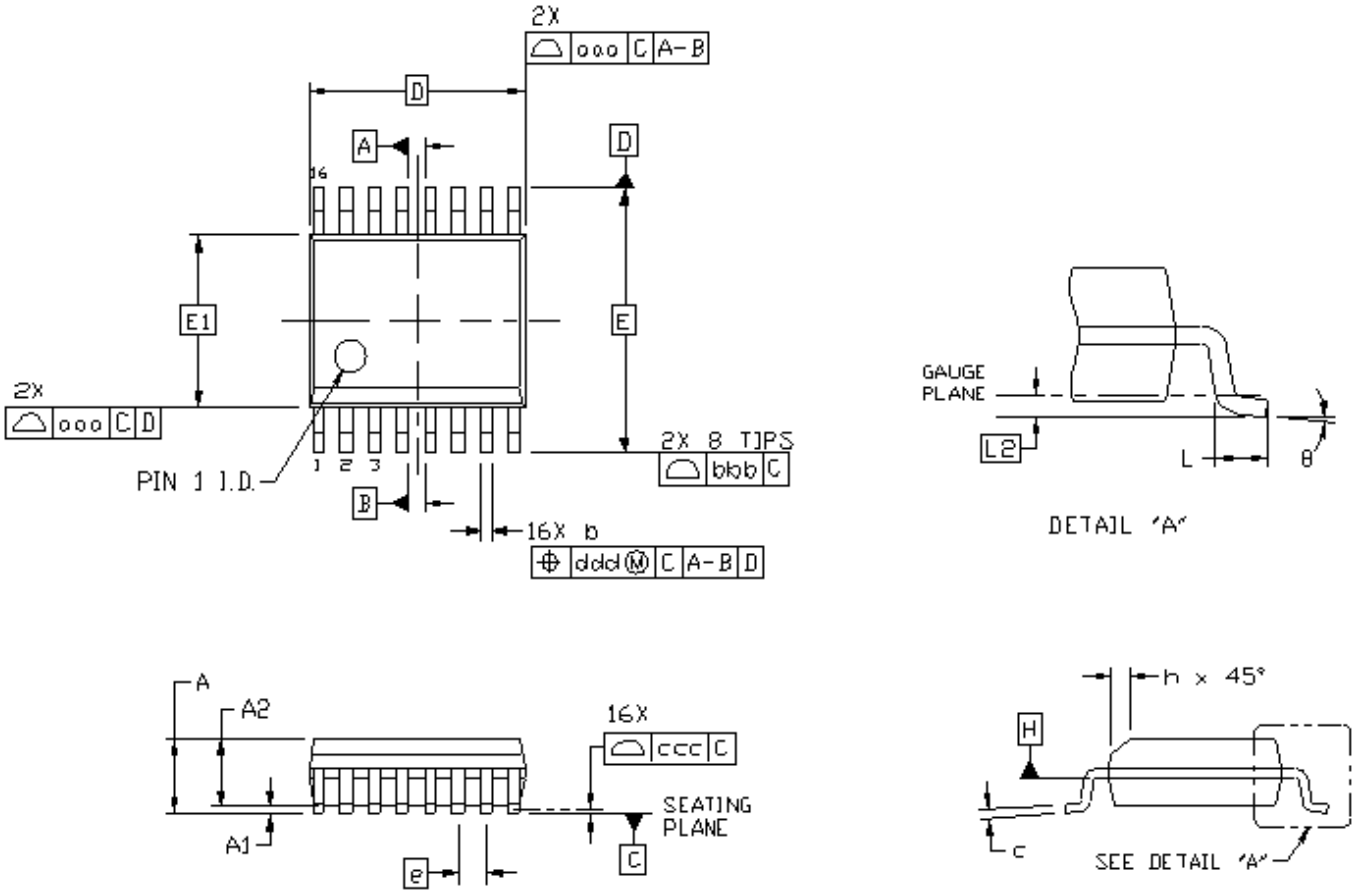

Figure 6.3. QSOP-16

Table 6.3. QSOP-16 Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50

Dimension	Min	Max
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Land Pattern

7.1 Land Pattern (WB SOIC-16)

The figure below illustrates the recommended land pattern details for the Si86Sx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

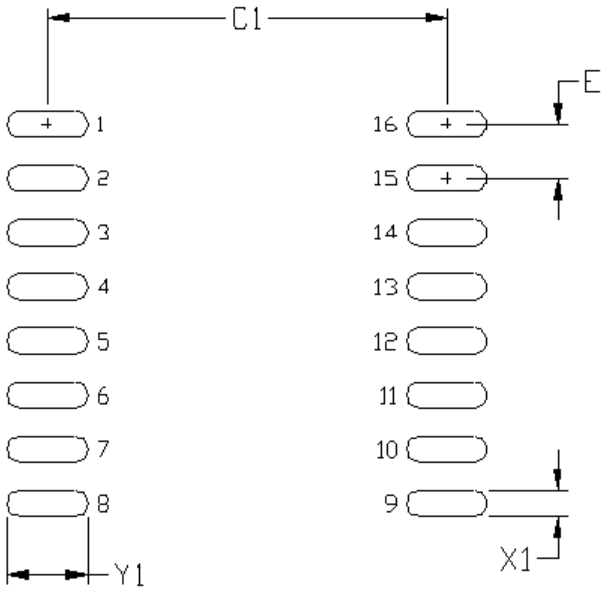

Figure 7.1. WB SOIC-16 PCB Land Pattern

Table 7.1. WB SOIC-16 Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2 Land Pattern (NB SOIC-16)

The figure below illustrates the recommended land pattern details for the Si86Sx in a 16-pin narrow-body SOIC package. The table lists the values for the dimensions shown in the illustration.

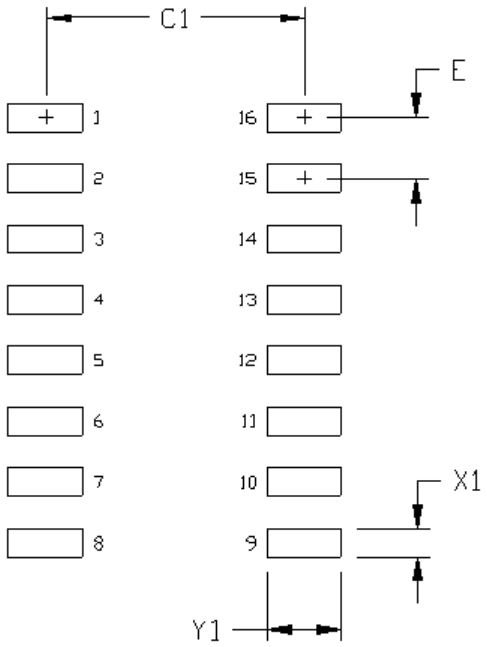

Figure 7.2. NB SOIC-16 PCB Land Pattern

Table 7.2. NB SOIC-16 Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.3 Land Pattern (QSOP-16)

The figure below illustrates the recommended land pattern details for the Si86Sx in a 16-pin QSOP package. The table lists the values for the dimensions shown in the illustration.

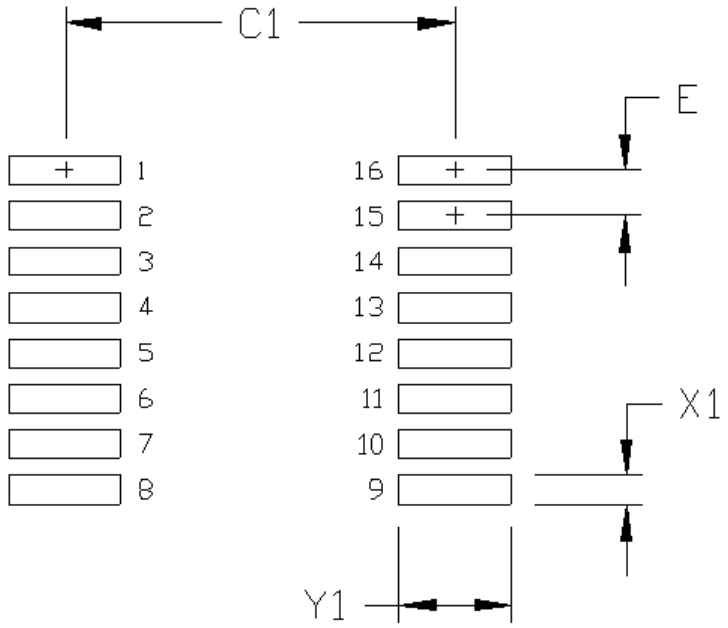

Figure 7.3. QSOP-16 PCB Land Pattern

Table 7.3. QSOP-16 Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Marking

8.1 Top Marking (WB SOIC-16)

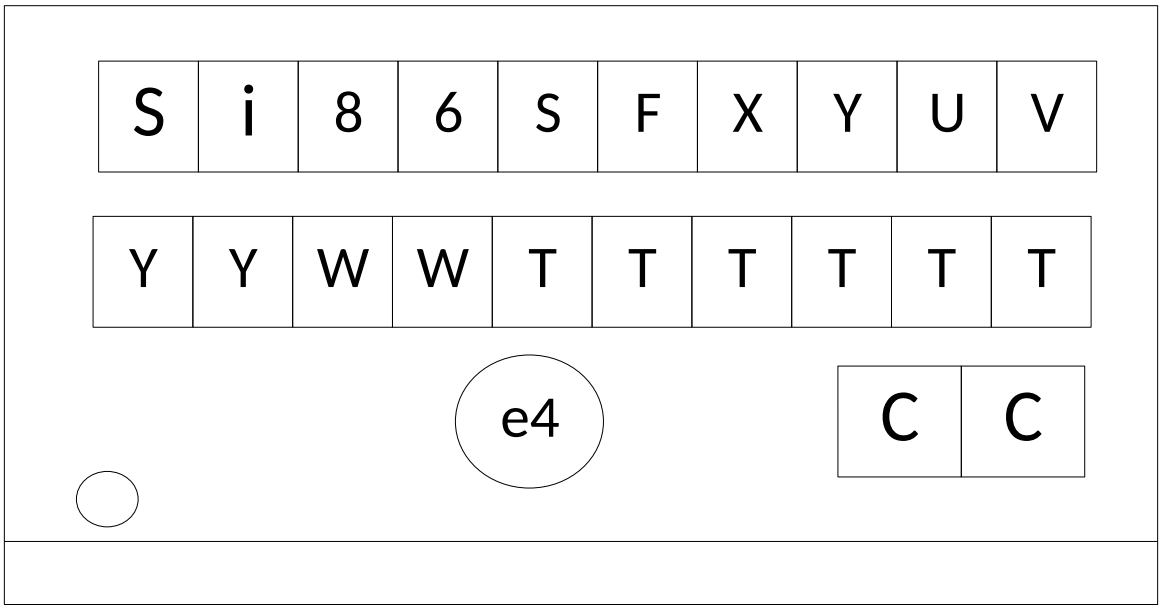

Figure 8.1. WB SOIC-16 Top Marking

Table 8.1. WB SOIC-16 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating B = 2.5 kV_{RMS} C = 3.75 kV_{RMS} E = 6.0 kV_{RMS}

Line 2 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
	TTTTTT	Manufacturing code from assembly house purchase order form
Line 3 marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	CC	Country of Origin ISO Code Abbreviation

8.2 Top Marking (NB SOIC-16)

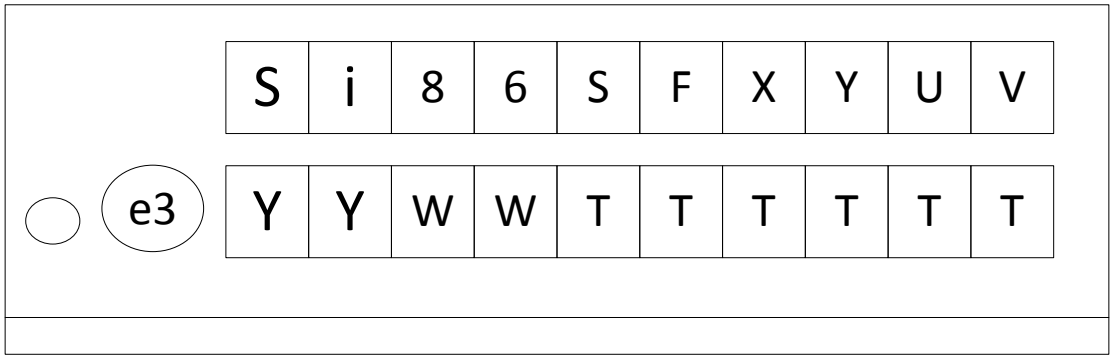

Figure 8.2. NB SOIC-16 Top Marking

Table 8.2. NB SOIC-16 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating B = 2.5 kV_{RMS} C = 3.75 kV_{RMS} E = 6.0 kV_{RMS}
Line 2 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
	TTTTTT	Manufacturing code from assembly house purchase order form
	Circle = 1.3 mm Diameter	“e3” Pb-Free Symbol

8.3 Top Marking (QSOP-16)

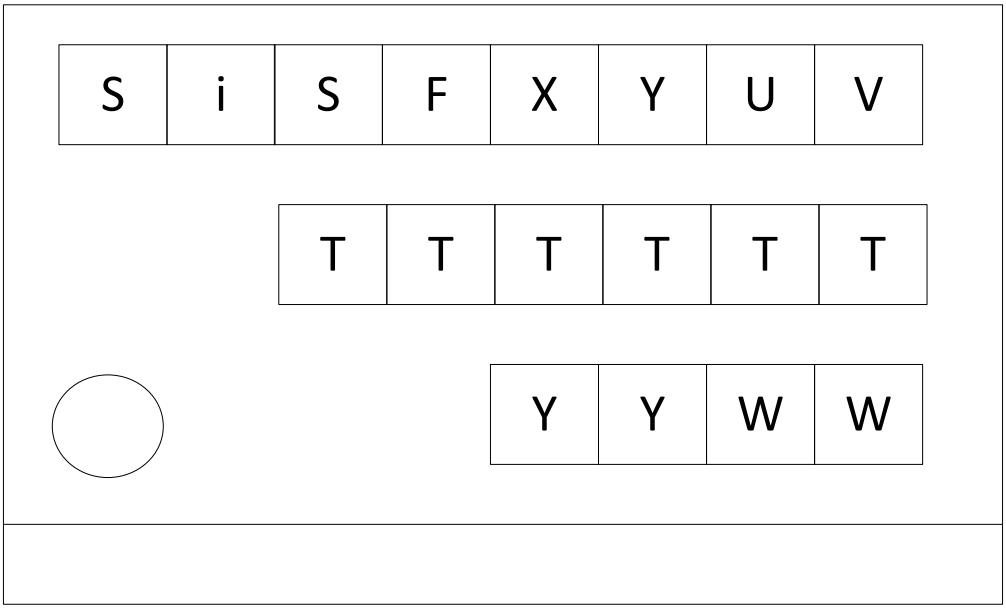

Figure 8.3. QSOP-16 Top Marking

Table 8.3. QSOP-16 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See 1. Ordering Guide for more information)	SiS = Si86S Isolator product series F = product family 6 = Industry standard footprint L = Low power mode M = Sleep mode S = SPI compatible Q = Custom QSPI implementation X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating B = 2.5 kV_{RMS} C = 3.75 kV_{RMS} E = 6.0 kV_{RMS}
Line 2 marking:	TTTTTT	Manufacturing code from assembly house purchase order form

Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house

9. Revision History

Revision 0.5

August, 2022

- Initial release.

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