19-0025; Rev. 1; 12/92

Evaluation Kit Available

MAXIM

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

General Description

The MAX176 is a complete analog-to-digital converter (ADC) that achieves a 250k samples per second (ksps) sampling rate by combining a fast track/hold (0.4µs max acquisition time), a 3.5µs ADC, and a buried-zener voltage reference. The device also saves space with serial interface and 8-pin DIP or 16-pin surface-mount SO packages.

Supply and reference decoupling capacitors are the only external components needed. The CLOCK input can be driven from an external divided-down microprocessor clock or from the serial-clock output of a microcontroller. The MAX176 works with +5V and -12V to -15V supply voltages (148mW typ power dissipation).

The MAX176's 3-wire serial interface works with general-purpose serial-to-parallel converters, such as the 74HC595, as well as with digital-signal processors and microcontrollers. Its 3-wire serial interface is fully compatible with SPI, QSPI and Microwire™ interface standards.

Applications

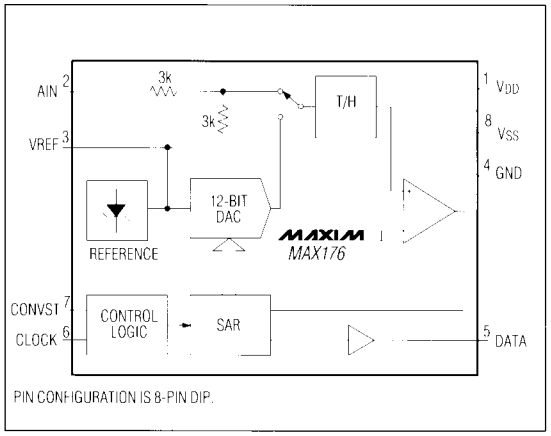
Telecommunications

Digital-Signal Processing (DSP)

Sonar/Radar Signal Processing

Industrial Data Acquisition

Functional Diagram



PIN CONFIGURATION IS 8-PIN DIP.

Features

- ♦ 12-Bit Resolution and Linearity
- ♦ 0.4µs Track/Hold Acquisition Time
- ♦ 3.5µs Max Conversion Time
- ♦ 250ksps Sampling Rate
- ♦ SPI-, QSPI- and Microwire™-Compatible Serial Output
- ♦ ±5V Input Voltage Range
- ♦ On-Chip Voltage Reference
- ♦ Low Power (148mW)
- ♦ Easy to Opto- or Transformer-Isolate
- ♦ Small-Footprint 8-Pin DIP, 16-Pin SO

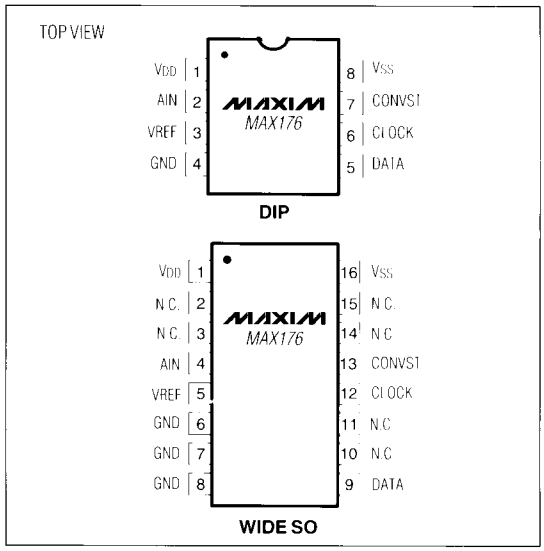
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX176ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX176BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX176ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX176BCWE	0°C to +70°C	16 Wide SO	±1
MAX176BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configurations



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Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -17V
AIN to GND ..... ±15V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
Digital Output Voltage to GND ..... -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX176_C_ _ ..... 0°C to +70°C
MAX176_E_ _ ..... -40°C to +85°C
MAX176_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, f_{CLK} = 4MHz for MAX176_C/E and f_{CLK} = 3MHz for MAX176_M, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC ACCURACY							
Resolution		Guaranteed monotonic over temp		12			Bits
Integral Nonlinearity (Note 1)	INL	T_A = T_{MIN} to T_{MAX}	MAX176AC/AE			±1/2	LSB
			MAX176BC/BE/BM			±1	
			MAX176AM			±3/4	
		T_A = +25°C	MAX176AM			±1/2	
Differential Nonlinearity (Note 1)	DNL		MAX176A			±3/4	LSB
			MAX176B			±1	
Offset Error (Notes 1, 2)					±1	±3	LSB
Offset Tempco					0.5		ppm/°C
Full-Scale Error (Note 3)		T_A = +25°C				±8	LSB
Full-Scale Tempco (Note 4)		Excluding reference drift			±1		ppm/°C
ANALOG INPUT							
Input Voltage Range				-5		5	V
Input Current						2.5	mA
Input Capacitance (Note 5)						10	pF
INTERNAL REFERENCE							
VREF Output Voltage				-4.98	-5.00	-5.02	V
VREF Output Tempco (Note 6)		MAX176_C				±30	ppm/°C
		MAX176_E/M				±40	
Load Regulation (Note 7)		0mA < I_L < 5mA				5	mV
POWER-SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS change, V_{SS} = -15V or -12V, V_{DD} = 5V ±5%				±1/2	LSB
Negative Supply Rejection	V_{SS}	FS change, V_{DD} = 5V	V_{SS} = -15V ±5%			±1/2	LSB
			V_{SS} = -12V ±5%			±1/2	
LOGIC INPUTS (CLK, CONVST)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 5)	C_{IN}					10	pF
Input Current	I_{IN}	Input voltage = 0V to V_{DD}				±5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, f_{CLK} = 4MHz for MAX176_C/E and f_{CLK} = 3MHz for MAX176_M, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC TESTS (A_{IN} = 10V_{p-p}, f_{AIN} = 50.17kHz, $f_{SAMPLING}$ = 250ksps for MAX176_C/E, $f_{SAMPLING}$ = 200ksps for MAX176_M)							
Signal-to-Noise plus Distortion	S/(N+D)			70	72		dB
Total Harmonic Distortion	THD				-90	-80	dB
Peak Harmonic or Spurious Noise					-90	-80	dB
Input Slew Rate				1.5			V/µs
Conversion Time	tCONV	14 clock cycles	MAX176_C/E			3.5	µs
			MAX176_M			4.7	
Acquisition Time (Note 5)	tAQ					400	ns
Clock Frequency	fCLK		MAX176_C/E	0.1		4.0	MHz
			MAX176_M	0.1		3.0	
LOGIC OUTPUT (DATA)							
Output Low Voltage	VOL	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	VOH	I_{SOURCE} = 200µA		4.0			V
POWER REQUIREMENTS							
Positive Supply Voltage	VDD	±5% for specified performance			5		V
Negative Supply Voltage	VSS	±5% for specified performance			-15 to -12		V
Positive Supply Current	IDD	CONVST = V_{DD}, AIN = 0V			5.5	8	mA
Negative Supply Current	ISS	CONVST = V_{DD}, AIN = 0V			-8	-11	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V			123	172	mW

TIMING CHARACTERISTICS (Note 8)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to 15.75V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Pulse Width High	tCH			50			ns
Low	tCL		MAX176_C/E	80			
			MAX176_M	100			
CONVST Pulse Width High	tSH			50			ns
Low	tSL		MAX176_C/E	120			
			MAX176_M	150			
CONVST-to-CLOCK Skew Leading Clock	tSC0					30	ns
Leading Clock +1	tSC1		MAX176_C/E	120			
			MAX176_M	160			
Clock-to-Data Delay (Note 9)	tPD		MAX176_C/E	20		130	ns
			MAX176_M	20		170	
Acquisition Time (Note 5)	tAQ	FS change at AIN				400	ns

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

TIMING CHARACTERISTICS (Note 8) (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Aperture Delay (Note 5)				10		ns
CONVST Rise Time (Note 5)					100	ns
Output Float Delay (Note 10)		MAX176C/E			100	ns
		MAX176M			120	

Note 1: These tests are performed at V_{DD} = +5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Offset measured at 0...00 to 0...01 digital output code.
Note 3: FS = 5.000V. Ideal last-code transition = FS - 3/2LSB. Adjusted for offset error.
Note 4: Full-Scale Tempco = (Δ V_{FS})/(Δ T), where Δ V_{FS} is Full-Scale voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 5: Guaranteed by design, not subject to test.
Note 6: VREF Tempco = (Δ VREF)/(Δ T), where Δ VREF is reference-voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 7: Output current should not change during conversion.
Note 8: Timing specifications are 100% tested. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Output delays are measured to 0.8V if going low and 2.4V if going high.
Note 9: DATA pin is loaded with 50pF to GND.
Note 10: DATA pin is loaded with 10pF || 3kΩ. Defined as the time required for data lines to change 0.5V.

Pin Description

PIN DIP	PIN SO	NAME	FUNCTION
1	1	V_{DD}	Positive Supply, +5V ±5%
2	4	AIN	Analog Input, ±5V bipolar input range
3	5	VREF	Reference Voltage Output, -5.0V
-	6, 7, 8	GND	Ground. Connect all 3 pins to system ground.
4		GND	Ground
	8	DGND	Digital Ground
5	9	DATA	Serial Data Output
6	12	CLOCK	Clock Input, TTL/+5V CMOS compatible
7	13	CONVST	Conversion Start Input
8	16	V_{SS}	Negative Supply, -11.4V to -15.75V
-	2, 3, 10, 11, 14, 15	N.C.	No Connect. Not internally connected.

Detailed Description

Converter Operation

The MAX176 uses a successive-approximation technique to convert an unknown analog input to a 12-bit digital output code. The digital interface requires only three digital lines: CLOCK and CONVST are both inputs, and the DATA output provides the conversion result in serial form. Figure 1 shows the typical operating circuit.

Figure 2 shows the MAX176 analog-equivalent circuit, which illustrates the basic functional blocks within the device. Note that after the input voltage is sampled, AIN is disconnected from the MAX176's converter portion. This removes the possibility of the converter demanding current spikes from the device driving AIN.

A conversion is intiated by the convert start rising edge. Once started, a conversion cannot be stopped and transitions at the CONVST input have no effect until the current conversion is completed. The result of a conversion is available at the DATA output in twos-complement, serial format. A high bit followed by the data bits (MSB first) make up the serial data stream. Conversions may be done one at a time (burst mode) or on a repetitive basis (continuous-conversion mode).

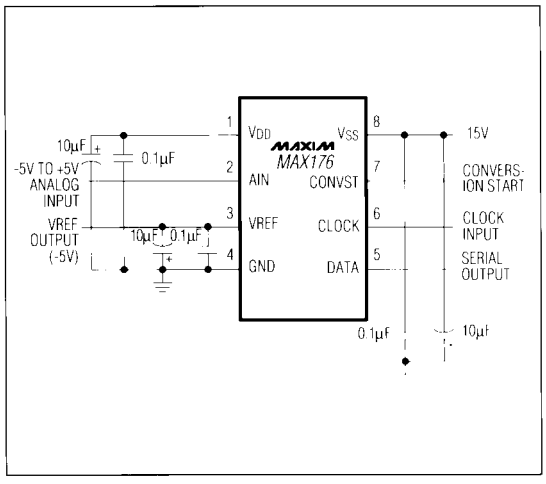

Figure 1. MAX176 Operational Configuration

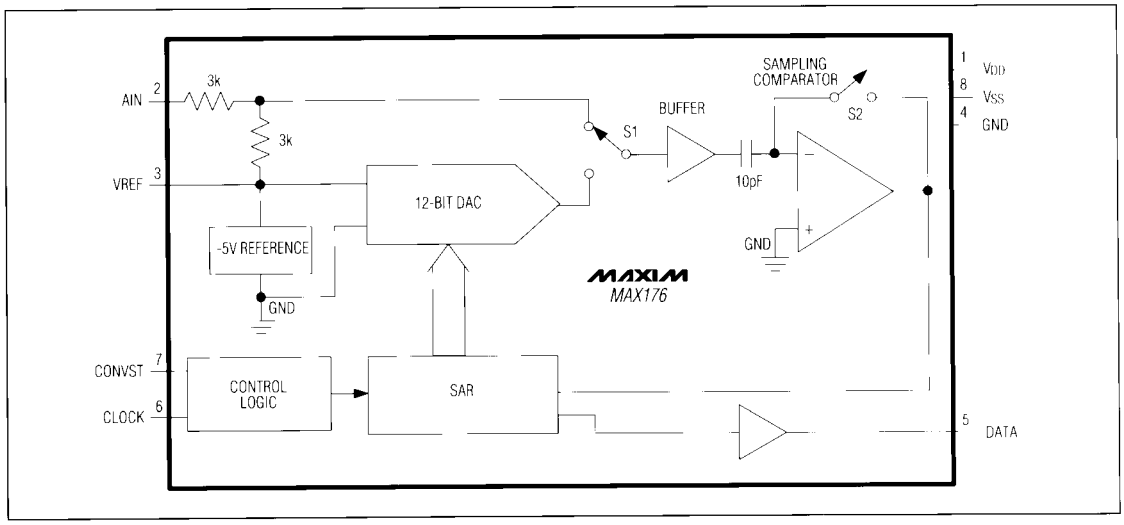

Figure 2. MAX176 Analog Equivalent Circuit

Burst Mode

Figure 3 illustrates the timing relationship between the convert start, clock, and data waveforms when the MAX176 operates in burst mode. Convert start's rising edge causes the internal track/hold (T/H) circuit to hold the analog input voltage and initiates the conversion. The T/H returns to track mode after the 13th falling clock edge.

When burst mode is used, clock edges typically appear **after** convert start's rising edge. Thus, Figure 4 shows the recommended placement of clock's falling edge after the rising edge of convert start; this placement ensures that the serial output's leading high bit appears at the first falling clock edge after convert start rises. The convert start to clock skew specification, t_{SC1}, dictates the suggested positioning of clock's falling edge. No problem occurs if clock's falling edge appears earlier than suggested; the serial data stream is simply delayed by a clock cycle. Note, however, that a high-speed clock edge occurring within 40ns of convert start's rising edge could cause a small inaccuracy in the sampled voltage. This is due to the ground bounce induced by the clock edge speed.

Each bit of the serial data stream appears after a clock falling edge. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Rising edges are usually used to strobe the serial data into a register. Pay attention to the clock-to-data delay (t_{pd}) specification at the highest clock frequencies when using a rising clock edge to strobe a data bit into a register.

Extra clock pulses prior to a new convert start rising edge have no effect on the converter operation.

Continuous-Conversion Mode

Figure 5 shows the timing relationship between the convert start, clock, and data waveforms when the MAX176 is operated in continuous-conversion mode. As in the burst mode, convert start's rising edge places the T/H circuit in hold mode and initiates the conversion. Here also, the 13th falling clock edge puts the T/H in track mode.

In continuous-conversion mode, convert start's rising edge must be correctly positioned with respect to clock's falling edges to satisfy the t_{SC0} and t_{SC1} specifications (Figure 6). These specifications must be met if the serial data stream high bit is to appear after the first falling clock edge. One caution: A high-speed clock edge may cause ground bounce; if the rising edge of convert start is within 40ns of a clock edge, the voltage stored in the T/H may be slightly inaccurate because of this ground bounce.

A conversion period of 15 clock cycles minimum is recommended. Most systems will be 16 cycles since such counters are more common. Extra clock pulses between conversions have no effect. If the clock frequency is below 2.5MHz, a minimum period of 14 cycles can also be used.

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

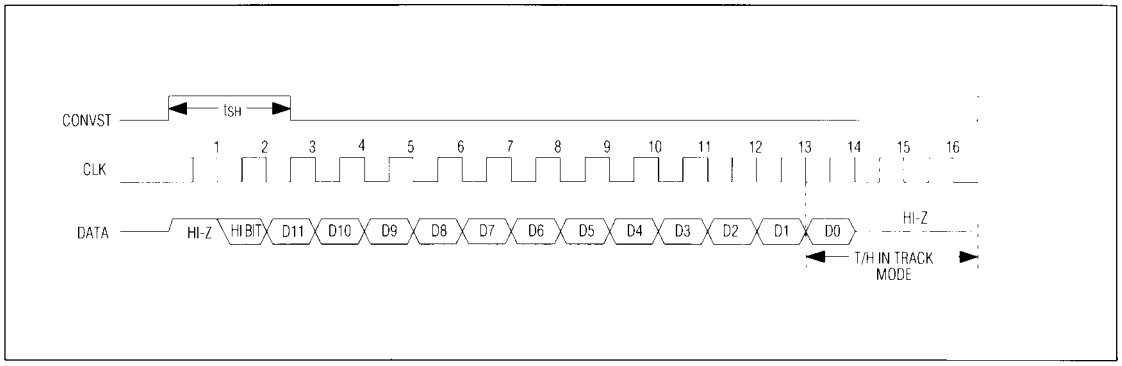

Figure 3. MAX176 Timing in Burst Mode

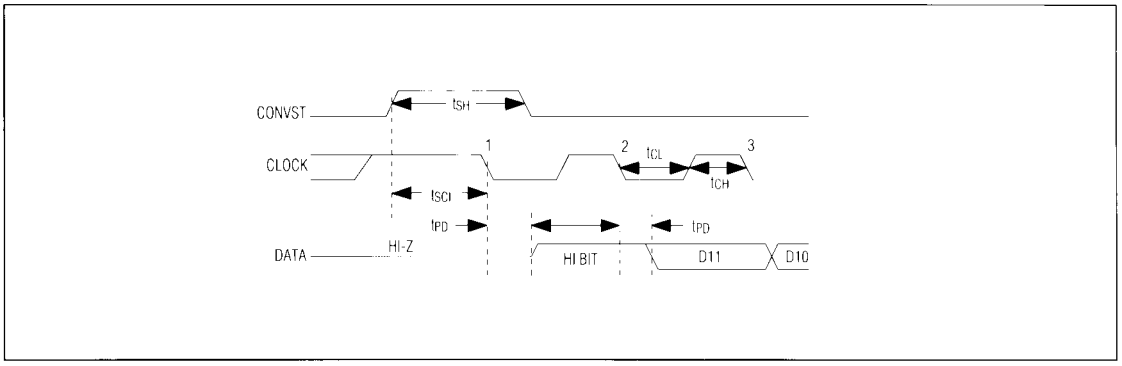

Figure 4. Recommended Placement of Clock Falling Edge in Burst Mode

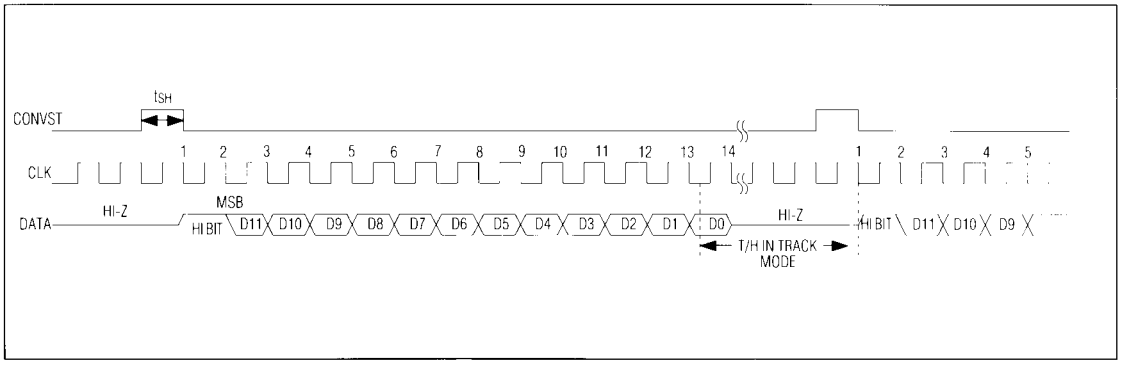

Figure 5. MAX176 Timing in Continuous Mode

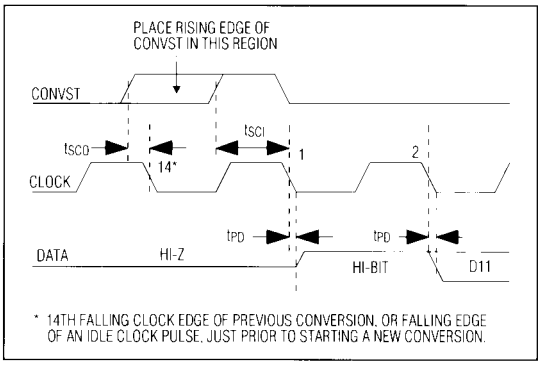

Figure 6. Recommended Placement of CONVST Rising Edge in Continuous Mode

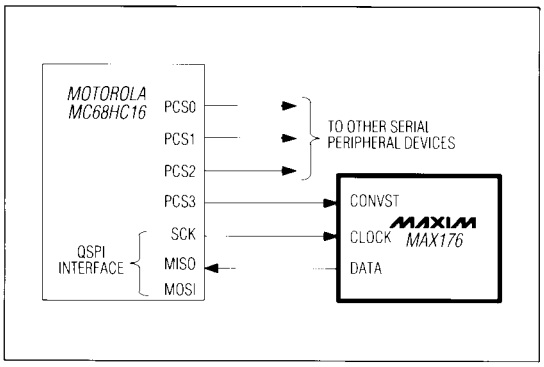

Figure 7. MAX176 Connected to QSPI Interface

Upper and Lower Clock Frequencies

It is possible to operate the MAX176 at clock rates up to 4MHz (3MHz for the military version) and down to 100kHz (for both the commercial and military devices). The lower clock limit is necessary because of the internal T/H circuit's droop.

Connection to Standard Serial Interfaces

The MAX176 serial interface is fully compatible with SPI and Microwire standard serial interfaces. Common implementations of these interfaces in microprocessors (µPs) limit the MAX176's throughput rate; the µP simply can't keep up with the serial data stream. The Motorola QSPI interface can handle the MAX176's 250ksps conversion rate; SCK from the MC68HC16 (shown in Figure 7) can operate at the MAX176's 4MHz maximum clock rate.

Output Coding and Transfer Function

Data output from the MAX176 is in twos-complement format. The first bit appearing at DATA is always high, followed by the 12 data bits (inverted most significant bit (MSB) first: 0 for positive analog inputs, 1 for negative, followed by the remaining noninverted 11 data bits).

Figure 8 shows the MAX176 nominal transfer function. Code transitions occur halfway between successive integer LSB values; one LSB = 10V/4096 = 2.44mV.

Applications Information

Offset and Full-Scale Adjustment

In applications where the offset and full-scale ranges have to be adjusted for the ADC, use Figure 9's circuit. This circuit allows adjustment of both the offset and full-scale (gain) errors. Adjust the offset first. Apply 1/2LSB (1.22mV) at the analog input and adjust the amplifier's offset until the digital output code changes between 0000 0000 0000 and 0000 0000 0001. Changes in the +5V supply affect the offset adjustment slightly. If significant supply variation is expected, connect a reference to R5 in place of the +5V supply.

To adjust the negative full-scale range, apply -FS + 1/2LSB (-2.49939V, remembering the amplifier has a gain of approximately 2) at the analog input, and adjust R2 until the output code changes between 1000 0000 0000 and 1000 0000 0001. Once this adjustment is made, the positive full-scale reading will be dictated by the integral nonlinearity (INL) specification; thus, this reading will be no further away from the optimal value than the maximum INL specification.

The value of potentiometer R5 can be increased in order to decrease the circuit's current consumption. However, increasing this resistor value decreases the adjustment sensitivity when in the middle range of pot R5, and causes relatively large changes in the op amp's output when at either end of the pot range.

Adding a voltage divider at the noninverting input allows a wider input voltage range. See the *Driving the Analog Input* section for recommended op amps for this circuit.

Figure 10 shows an alternative inverting configuration for gain and offset adjustment.

Serial-to-Parallel Data Conversion

Figure 11a shows a MAX176 with a serial-to-parallel converter. The analog input is referred to signal ground at the MAX176 GND pin. The parallel data outputs are updated at the convert start signal's rising edge. See Figure 11b for the circuit timing.

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

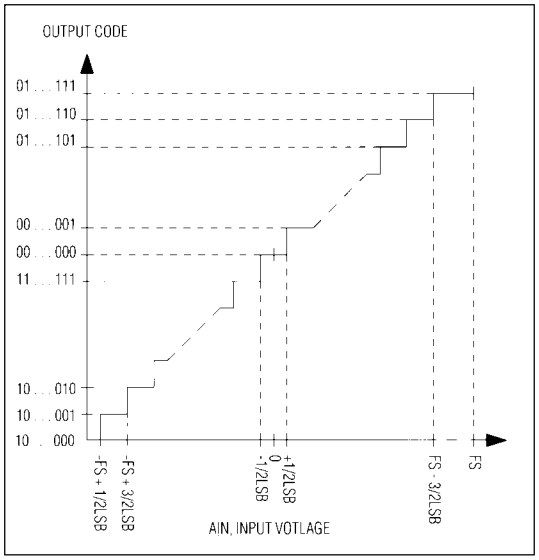

Figure 8. MAX176 Transfer Function

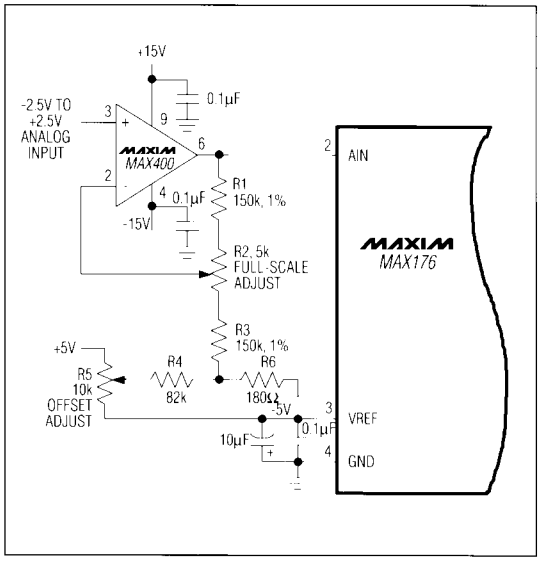

Figure 9. Noninverting Offset and Full-Scale Adjustment

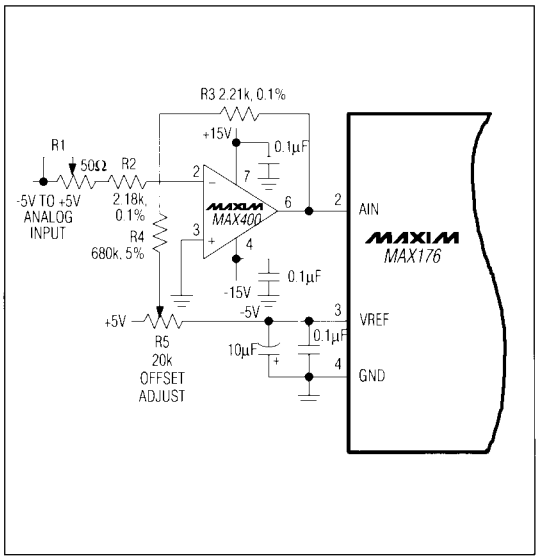

Figure 10. Inverting Offset and Full-Scale Adjustment

This circuit is configured to operate in continuous-conversion mode. However, it may be modified for burst-mode operation by controlling the shift register RCK inputs with a signal other than convert start. When continuous-conversion mode is used, convert start must go high at the 14th falling clock edge to prevent shifting of data past the shift register outputs shown; convert start's rising edge latches the data that has been serially loaded into the two 74HC595 shift registers. Clock frequency is restricted because of the clock-to-data delay (see *Electrical Characteristics*); the correct data must be present at the SER pin when clock rising edges strobe the data into the shift registers. The clock frequency is thus limited to 3.3MHz for the commercial version of the MAX176, unless the clock signal to the shift registers is delayed or inverted. This limitation also accounts for the 20ns shift-register setup time. Note that for clock frequencies above 2.5MHz, each conversion requires 15 clock cycles or more to allow sufficient T/H acquisition time. If 15 or 16 clock pulses occur between each convert start pulse, this circuit still functions, but the data at the shift register outputs is shifted up one or two positions, respectively, so that the MSB appears at the top shift register's QE or QF output. Figure 11b illustrates the timing for this shift register circuit.

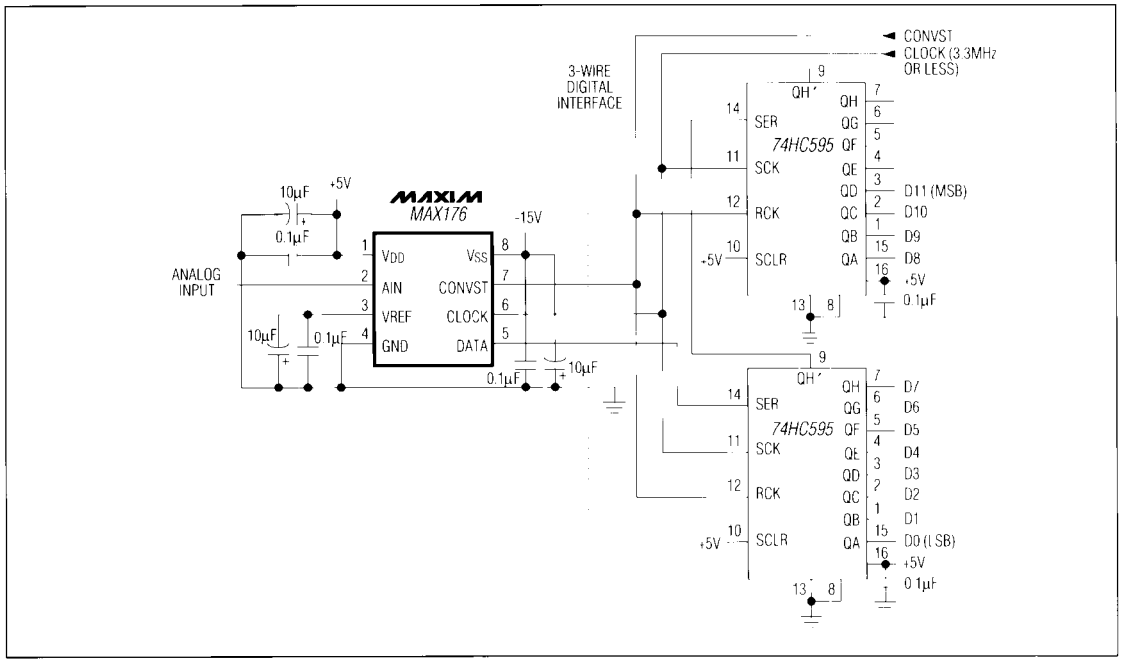

Figure 11a. 3-Wire Interface to Parallel Port

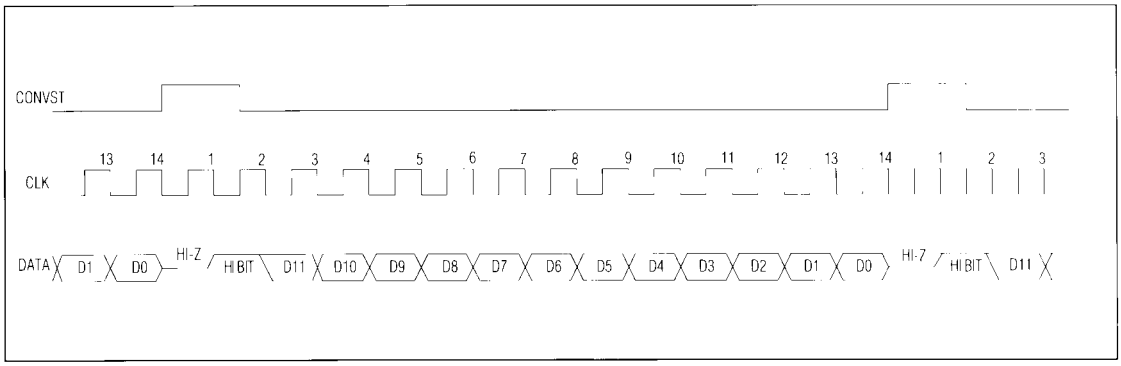

Figure 11b. Timing for Serial-to-Parallel Converter

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

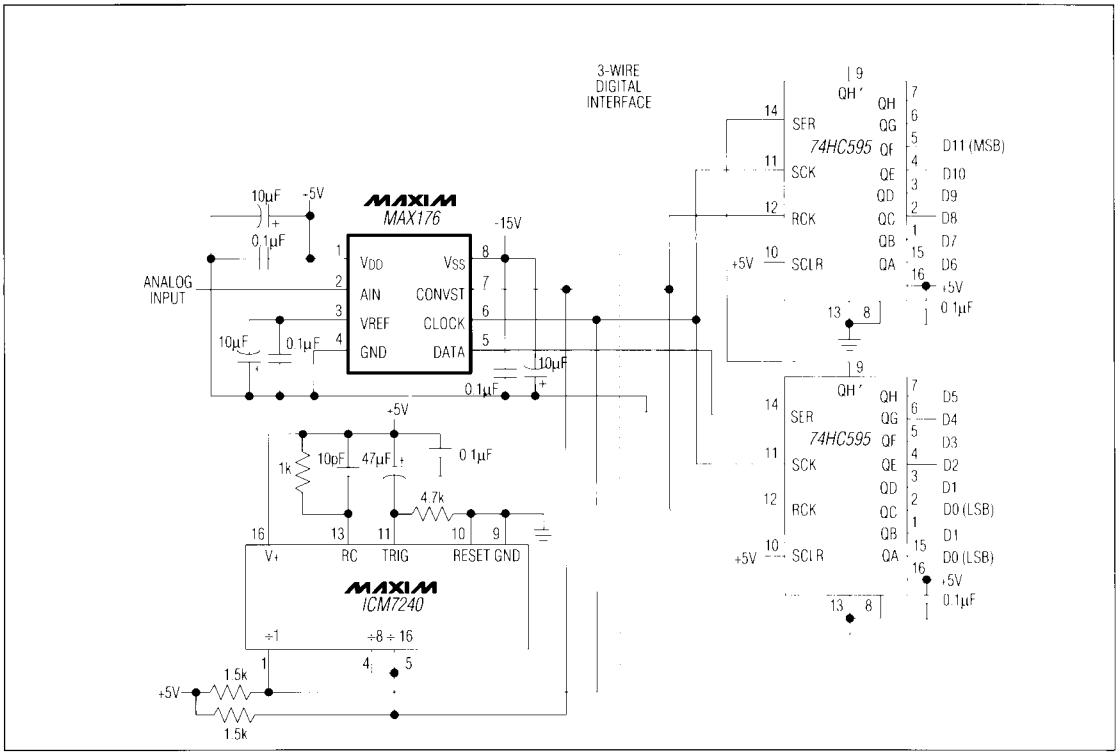

Figure 12. 3-Wire Interface to Parallel Port Using Timer Chip

In Figure 12's circuit, the clock and convert start signals are generated by an ICM7240 timer/converter, allowing stand-alone MAX176 operation. The ICM7240 provides a convert start pulse for every 16 clock cycles it generates. Due to the ICM7240's upper frequency limit, this circuit's clock frequency is 1MHz maximum. If CONVST is capacitively loaded with greater than 80pF, the maximum allowable convert start rise-time specification might be exceeded. Using a logic buffer between the ICM7240 and CONVST of the MAX176 eliminates this problem. Check that none of the timing characteristics are violated when longer rise times occur due to capacitive loading of CONVST or CLOCK.

MAX176 with Opto-Isolators

Transducer outputs often require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity, or bridge large differences in ground potential. Isolation amplifiers typically used for accomplishing this are expensive. In cases where the signal is eventually converted to a digital form, it is cost effective to isolate the input using opto-isolaters in a serial data link. The MAX176 is ideal in this application because it includes both T/H amplifier and voltage reference, and because of its low power consumption (Figure 13a). The ADC results are transmitted across a 1500V isolation barrier provided by three 6N136 opto-isolators. Note that isolated power must be provided to the converter and the isolated side of the opto-isolators. 74HC595 three-state shift registers are used to construct a 12-bit parallel data output. (For those who prefer even greater space savings and do not need a T/H, Maxim's MAX171 combines the MAX170, three opto-isolators, and load resistors in a 16-pin DIP package.)

Figure 13b shows the timing diagram for this application. Conversion speed is limited by the delay through the opto-isolators. With a 140kHz clock, conversion time is 100µs.

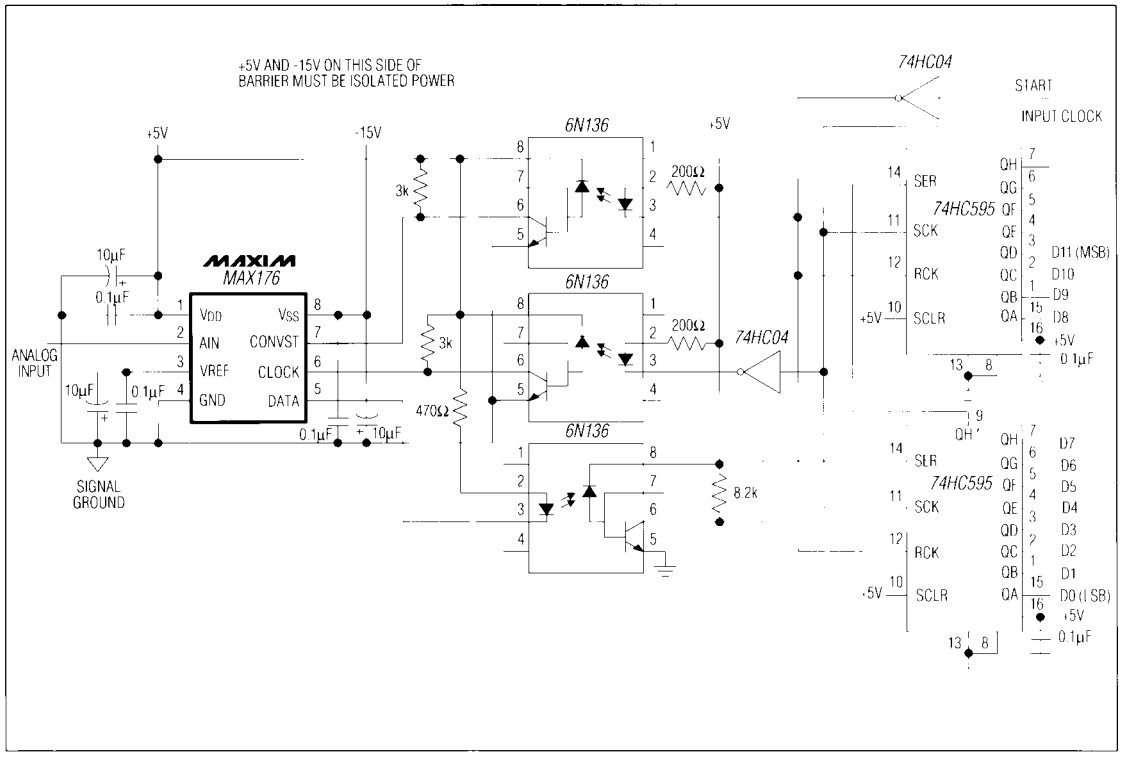

Figure 13a. 12-Bit Isolated A/D Converter – 100µs Conversion Time

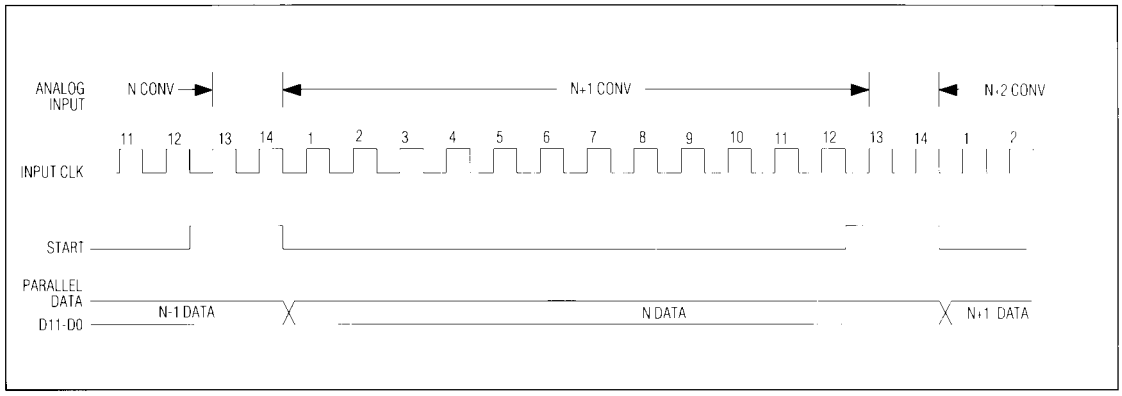

Figure 13b. Timing for Isolated A/D Interface

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

In this circuit, the 74HC04 inverters must sink the current flowing through the opto-isolators. However, maximum V_{OL} for these parts is specified for lighter sink currents. If the 74HC04 output resistance is calculated by dividing V_{OL} max by the sink current used for this specification (this resistance is valid up to about 30mA of sink current), the resulting voltage can be calculated when the part sinks these higher currents. The same procedure can be applied to the MAX176 DATA output - the calculated maximum resistance (250Ω) is valid up to 10mA of sink current.

The rise time of the signal applied to the MAX176's CONVST pin must be less than 100ns (see *Electrical Characteristics*). Because it has an open-collector output, the rise time of CONVST's opto-isolator is a function of its pull-up resistor and any stray capacitance. Minimize this stray capacitance to ensure a fast enough rise time.

Another consideration is the delays through this circuit due primarily to the opto-isolators. The largest delay is between input clock and the appearance of data at the lower shift register's SER pin. It is caused by delay through the 74HC04, the MAX176's clock-to-data delay (see *Electrical Characteristics*), and the delay from two opto-isolators. This delay must be less than one clock period (by the setup time of the 74HC595), and it determines the fastest allowable clock speed for the circuit.

Finally, noise pickup on the relatively slow opto-coupler transitions can cause false triggering at the converter's edge-sensitive CONVST input. To avoid this problem, set the rising edge of start (falling edge of convert start) to occur when the CONVST input ignores transitions (i.e. before clock's 13th falling edge). Start's falling edge triggers the next conversion, and also causes the previous conversion's results to appear at the parallel data outputs.

Physical Layout

For best system performance, use printed circuit boards for the MAX176 - wire-wrap boards are not recommended. The board layout should ensure that digital and analog signal lines are kept separate, and that digital lines do not pass underneath the MAX176 package.

Grounding

Figure 14 shows the recommended system ground connections. A single-point analog STAR ground should be established at the MAX176 GND pin. All analog-circuitry grounds should be connected to this STAR ground. The ground return to the power supply from STAR ground should be low impedance for noise-free operation. Digital-circuitry grounds must be connected to the digital supply common. All ground pins of the small-outline version of the MAX176 should connect to the STAR ground.

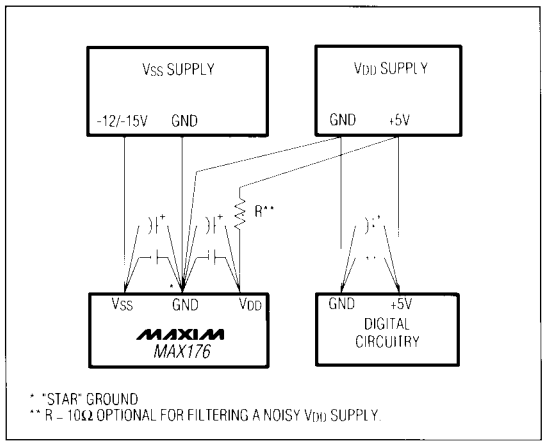

Figure 14. Power-Supply Grounding

Power-Supply Bypassing

The MAX176's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog STAR ground with 0.1µF and 10µF capacitors with minimum lead length for supply-noise rejection. If the +5V power supply is very noisy, connect a small resistor (10Ω) to filter external noise (Figure 14).

Internal Voltage Reference

The MAX176 has an on-chip reference with a buffered and temperature-compensated buried-zener diode, laser-trimmed to -5V ±0.4%. Its output is connected to the VREF pin and also drives the internal DAC. This output can be used as a reference voltage source for other components, and can sink up to 5mA.

Decouple VREF with a low-ESR 10µF capacitor in parallel with a 0.1µF capacitor.

Driving the Analog Input

The input signal connections to AIN and GND should be as short as possible to minimize noise pickup. If the leads must be long, use shielded cables. The ADC analog input range is nominally ±5V. However, the analog input can be driven to ±15V with no damage to the device.

Because the MAX176 includes a T/H, the drive requirements of an op amp connected to AIN are less critical than those for a successive-approximation ADC without a T/H. This amplifier, however, must provide current with an amplitude dependent on the signal level at AIN (Figure 2). Also, the amplifier bandwidth should be sufficient to handle the frequency of the signal applied to it. The MAX400 and OP07 work well at lower frequencies. For higher-frequency operation, the MAX427 and OP27 are suitable choices. The allowed input frequency range is limited by the 250ksps sample rate of the MAX176. Thus, the maximum sinusoidal input frequency allowed is 125kHz. Higher-frequency signals cause aliasing problems unless undersampling techniques are used.

Dynamic Performance

High-speed sampling capability and 250kHz throughput make the MAX176 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency. Figure 15 shows an FFT plot.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL) and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (S/(N + D) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other A/D output signals. The output band is limited to frequencies above DC and below one-half the A/D sample (conversion) rate. This includes distortion as well as noise components.

The theoretical minimum A/D noise is cause by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can, therefore, do no better than 74dB.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution, or effective number of bits, the ADC provides: N = (SNR - 1.76)/6.02.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic (or spurious) noise is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

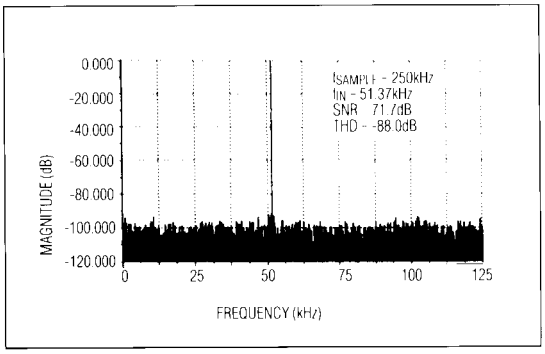

Figure 15. MAX176 FFT Plot

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX176AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX176BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX176AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX176BEWE	-40°C to +85°C	16 Wide SO	±1
MAX176AMJA	-55°C to +125°C	8 CERDIP**	±3/4
MAX176BMJA	-55°C to +125°C	8 CERDIP**	±1

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topography