



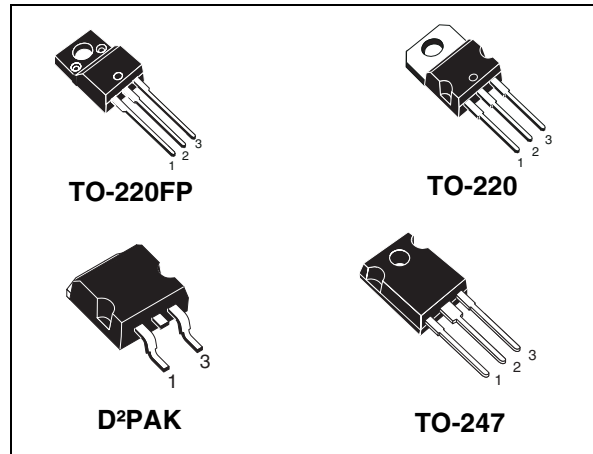
# STB28NM50N, STF28NM50N STP28NM50N, STW28NM50N

N-channel 500 V, 0.135  $\Omega$ , 21 A D<sup>2</sup>PAK, TO-220, TO-220FP, TO-247  
MDmesh™ II Power MOSFET

## Features

Order codes	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB28NM50N	550 V	< 0.158 $\Omega$	21 A
STF28NM50N			
STP28NM50N			
STW28NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

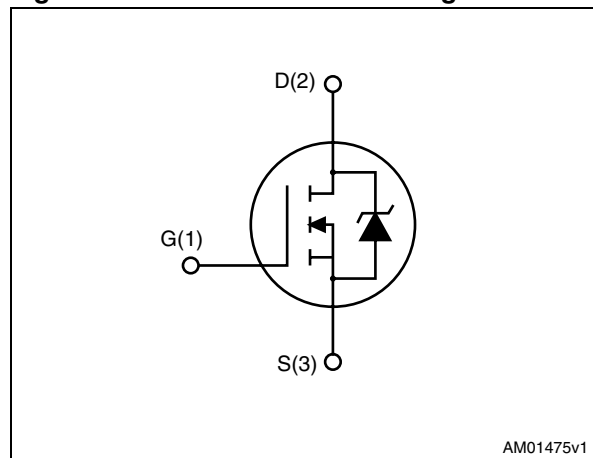


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB28NM50N	28NM50N	D <sup>2</sup> PAK	Tape and reel
STF28NM50N		TO-220FP	Tube
STP28NM50N		TO-220	
STW28NM50N		TO-247	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value				Unit
		TO-220	D <sup>2</sup> PAK	TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	500				V
V <sub>GS</sub>	Gate- source voltage	± 25				V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	21		21 <sup>(1)</sup>		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	13		13 <sup>(1)</sup>		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	84		84 <sup>(1)</sup>		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	150		35		W
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)			2500		V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15				V/ns
T <sub>stg</sub>	Storage temperature	- 55 to 150				°C
T <sub>j</sub>	Max. operating junction temperature	150				°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- I<sub>SD</sub> ≤ 21 A, di/dt ≤ 400 A/μs, V<sub>DS peak</sub> ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		TO-220	D <sup>2</sup> PAK	TO-247	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.83			3.6	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5		50	62.5	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max		30			°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300		300		°C

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> Max)	7.5	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	300	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}, @125^{\circ}C$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 10.5 \text{ A}$		0.135	0.158	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	1735	-	pF
$C_{oss}$	Output capacitance			122		pF
$C_{rss}$	Reverse transfer capacitance			4.3		pF
$C_{oss(eq)}^{(1)}$	Equivalent output capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 50 \text{ V}$	-	418	-	pF
$Q_g$	Total gate charge	$V_{DD} = 400 \text{ V}, I_D = 21 \text{ A},$ $V_{GS} = 10 \text{ V},$ (see <a href="#">Figure 19</a> )	-	50	-	nC
$Q_{gs}$	Gate-source charge			9.5		nC
$Q_{gd}$	Gate-drain charge			25		nC
$R_g$	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain	-	2.7	-	$\Omega$

1.  $C_{oss(eq)}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$ , $I_D = 10.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )		13.6		ns	
$t_r$	Rise time			19		ns	
$t_{d(off)}$	Turn-off delay time				62	-	ns
$t_f$	Fall time				52		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 21\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 400\text{ V}$ (see <a href="#">Figure 23</a> )	-	326		ns
$Q_{rr}$	Reverse recovery charge			5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			30		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 21\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 400\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 23</a> )	-	376		ns
$Q_{rr}$	Reverse recovery charge			6.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			33.2		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D<sup>2</sup>PAK

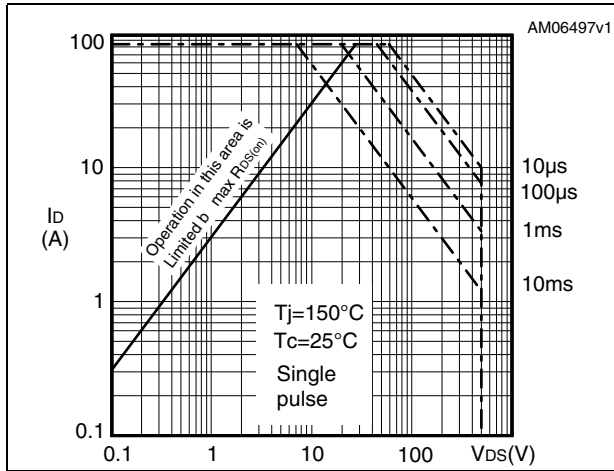


Figure 3. Thermal impedance for TO-220, D<sup>2</sup>PAK

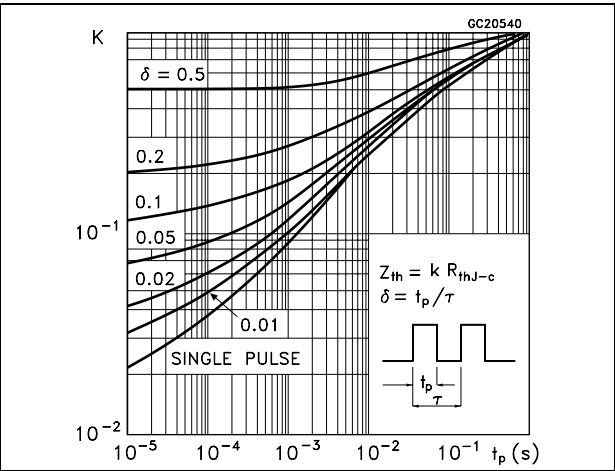


Figure 4. Safe operating area for TO-220FP

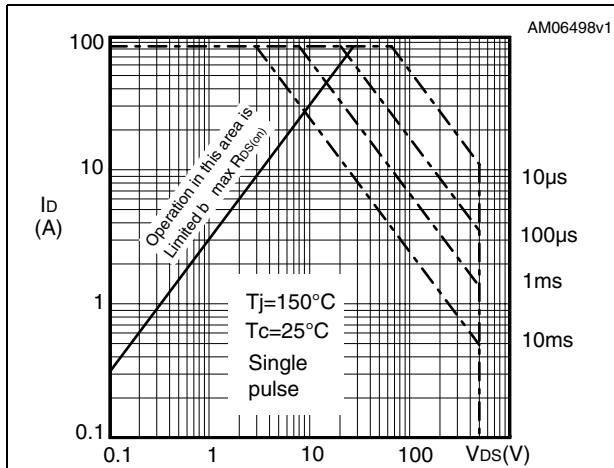


Figure 5. Thermal impedance for TO-220FP

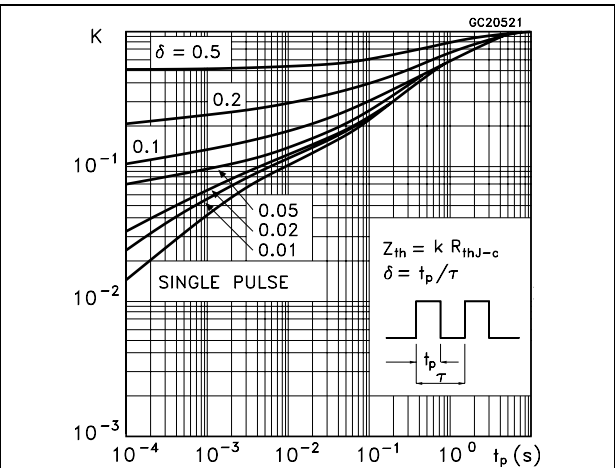


Figure 6. Safe operating area for TO-247

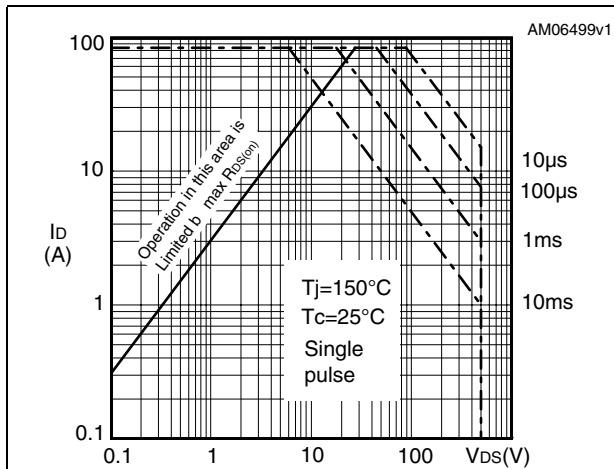


Figure 7. Thermal impedance for TO-247

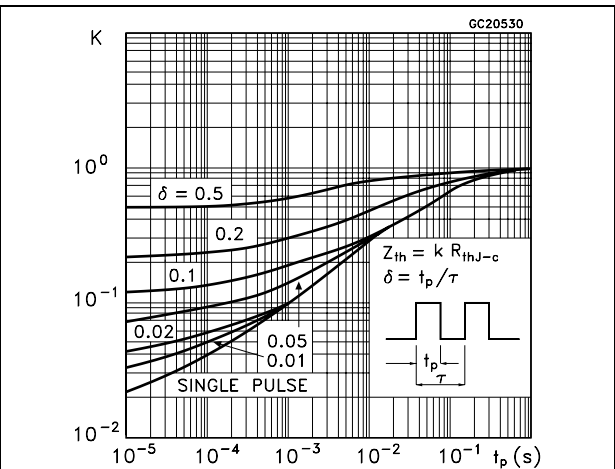


Figure 8. Output characteristics

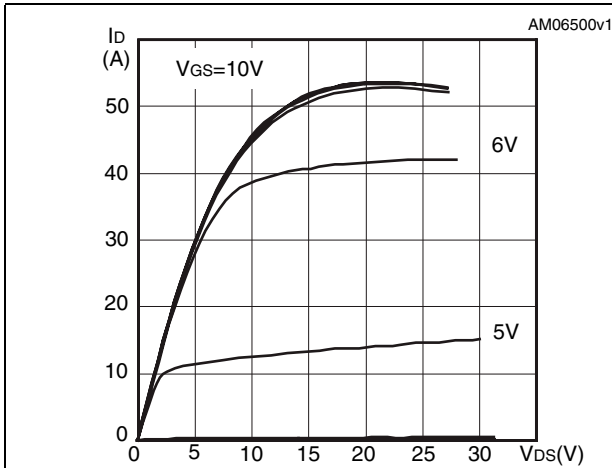


Figure 9. Transfer characteristics

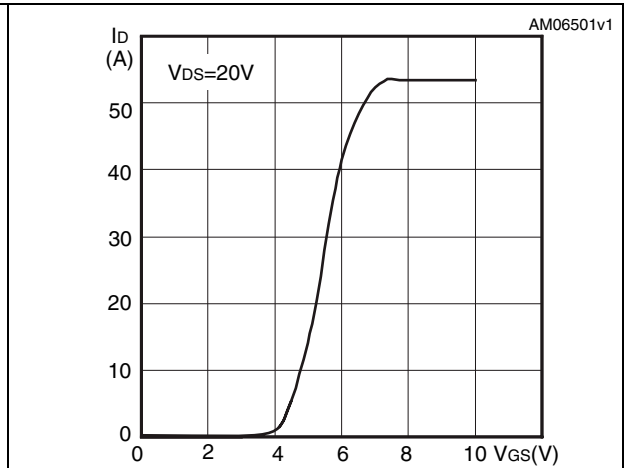


Figure 10. Gate charge vs gate-source voltage Figure 11. Static drain-source on resistance

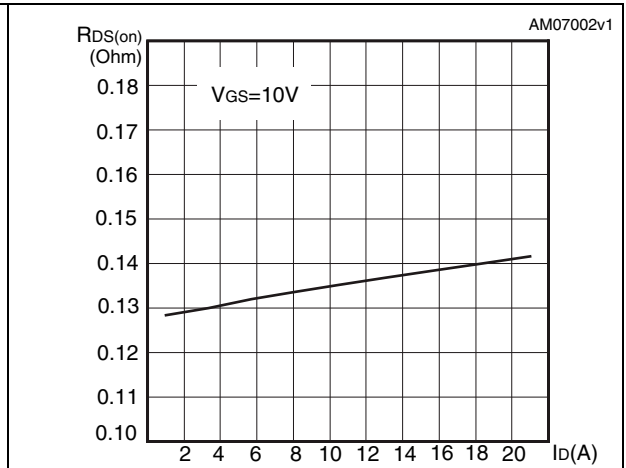
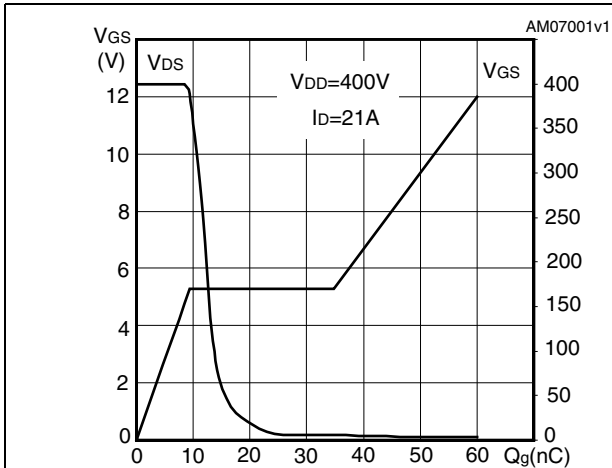


Figure 12. Capacitance variations

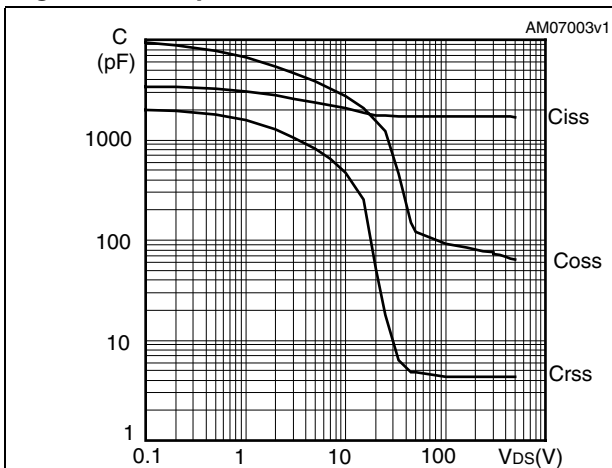


Figure 13. Output capacitance stored energy

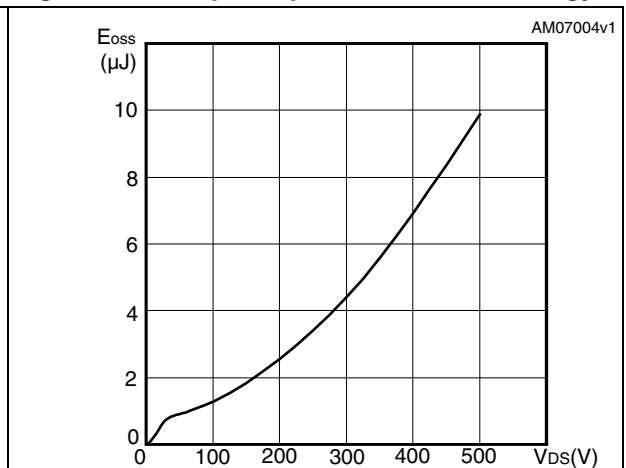


Figure 14. Normalized gate threshold voltage vs temperature

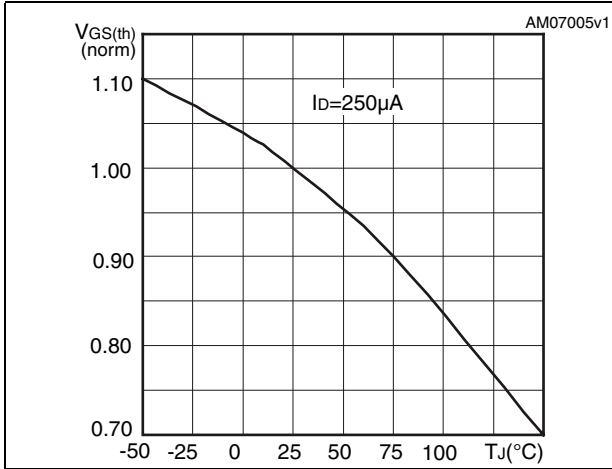


Figure 15. Normalized on resistance vs temperature

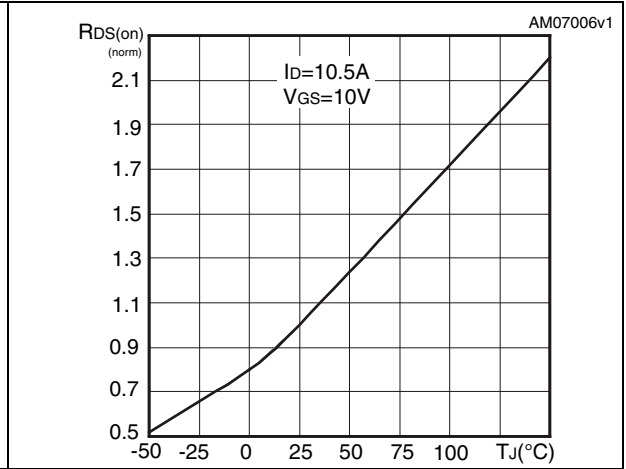


Figure 16. Normalized B<sub>V</sub>DSS vs temperature

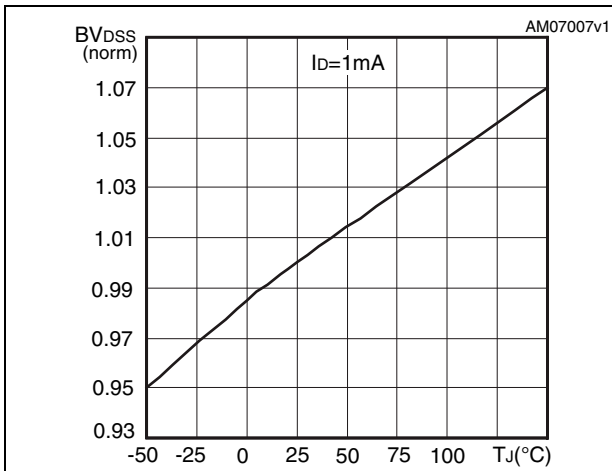
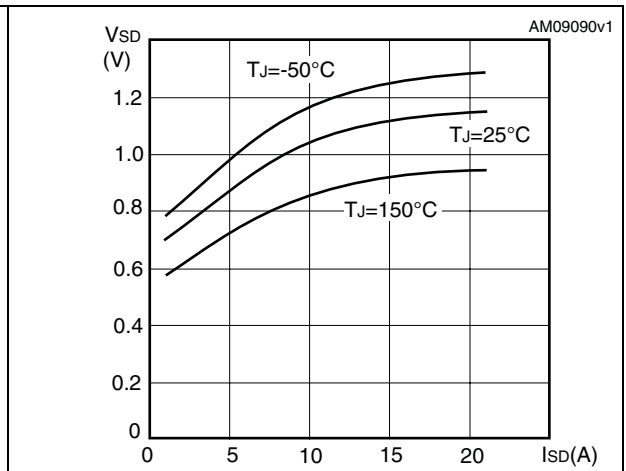


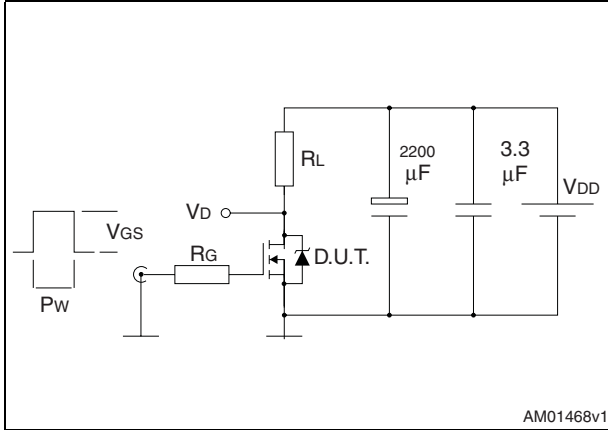
Figure 17. Source-drain diode forward characteristics





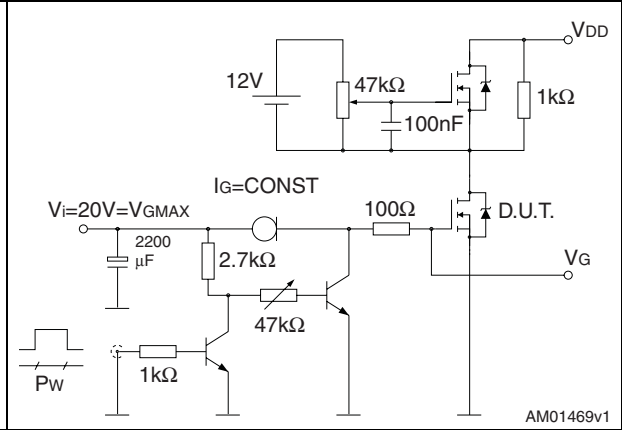
### 3 Test circuits

**Figure 18. Switching times test circuit for resistive load**



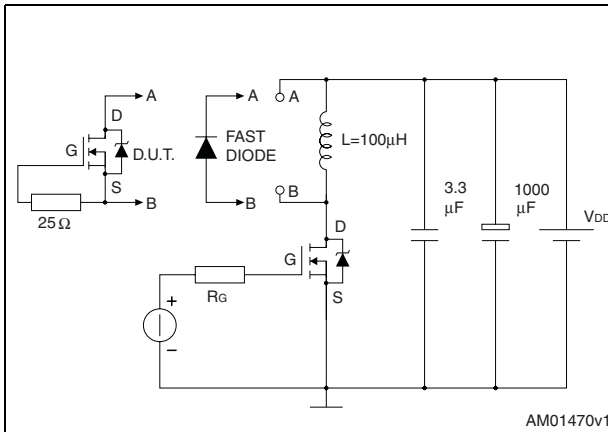
AM01468v1

**Figure 19. Gate charge test circuit**



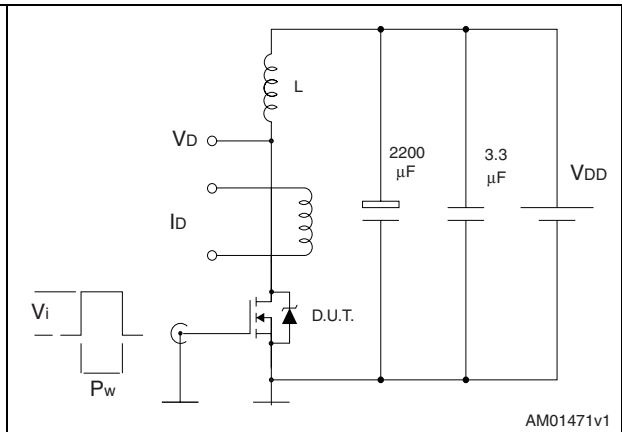
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**Figure 20. Test circuit for inductive load switching and diode recovery times**



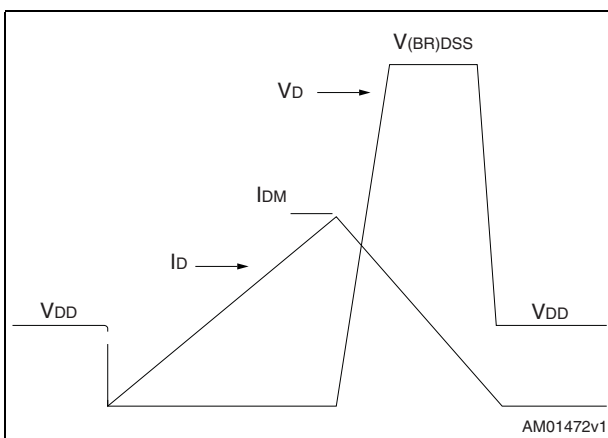
AM01470v1

**Figure 21. Unclamped inductive load test circuit**



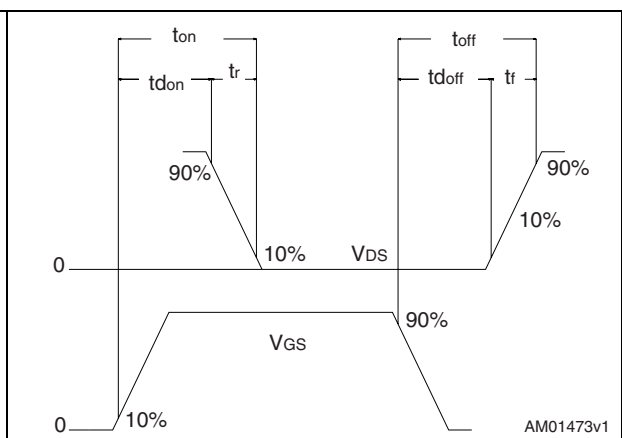
AM01471v1

**Figure 22. Unclamped inductive waveform**



AM01472v1

**Figure 23. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing

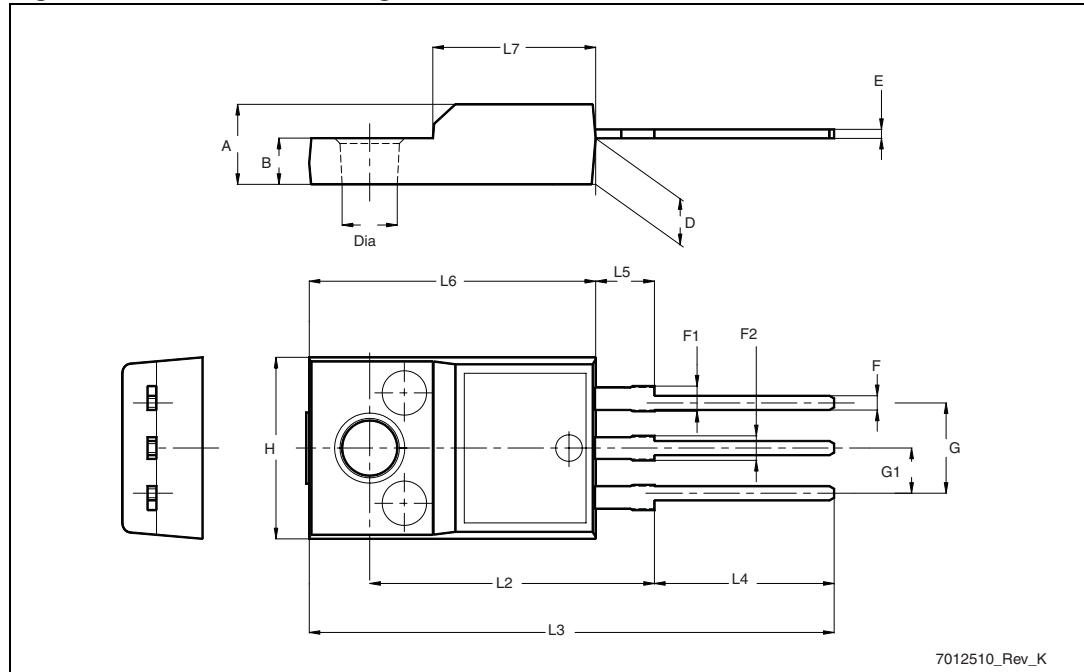


Table 10. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 25. D<sup>2</sup>PAK footprint<sup>(a)</sup>

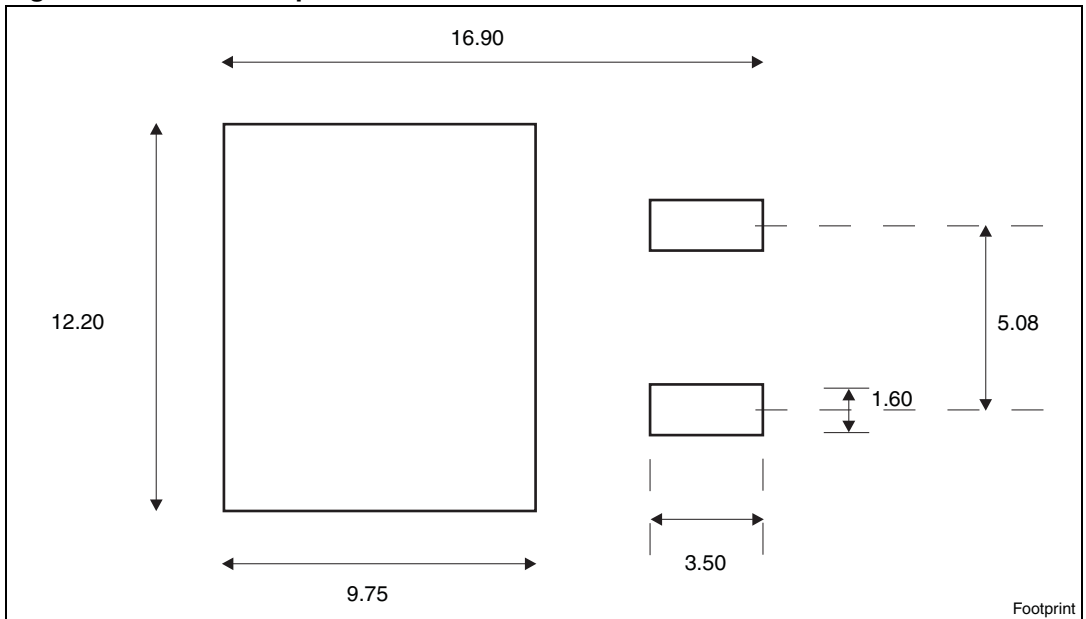
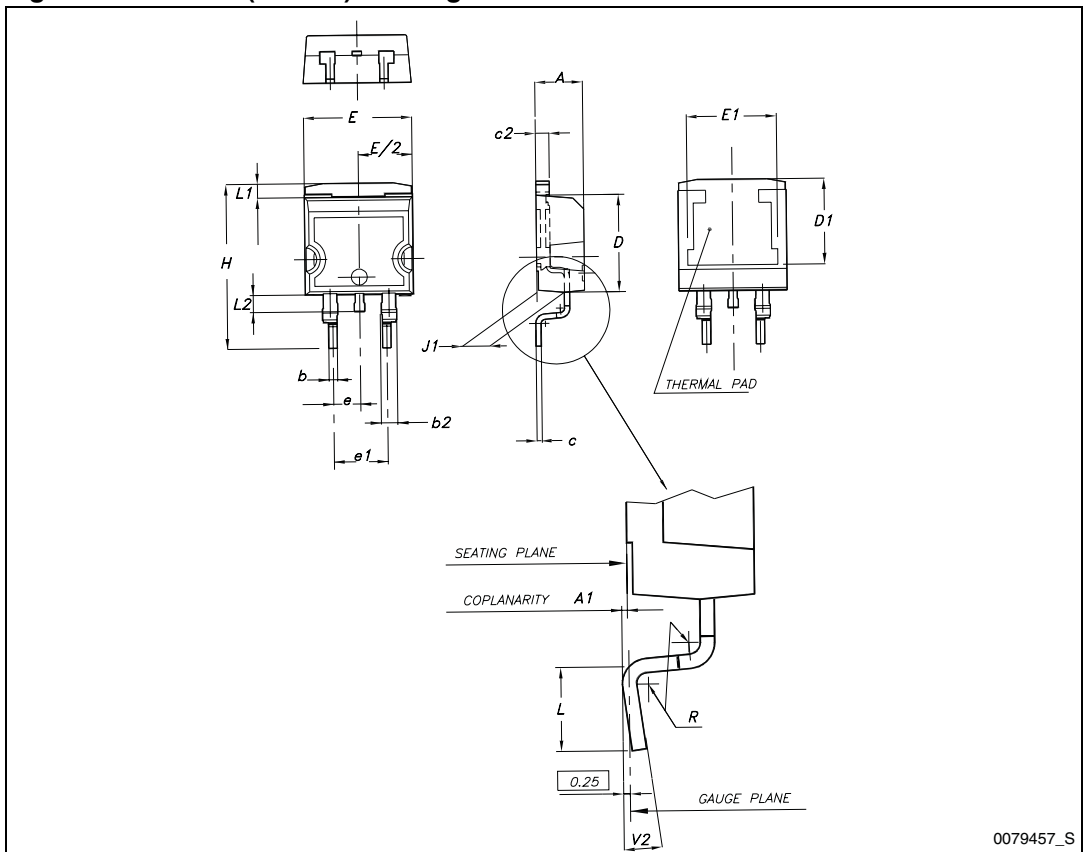


Figure 26. D<sup>2</sup>PAK (TO-263) drawing



a. All dimension are in millimeters

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

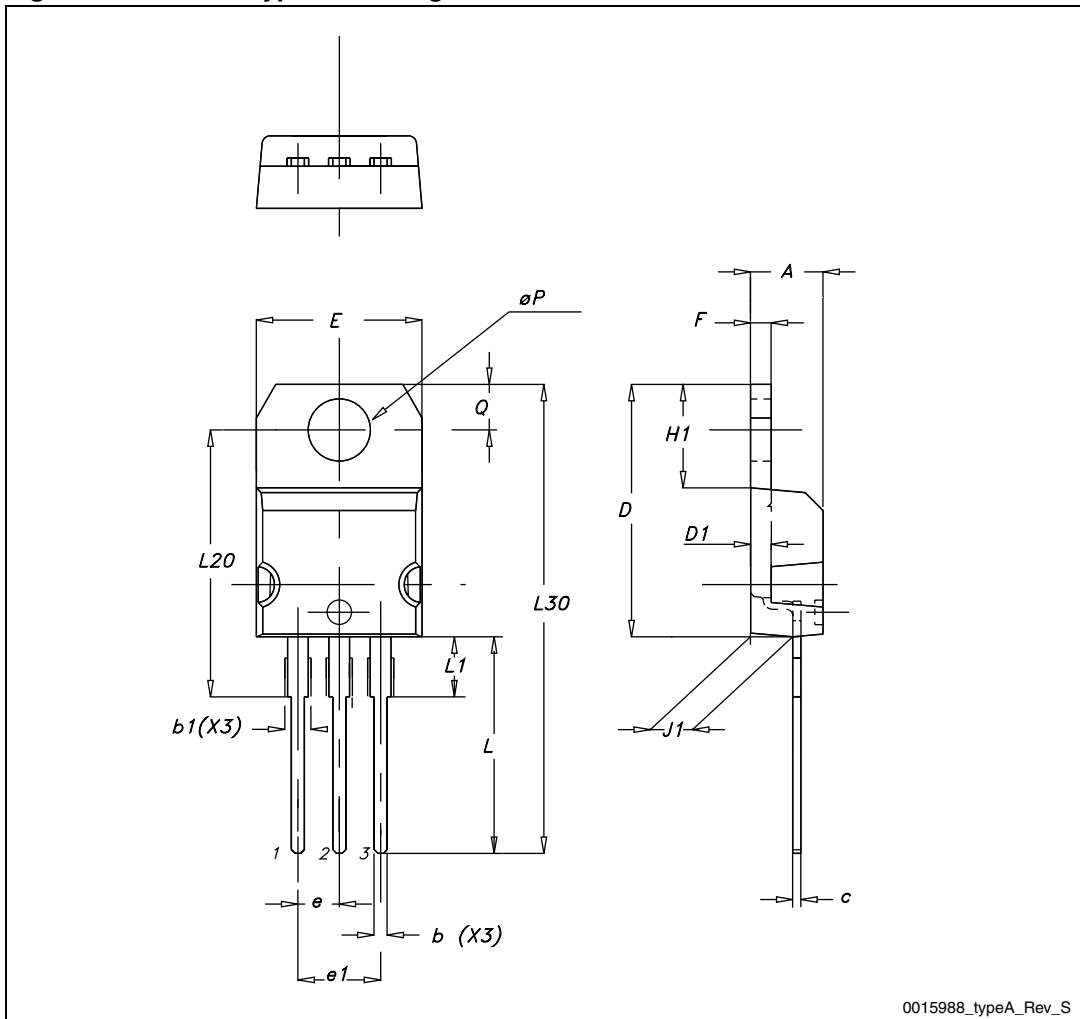
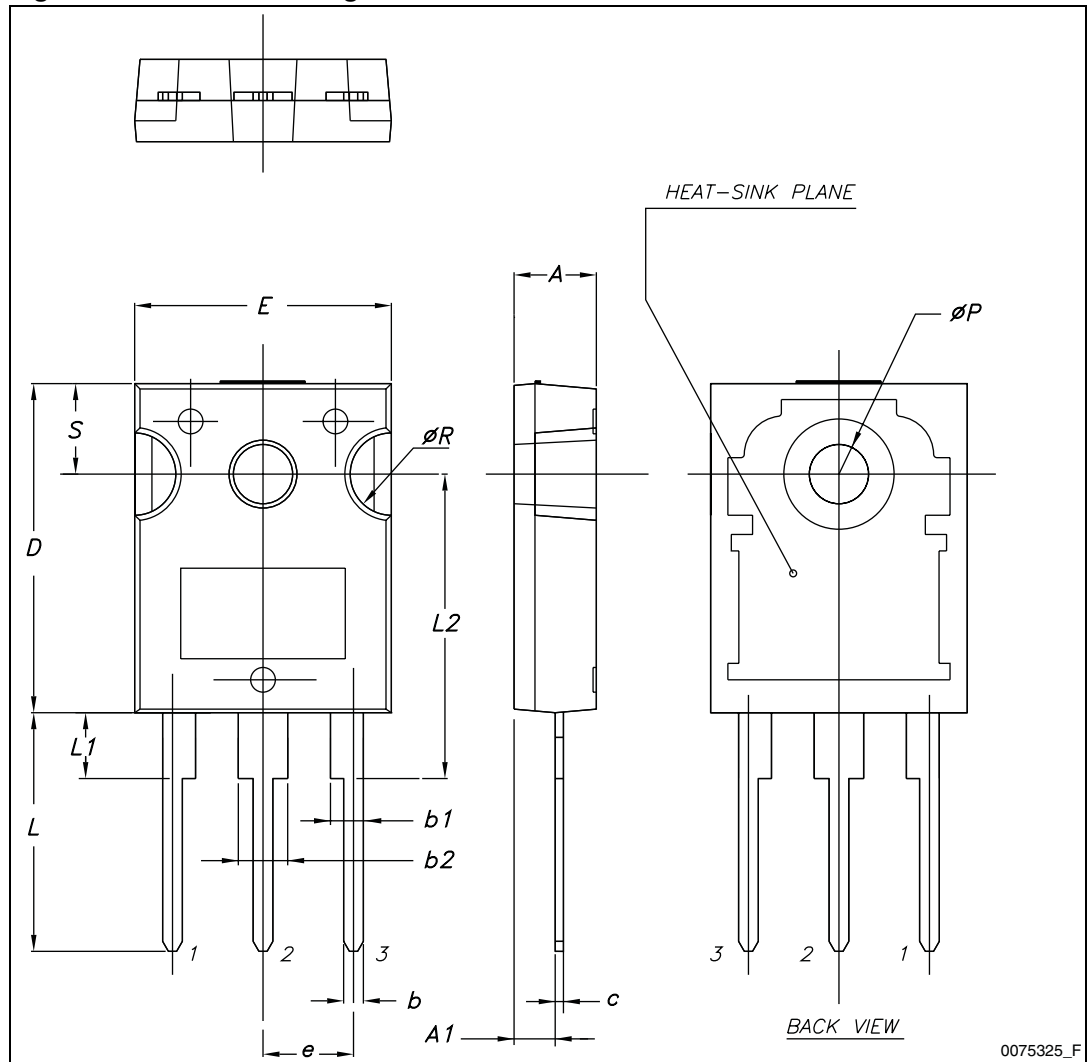


Table 12. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	



Figure 28. TO-247 drawing



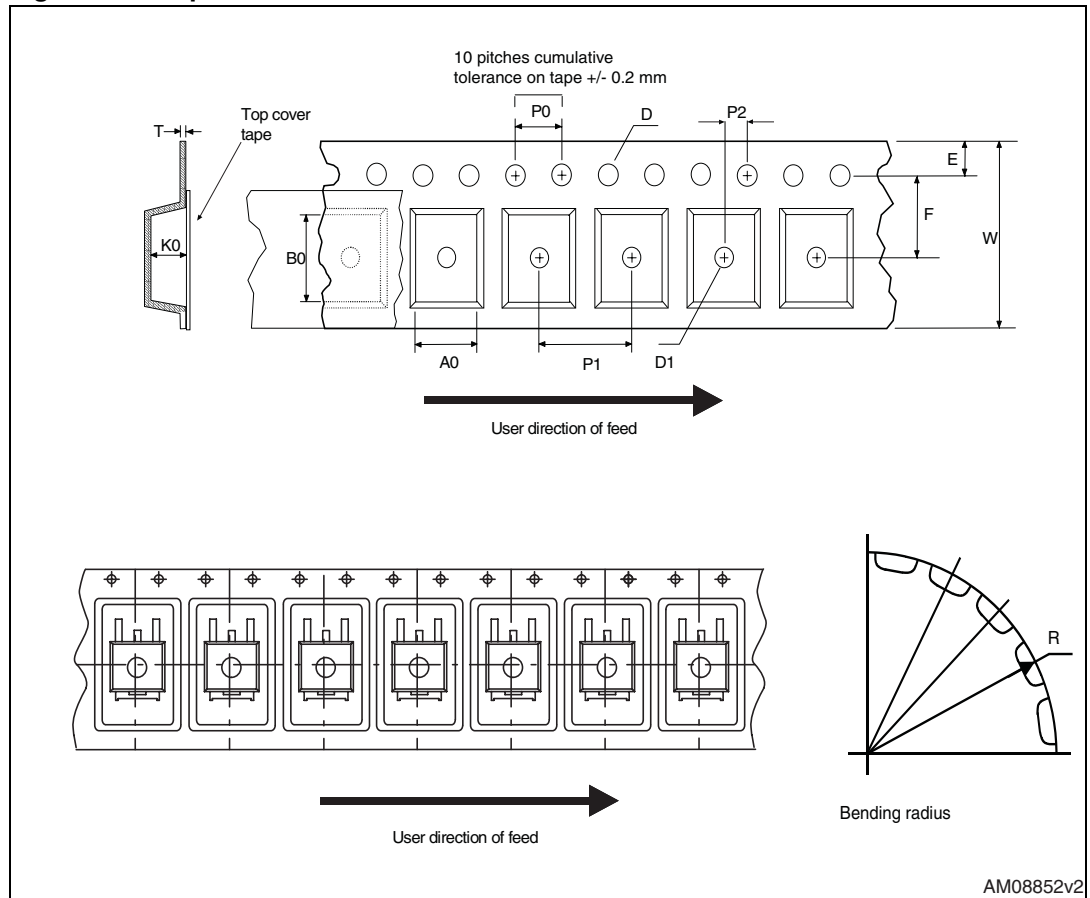
0075325\_F

## 5 Packaging mechanical data

Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

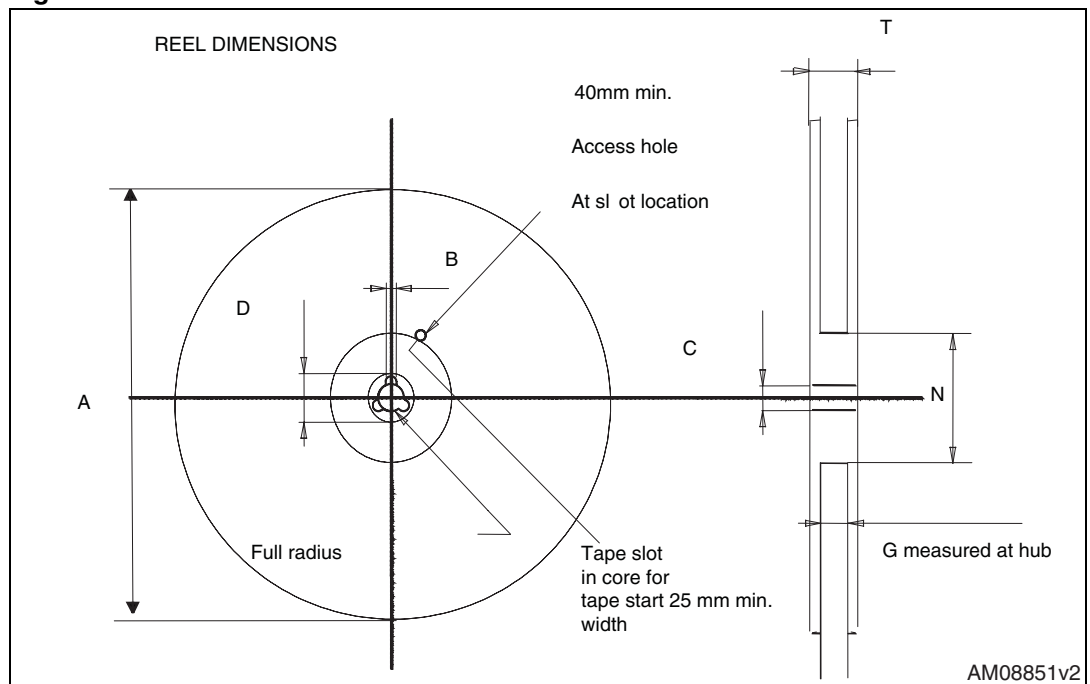
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 29. Tape



AM08852v2

Figure 30. Reel



AM08851v2

## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-Jul-2010	1	First release.
27-Jun-2011	2	<ul style="list-style-type: none"><li>– Updated <a href="#">Table 6: Dynamic</a>.</li><li>– Updated <a href="#">Section 2.1: Electrical characteristics (curves)</a>.</li></ul>

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