Sink Only USB Type-C PD Controller

General Description

The RT1719 is a USB Type-C controller that complies with the latest USB Type-C and PD standards. It does the USB Type-C detection including attach and orientation. The RT1719 integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power. The BMC PD block supports the full Type-C specification.

Ordering Information

RT1719□□

- Package Type
  QW : WQFN-20L 3.5x3.5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

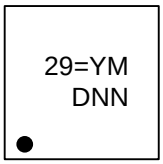
Features

- **PD 2.0 and 3.0 Compatible**
- **Attach/Detach Detection as Device**
- **Current Capability Definition**
- **Data Role Support**
- **Dead Battery Support**
- **Simple I^2C Interface with AP or EC**
- **BIST Mode Supported**

Applications

- Cameras
- Printers
- Toys
- Drones
- Handheld Devices
- Sink Devices

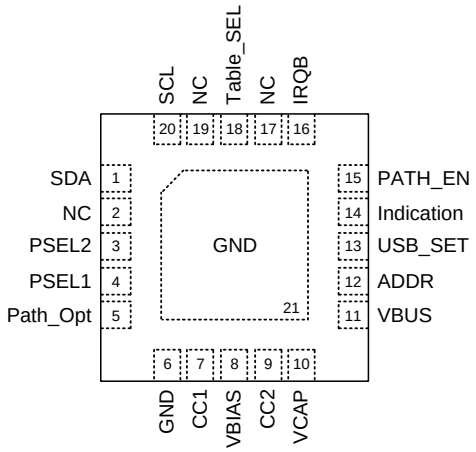
Marking Information



29= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

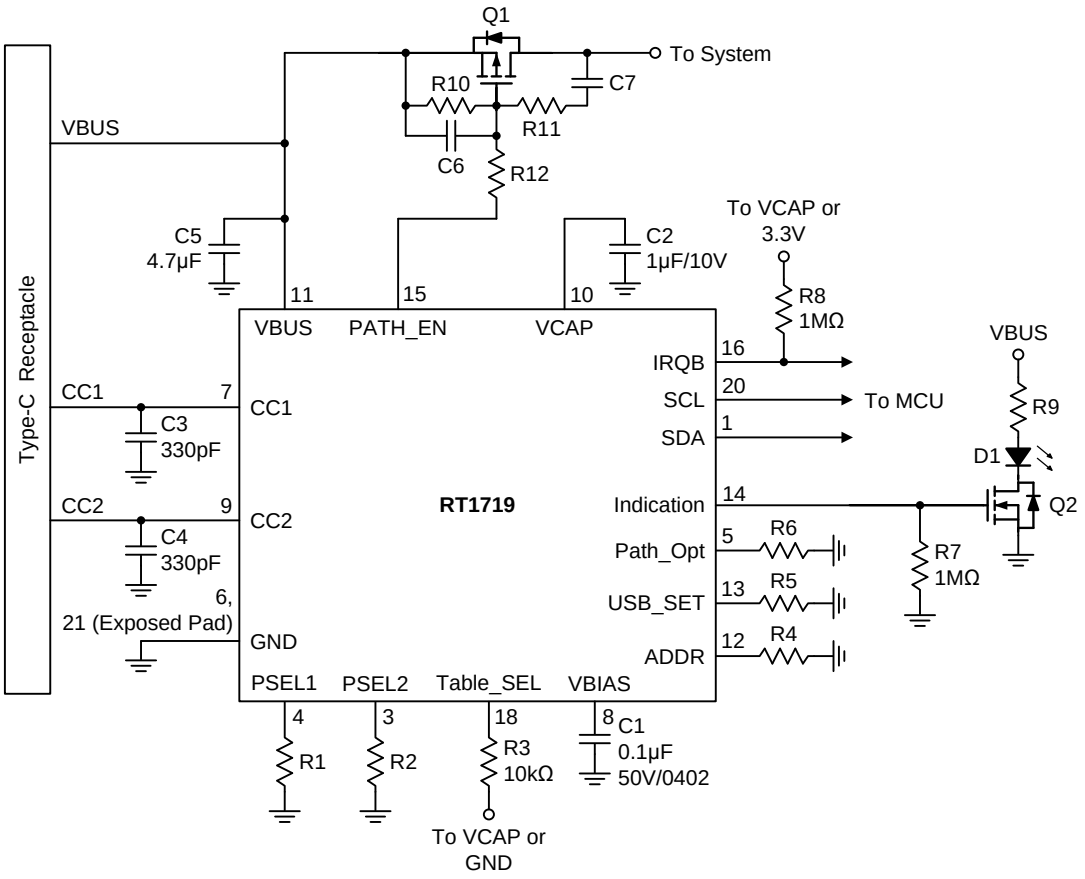


WQFN-20L 3.5x3.5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SDA	I^2C serial data signal to be connected to the I^2C master. Please connect 1kΩ to GND if I^2C is not used.
2, 17, 19	NC	No internal connection.
3	PSEL2	Power selection 2 for power data object.
4	PSEL1	Power selection 1 for power data object.
5	Path_Opt	Power path option.
6, 21 (Exposed Pad)	GND	Ground pin. The exposed pad must be connected to GND and be well soldered to a large copper PCB for maximum power dissipation.
7	CC1	Type-C connector configuration channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
8	VBIAS	Put a 0.1μF (0402/50V) capacitor. This pin cannot drive external load.
9	CC2	Type-C connector configuration channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
10	VCAP	Put a 1μF capacitor. This pin cannot drive external load.
11	VBUS	VBUS input pin for attach/detach detection and supply input.
12	ADDR	Address selection node when used with multiple Type-C ports.
13	USB_SET	USB ability setting node.
14	Indication	The power data object does not match the indication pin.
15	PATH_EN	Open-drain gate driver. which may be used to drive an PMOS.
16	IRQB	Interrupt output, active-low open-drain, to prompt the processor to read the registers. Please connect 1kΩ to GND if IRQB is not used.
18	Table_SEL	Power data object table selection
20	SCL	I^2C serial clock signal to be connected to the I^2C master. Please connect 1kΩ to GND if I^2C is not used.

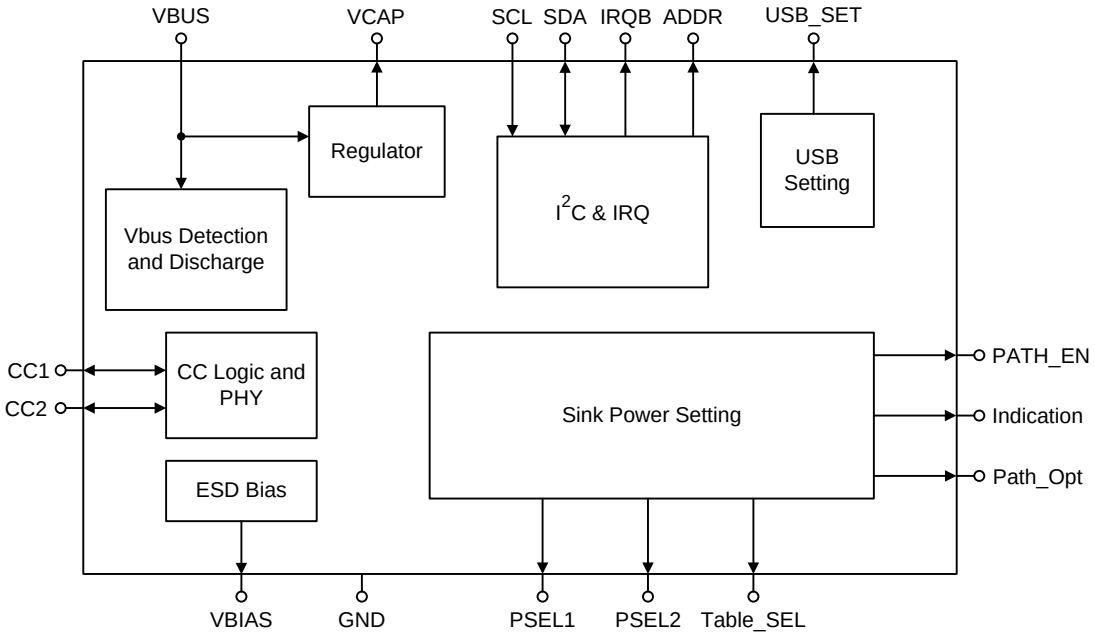
Typical Application Circuit



Note :

1. R1, R2, R4, R5 and R6 depend on system design.
2. R9 depends on the D1 at VBUS = 5V.
3. R10, R11, R12, C6 and C7 depend on the soft-start for power path.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VBUS ---------- –0.3V to 28V
- CC1, CC2, PATH_EN,VBIAS ---------- –0.3V to 24V
- VCAP, Indication, Path_Opt, USB_SET, ADDR ---------- –0.3V to 6V
- SDA, SCL, IRQB, PSEL1, PSEL2, Table_SEL ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-20L 3.5x3.5 ---------- 3.5W
- Package Thermal Resistance (Note 2)

  WQFN-20L 3.5x3.5, θ_{JA} ---------- 28.5°C/W

  WQFN-20L 3.5x3.5, θ_{JC} ---------- 7.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model)

  VBUS, CC1, CC2 ---------- ±4kV

  Other Pins ---------- ±2kV

  VBUS, CC1, CC2 (IEC 61000-4-2 Contact Discharge) ---------- ±8kV

  VBUS, CC1, CC2 (IEC 61000-4-2 Air Discharge) ---------- ±15kV

  VBUS, CC1, CC2 (IEC 61000-4-5 Surge) ---------- ±28V

Recommended Operating Conditions (Note 4)

- VBUS Input Voltage ---------- 3V to 22V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Common Normative Signaling Requirements						
Bit Rate	$f_{BitRate}$	V_{BUS} = 3V to 22V	270	300	330	kbps
Common Normative Signaling Requirements for Transmitter						
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate	$p_{BitRate}$	V_{BUS} = 3V to 22V	--	--	0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble	$t_{InterFrameGap}$	V_{BUS} = 3V to 22V	25	--	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line	$t_{StartDrive}$	V_{BUS} = 3V to 22V	–1	--	1	μs
BMC Common Normative Requirements						
Time to cease driving the line after the end of the last bit of the Frame	$t_{EndDriveBMC}$	V_{BUS} = 3V to 22V	--	--	23	ms
Fall Time	t_{Fall}	V_{BUS} = 3V to 22V 10% and 90% amplitude points, minimum is under an unloaded condition.	300	--	--	ns
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC}$	V_{BUS} = 3V to 22V	1	--	--	ms
Rise Time	t_{Rise}	V_{BUS} = 3V to 22V 10% and 90% amplitude points, minimum is under an unloaded condition.	300	--	--	ns
Voltage Swing	V_{Swing}	V_{BUS} = 3V to 22V	1.05	1.125	1.2	V
Transmitter Output Impedance	z_{Driver}	V_{BUS} = 3V to 22V	33	--	75	Ω
Receiver Input Impedance	z_{BmcRx}	V_{BUS} = 3V to 22V	1	--	--	MΩ
Power Consumption						
Idle Mode	I_{Idle_Sink}	V_{BUS} = 3V to 22V. I^2C and IRQB are not used.	--	130	180	μA
		V_{BUS} = 3V to 22V. I^2C and IRQB pull high voltage is 3.3V.	--	160	300	
BIST Mode	I_{BIST}	Sink current consumption in cable attached and CC send BIST V_{BUS} = 3V to 22V. I^2C and IRQB pull high voltage is 3.3V.	--	5.5	6.5	mA
Type-C Port Control						
UFP Rd	Rd	V_{BUS} = 3V to 22V	4.59	5.10	5.61	kΩ
UFP Pull-Down Voltage in Dead Battery under DFP 80μA	$V_{DB\_80\mu A}$		0.25	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 180μA	$V_{DB\_180\mu A}$		0.45	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 330μA	$V_{DB\_330\mu A}$		0.85	--	2.45	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Port Control						
VBUS High Voltage Bound for 20V	V_{HV20}		21.85	23	24.15	V
VBUS Low Voltage Bound for 20V	V_{LV20}		15.975	16.9	17.75	V
VBUS High Voltage Bound for 15V	V_{HV15}		16.15	17	17.85	V
VBUS Low Voltage Bound for 15V	V_{LV15}		11.7	12.35	13	V
VBUS High Voltage Bound for 12V	V_{HV12}		13.3	14	14.7	V
VBUS Low Voltage Bound for 12V	V_{LV12}		9.135	9.6	10.18	V
VBUS High Voltage Bound for 9V	V_{HV09}		9.975	10.5	11.025	V
VBUS Low Voltage Bound for 9V	V_{LV09}		6.57	6.93	7.36	V
VBUS High Voltage Bound for 5V	V_{HV05}		5.7	6	6.3	V
VBUS_PRESENT Voltage Rising Threshold	$V_{BUS\_PRESENT\_rising}$	V_{BUS} rising	3.7	3.85	4	V
VBUS_PRESENT Voltage Falling Threshold	$V_{BUS\_PRESENT\_Falling}$	V_{BUS} falling	3.4	3.5	3.6	V
IRQB Low-Level Output Voltage						
IRQB Low-Level Output Voltage	V_{IRQB_OL}	I_{IRQB_OL} = 4mA	--	--	0.4	V
VCAP						
Voltage at VCAP	V_{CAP2}	V_{BUS} ≥ 5V, no load.	4.3	--	5	V
Indication						
Output Voltage High-Level	V_{OH}	With 1MΩ resistance load	VCAP - 1	--	VCAP	V
Output Voltage Low-Level	V_{OL}	I_{OL} = 4mA	--	--	0.4	V
Table_SEL						
Input Voltage High-Level	V_{IH}		VCAP x 0.75	--	--	V
Input Voltage Low-Level	V_{IL}		--	--	VCAP x 0.25	V
Input Leakage Current	$I_{IN\_Leakage}$		–1	--	1	μA
PATH_EN						
PATH_EN Low-Level Output Voltage	$V_{PATHE\_EN\ OL}$	$I_{PATH\_EN\_OL}$ = 800μA	--	--	0.4	V
I^2C Electrical Characteristics						
I^2C Bus Pulled Voltage	V_{I2C_Hi}		1.8	--	3.6	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-Level Input Voltage	V_{IL}	V_{BUS} = 3V to 22V	--	--	0.4	V
High-Level Input Voltage	V_{IH}	V_{BUS} = 3V to 22V	1.26	--	--	V
Low-Level Output Voltage	V_{OL}	V_{BUS} = 3V to 22V, open-drain	--	--	0.4	V
Input Current Each IO Pin	I_I	V_{BUS} = 3V to 22V $0.1V_{DD} < V_I < 0.9V_{DDMAX}$	–10	--	10	μA
SCL Clock Frequency	f_{SCL}	V_{BUS} = 3V to 22V	100	--	2000	kHz
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	V_{BUS} = 3V to 22V	--	--	50	ns
Data Hold Time	$t_{HD:DAT}$	V_{BUS} = 3V to 22V	30	--	--	ns
Data Set-Up Time	$t_{SU:DAT}$	V_{BUS} = 3V to 22V	50	--	--	ns

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Register Map

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x00	1	CC_CTRL	7	CMPEN_ VDET_CC	1	RW	PD_CC1/PD_CC2 VDET resistor force off control for CMP detection 0 : Turn off CMPEN_VDET_CCx 1 : Keep HW behavior, turn on when present normal mode RD. (default)
			6	CMPEN_ VBUS_TO_ CC	0	RW	Enable VBUS short to CC1 and CC2 detection. Individual interrupt is generated when CC1 or CC2 voltage is > 3.45V. 0 : Disable CC1 and CC2 short to VBUS detection. (default) 1 : Enable CC1 and CC2 short to VBUS detection.
			5	PATHCTRL_M ODE	0	RW	PATH_CTRL pin from register setting. 0 : PATH_CTRL pin from HW control (default) 1 : PATH_CTRL pin from register setting.
			4	PATHCTRL_E N	0	RW	PATH_CTRL pin's register setting. 0 : Disable VBUS power path (default) 1 : Enable VBUS power path
			3	CC_MODE	0	RW	CC control from register setting. 0 : CC control from HW control. (default) 1 : CC control from register setting
			2	PLUG_ ORIENT	0	RW	Orientation setting when CC_MODE = 1 0 : Monitor the CC1 pin for BMC communications if PD messaging is enabled. (default) 1 : Monitor the CC2 pin for BMC communications if PD messaging is enabled.
			1	CC2	1	RW	CC2 role setting when CC_MODE = 1 0 : Open (Disconnect or don’t care) 1 : Rd (default)
			0	CC1	1	RW	CC1 role setting when CC_MODE = 1 0 : Open (Disconnect or don’t care) 1 : Rd (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x01	1	VBUSDISC_CTRL	7	FORCE_DISC_EN	0	RW	0 : Disable forced discharge (default) 1 : Enable forced discharge of VBUS.
			6	BLEED_DISC_EN	0	RW	0 : Disable bleed discharge (default) 1 : Enable bleed discharge of VBUS
			5	AUTO_DISC_EN	1	RW	Auto enable Force Discharge when CC detach and VBUS < VBUS_SNK_DISCONNECT till 650ms timeout or FORCE_DISC_EN = 1 (0x01[7]) or VBUS_PRESENT go High 0 : Disable 1 : Enable (default)
			4	Reserved	0	R	Reserved
			3:0	Reserved	0000	RW	Reserved
0x03	1	TX_CTRL1	7	TX_DRSWAP	0	RW	Initiated Date Role Swap request to source. To request change data role from DFP to UFP or UFP to DFP is controlled by MCU. Requesting Data Role Swap when USBSET configuration to not a dual role data will trigger INT_I2C_ERR. Requesting Data Role Swap when TXNG(RP 1.5A) and negotiated at PD3.0 will trigger INT_I2C_ERR. 0 : No DR_Swap sent. (default) 1 : DR_Swap sent and then 0x03[7] returns to 0b.
			6:5	Reserved	01	RW	Reserved
			4	EVASCAP_MODE	0	RW	Enable Source Cap evaluation based on the REQ_SRCPDO_NO (0x03[2:0]) or MCU selected capability instead of PSEL. 0 : Evaluation per PSEL setting. (default) 1 : Evaluation per register setting.
			3	Reserved	0	RW	Reserved
			2:0	REQ_SRCPDO_NO	000	RW	Selected SRCPDO number in the request message which is initiated by TX_SPDO_REQ. Set to 000 or invalid object number will trigger INT_I2C_ERR when set TX_SPDO_REQ = 1 000 : No PDO selected (default) 001 : Select the first PDO. … 111 : Select the seventh PDO.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x04	1	TX_CTRL2	7	TX_SPDO_REQ	0	RW	Set EVASCAP_MODE = 1 (0x03[4]) when try to initiate Request message to source. Initiated Fixed power supply Request of select SRCPDO (0x03[2:0]) to source. When initiated, it will update Sink Capabilities to 2 objects which contain 5V/PSEL_5V current and selected SRC PDO's voltage/current when REQ_SRCPDO_NO not 1. Or update Sink Capabilities to 1 object which is the same as 1st SRC PDO when REQ_SRCPDO_NO = 1. Requesting TX_SPDO_REQ when TXNG (RP 1.5A) and negotiated at PD3.0 will trigger INT_I2C_ERR. 0 : No Request sent. (default) 1 : Request sent and then 0x04[7] returns to 0b.
			6	TX_SRCCAP_REQ	0	RW	Initiated Get_Source_Cap request to source. Requesting Get_Source_Cap when TXNG(RP 1.5A) and negotiated at PD3.0 will trigger INT_I2C_ERR. 0 : No Get_Source_Cap sent. (default) 1 : Get_Source_Cap sent and then 0x04[6] returns to 0b.
			5:1	Reserved	00000	R	Reserved
			0	REQ_HIGHER_CAP	0	RW	HIGHER_CAP field in the Request message which is initiated by TX_SPDO_REQ (0x04[7]). 0 : No higher cap needed (default) 1 : Higher cap needed

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x0D	1	PINDEB_INFO	7:5	Reserved	000	RW	Reserved
			4	Reserved	0	R	Reserved
			3	LAT_ADR_RDY	0	R	ADDR pin de-bounce result after power on. 0 : De-bounce timeout. The slave ID is 0x40 in 7-bit. (default) 1 : De-bounce success
			2	LAT_PATH_RDY	0	R	Path_Opt pin de-bounce result after power on. 0 : De-bounce timeout. PATH_EN in off state (default) 1 : De-bounce success
			1	LAT_USB_RDY	0	R	USB_SET pin de-bounce result after power on. 0 : De-bounce timeout. USB Comm capability and Dual Data Role are not supported (default) 1 : De-bounce success
			0	LAT_PSEL_RDY	0	R	PSEL1/PSEL2/TABLE_SET pin de-bounce result after power on. 0 : De-bounce timeout. PD Comm capability is not supported and PATH_EN is off if Path_Opt is 0 or 1. (Table_SEL, PSEL2, PSEL1) = (0,111,111) (default) 1 : De-bounce success
0x0E	1	POLICY_INFO	7:4	Reserved	0000	R	Reserved
			3	VBUSONLY_MIS	0	R	Indication of No-RP Source attached. And it's current capability (5V/500mA) not meet Sink requirement. 0 : No No-RP Source attached (default) 1 : No-RP Source attached
			2:0	Reserved	000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x0F	1	TYPECATTACH_INFO	7:5	SPDO_NUM	000	R	Indication of how many Source PDOs is received.
			4	ATTACH_VBUS	0	R	Indication of VBUS only attached last over 300ms. 0 : Not in attached VBUS state. (default) 1 : In attached VBUS state.
			3	Reserved	0	R	Reserved
			2	ATTACH_DBG	0	R	Indication of Type-C is in Attached as Debug Accessory State. 0 : Not in debug accessory state (default) 1 : In debug accessory State
			1	ATTACH_SNK	0	R	Indication of Type-C is in Attached as Sink State. 0 : Not in attached as Sink state (default) 1 : In attached as Sink State
			0	TYPEC_MIS	0	R	Indication of Type-C current capability not meet Sink requirement. 0 : No mismatch with Source (default) 1 : Mismatch with Type-C-Only Source
0x10	1	PDATTACH_INFO	7	POLARITY	0	R	Attached polarity, updated when enter entered into attached_snk state from attachedwait_state. Detection apply for signal RP only. 0 : CC1 (default) 1 : CC2
			6	DATA_ROLE	0	R	current data role after Type-C attached. 0 : UFP (default) 1 : DFP
			5:4	USBPD_SPECREV	00	R	Negotiated PD SPEC 00 : Revision 1.0 (default) 01 : Revision 2.0 10 : Revision 3.0 11 : Reserved
			3	SPDO_MIS	0	R	Indication of capability mismatch.
			2:0	SPDO_SEL	000	R	Indication of which SRCPDO is been used.
0x11	1	SRCPDO1_0	7:0	SRCPDO1_0	00000000	R	Received SRCCAP message and stored OBJ1 content, reset when Type-C detached.
0x12	1	SRCPDO1_1	7:0	SRCPDO1_1	00000000	R	Received SRCCAP message and stored OBJ1 content, reset when Type-C detached.
0x13	1	SRCPDO1_2	7:0	SRCPDO1_2	00000000	R	Received SRCCAP message and stored OBJ1 content, reset when Type-C detached.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x14	1	SRCPDO1_3	7:0	SRCPDO1_3	00000000	R	Received SRCCAP message and stored OBJ1 content, reset when Type-C detached.
0x15	1	SRCPDO2_0	7:0	SRCPDO2_0	00000000	R	Received SRCCAP message and stored OBJ2 content, reset when Type-C detached.
0x16	1	SRCPDO2_1	7:0	SRCPDO2_1	00000000	R	Received SRCCAP message and stored OBJ2 content, reset when Type-C detached.
0x17	1	SRCPDO2_2	7:0	SRCPDO2_2	00000000	R	Received SRCCAP message and stored OBJ2 content, reset when Type-C detached.
0x18	1	SRCPDO2_3	7:0	SRCPDO2_3	00000000	R	Received SRCCAP message and stored OBJ2 content, reset when Type-C detached.
0x19	1	SRCPDO3_0	7:0	SRCPDO3_0	00000000	R	Received SRCCAP message and stored OBJ3 content, reset when Type-C detached.
0x1A	1	SRCPDO3_1	7:0	SRCPDO3_1	00000000	R	Received SRCCAP message and stored OBJ3 content, reset when Type-C detached.
0x1B	1	SRCPDO3_2	7:0	SRCPDO3_2	00000000	R	Received SRCCAP message and stored OBJ3 content, reset when Type-C detached.
0x1C	1	SRCPDO3_3	7:0	SRCPDO3_3	00000000	R	Received SRCCAP message and stored OBJ3 content, reset when Type-C detached.
0x1D	1	SRCPDO4_0	7:0	SRCPDO4_0	00000000	R	Received SRCCAP message and stored OBJ4 content, reset when Type-C detached.
0x1E	1	SRCPDO4_1	7:0	SRCPDO4_1	00000000	R	Received SRCCAP message and stored OBJ4 content, reset when Type-C detached.
0x1F	1	SRCPDO4_2	7:0	SRCPDO4_2	00000000	R	Received SRCCAP message and stored OBJ4 content, reset when Type-C detached.
0x20	1	SRCPDO4_3	7:0	SRCPDO4_3	00000000	R	Received SRCCAP message and stored OBJ4 content, reset when Type-C detached.
0x21	1	SRCPDO5_0	7:0	SRCPDO5_0	00000000	R	Received SRCCAP message and stored OBJ5 content, reset when Type-C detached.
0x22	1	SRCPDO5_1	7:0	SRCPDO5_1	00000000	R	Received SRCCAP message and stored OBJ5 content, reset when Type-C detached.
0x23	1	SRCPDO5_2	7:0	SRCPDO5_2	00000000	R	Received SRCCAP message and stored OBJ5 content, reset when Type-C detached.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x24	1	SRCPDO5_3	7:0	SRCPDO5_3	00000000	R	Received SRCCAP message and stored OBJ5 content, reset when Type-C detached.
0x25	1	SRCPDO6_0	7:0	SRCPDO6_0	00000000	R	Received SRCCAP message and stored OBJ6 content, reset when Type-C detached.
0x26	1	SRCPDO6_1	7:0	SRCPDO6_1	00000000	R	Received SRCCAP message and stored OBJ6 content, reset when Type-C detached.
0x27	1	SRCPDO6_2	7:0	SRCPDO6_2	00000000	R	Received SRCCAP message and stored OBJ6 content, reset when Type-C detached.
0x28	1	SRCPDO6_3	7:0	SRCPDO6_3	00000000	R	Received SRCCAP message and stored OBJ6 content, reset when Type-C detached.
0x29	1	SRCPDO7_0	7:0	SRCPDO7_0	00000000	R	Received SRCCAP message and stored OBJ7 content, reset when Type-C detached.
0x2A	1	SRCPDO7_1	7:0	SRCPDO7_1	00000000	R	Received SRCCAP message and stored OBJ7 content, reset when Type-C detached.
0x2B	1	SRCPDO7_2	7:0	SRCPDO7_2	00000000	R	Received SRCCAP message and stored OBJ7 content, reset when Type-C detached.
0x2C	1	SRCPDO7_3	7:0	SRCPDO7_3	00000000	R	Received SRCCAP message and stored OBJ7 content, reset when Type-C detached.
0x2D	1	MASK1	7	M_VBUS_HV	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			6	M_VBUS_DCT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			5	M_VBUS_PRESENT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			4	M_VBUS_TO_CC2	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			3	M_VBUS_TO_CC1	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			2	M_PE_SNK_RDY	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			1	M_TYPC_ATTACH_SNK	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			0	M_CC_CHANGE	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x2E	1	MASK2	7	M_DRSW_ ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			6	M_DRSW_ REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			5	M_DRSW_ WAIT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			4	M_DRSW_ TIMEOUT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			3	M_REQ_ ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			2	M_REQ_ REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			1	M_REQ_ WAIT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			0	M_GSRCCAP _SENT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
0x2F	1	MASK3	7	M_RX_DRSW _ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			6	M_RX_DRSW _REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			5	M_RX_ SRCCAP	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			4	M_RX_ NOTSUPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			3	M_RX_ HARDRST	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			2	M_RX_ PSRDY	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			1:0	Reserved	00	R	Reserved
0x30	1	MASK4	7	M_REQ_SENT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			6	M_TX_ SUCCESS	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			5	M_TX_ DISCARD	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			4	M_TX_FAIL	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
			3:1	Reserved	000	RW	Reserved
			0	M_I2C_ERR	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x33	1	RT_INT1	7	INT_VBUS_HV	0	WC	0 : Cleared (default) 1 : VBUS_HV_FLAG go High (VBUS reach over-voltage threshold)
			6	INT_VBUS_DCT	0	WC	0: Cleared (default) 1: VBUS_DCT_FLAG go High (VBUS reach disconnect threshold)
			5	INT_VBUS_PRESENT	0	WC	0: Cleared (default) 1: VBUS_PRESENT_FLAG go High (VBUS reach present threshold)
			4	INT_VBUS_TO_CC2	0	WC	0 : Cleared (default) 1 : The voltage at CC2 is higher than 3.45V.
			3	INT_VBUS_TO_CC1	0	WC	0 : Cleared (default) 1 : The voltage at CC1 is higher than 3.45V.
			2	INT_PE_SNK_RDY	0	WC	0 : Cleared (default) 1 : Policy Engine Enter PE_SNK_RDY state.
			1	INT_TYPC_ATTACH_SNK	0	WC	0 : Cleared (default) 1 : Type-C Attached_SNK state is entered.
			0	INT_CC_CHANGE	0	WC	0 : Cleared (default) 1 : CC1_ST or CC2_ST (0x38[3:0]) has changed.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x34	1	RT_INT2	7	INT_DRSW_ACCEPT	0	WC	0 : No DR_Swap transmitted, or Accept not received. Cleared. (default) 1 : Transmit DR_Swap and Accept received.
			6	INT_DRSW_REJECT	0	WC	0 : No DR_Swap transmitted, or Reject not received. Cleared. (default) 1 : Transmit DR_Swap and Reject received.
			5	INT_DRSW_WAIT	0	WC	0 : No DR_Swap transmitted, or Wait not received. Cleared. (default) 1 : Transmit DR_Swap and Wait received.
			4	INT_DRSW_TIMEOUT	0	WC	0 : No DR_Swap transmitted. Cleared. (default) 1 : Transmit DR_Swap and no any response.
			3	INT_REQ_ACCEPT	0	WC	0 : No Request transmitted, or Accept not received. Cleared. (default) 1 : Transmit Request and Accept received.
			2	INT_REQ_REJECT	0	WC	0 : No Request transmitted, or Reject not received. Cleared. (default) 1 : Transmit Request and Reject received.
			1	INT_REQ_WAIT	0	WC	0 : No Request transmitted, or Wait not received. Cleared. (default) 1 : Transmit Request and Wait received.
			0	INT_GSRCCAP_SENT	0	WC	0 : No Get_SRC_CAP transmitted or no GoodCRC response. Cleared. (default) 1 : Transmit Get_SRC_CAP and GoodCRC received.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x35	1	RT_INT3	7	INT_RX_ DRSW_ ACCEPT	0	WC	0 : No DR_Swap received or no Accept transmitted. Cleared. (default) 1 : DR_Swap received and Accept transmitted.
			6	INT_RX_ DRSW_ REJECT	0	WC	0 : No DR_Swap received or no Reject transmitted. Cleared. (default) 1 : DR_Swap received and Reject transmitted.
			5	INT_RX_ SRCCAP	0	WC	0 : No Source_Cap received. Cleared. (default) 1 : Source_Cap received in PE_SNK_READY state or PE_SNK_WAIT_FOR_CAP state.
			4	INT_RX_ NOTSUPT	0	WC	0 : No Not_Supported received. Cleared. (default) 1 : Not_Supported received.
			3	INT_RX_ HARDRST	0	WC	0 : No Hard Reset received. Cleared. (default) 1 : Hard Reset received.
			2	INT_RX_ PSRDY	0	WC	0 : No PS_RDY received. Cleared. (default) 1 : PS_RDY received.
			1:0	Reserved	00	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x36	1	RT_INT4	7	INT_REQ_SENT	0	WC	0 : No Request transmitted or no GoodCRC response. Cleared. (default) 1 : Transmit Request and GoodCRC received.
			6	INT_TX_SUCCESS	0	WC	0 : No PD message transmitted or no GoodCRC response. Cleared. (default) 1 : Reset or SOP message transmission successful. GoodCRC response received on SOP message transmission.
			5	INT_TX_DISCARD	0	WC	0 : PD message transmitted. Cleared. (default) 1 : Reset or SOP message transmission not sent due to an incoming receive message.
			4	INT_TX_FAIL	0	WC	0 : No PD message transmitted or GoodCRC response. Cleared. (default) 1 : SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
			3:2	Reserved	00	R	Reserved
			1	Reserved	0	WC	Reserved
			0	INT_I2C_ERR	0	WC	0 : Cleared (default) 1 : Transmit "Request" with invalid Object setting. E.g. Obj = 0, or Not Existing Obj number. Transmit "DR_Swap" when Pins are configured to not a dual role data. Transmit "Request", "DR_Swap" and "Get_Source_Cap" when RP level is 1.5A in PD 3.0 communication.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x37	1	RT_ST1	7	VBUS_HV	0	R	0 : VBUS is not at vHV (default) 1 : VBUS is at vHV
			6	VBUS_ SNKDISC	0	R	0 : VBUS is not at vSNKDisc (default) 1 : VBUS is at vSNKDisc
			5	VBUS_ PRESENT	0	R	0 : VBUS is not at vPRESENT (default) 1 : VBUS is at vPRESENT
			4	VBUS_TO_ CC2	0	R	0 : The voltage at CC2 is lower than 3.45V. (default) 1 : The voltage at CC2 is higher than 3.45V.
			3	VBUS_TO_ CC1	0	R	0 : The voltage at CC1 is lower than 3.45V. (default) 1 : The voltage at CC1 is higher than 3.45V.
			2	PE_SNK_ RDY	0	R	0 : Not in Policy Sink Ready State (default) 1 : In Policy Sink Ready State
			1	TYPC_ ATTACH_ SNK	0	R	0 : Not in Type-C attached sink state (default) 1 : In Type-C attached sink state
			0	Reserved	0	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x38	1	RT_ST2	7:5	Reserved	000	R	Reserved
			4	PD3_TXNG	0	R	0 : PD2.0 communication or RP level is 3A in PD3.0 communication. (default) 1 : Indication of connected CCx pin is in RP1P5A level after PD3.0 power contract is established (Explicit contract). Apply for attached as sink only, not available for debug accessory plugin.
			3:2	CC2_ STATUS	00	R	If (ROLE_CONTROL.CC2 = Rd) 00 : SNK.Open (Below maximum vRa) (default) 01 : SNK.Default (Above minimum vRd-Connect) 10 : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A 11 : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A If ROLE_CONTROL.CC2 = Open, this field is set to 00.
			1:0	CC1_ STATUS	00	R	If (ROLE_CONTROL.CC1 = Rd) 00 : SNK.Open (Below maximum vRa) (default) 01 : SNK.Default (Above minimum vRd-Connect) 10 : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A 11 : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A If ROLE_CONTROL.CC1 = Open, this field is set to 00.
0x3B	1	FAULT_ CTRL	7:3	Reserved	00000	R	Reserved
			2:0	FAULT_CNT	111	RW	Limit Fault (VBUS reach High Voltage threshold) handling (PATH_EN turns off) times to FAULT_CNT. After reach FAULT_CNT, PATH_EN remains off till new plugin. Set 0 to disable Limit Fault function. 000 : Disable 001 : 1 time … 111 : 7 times (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x3C	1	PSEL_ DEBINFO1	7	Reserved	0	R	Reserved
			6	LAT_TABLE_ SELL	1	R	Latched TABLE_SEL result during power on sequence. With 0x0D[0] indicate de-bounce success or timeout (30ms)
			5:3	LAT_PSEL2	111	R	Latched PSEL2 result during power on sequence. With 0x0D[0] indicate de-bounce success or timeout (30ms)
			2:0	LAT_PSEL1	111	R	Latched PSEL1 result during power on sequence. With 0x0D[0] indicate de-bounce success or timeout (30ms)
0x3E	1	USBSET_ DEBINFO	7:2	Reserved	000000	R	Reserved
			1:0	LAT_USB	00	R	Latched USB_SET result during power on sequence. With 0x0D[1] indicate de-bounce success or timeout (30ms)
0x3F	1	PATHOPT_ DEBINFO	7:3	Reserved	00000	R	Reserved
			2:0	LAT_ PATHOPT	000	R	Latched PATH_OPT result during power on sequence. With 0x0D[2] indicate de-bounce success or timeout (30ms)
0x50	1	PRO_ SNKCAP_ EXT1	7:0	VID[7:0]	00000000	RW	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x51	1		7:0	VID[15:8]	00000000	RW	
0x52	1	PRO_ SNKCAP_ EXT2	7:0	PID[7:0]	00000000	RW	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the product.
0x53	1		7:0	PID[15:8]	00000000	RW	
0x54	1	PRO_ SNKCAP_ EXT3	7:0	XID[7:0]	11111111	RW	A unique 32-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x55	1		7:0	XID[15:8]	11111111	RW	
0x56	1		7:0	XID[23:16]	11111111	RW	
0x57	1		7:0	XID[31:24]	11111111	RW	
0x58	1	PRO_ SNKCAP_ EXT4	7:0	FW_VER	00000000	RW	Firmware version number
0x59	1	PRO_ SNKCAP_ EXT5	7:0	HW_VER	00000000	RW	Hardware version number
0x5A	1	PRO_ SNKCAP_ EXT6	7:0	SKEDB_VER	00000001	RW	SKEDB version = 1
0x5B	1	PRO_ SNKCAP_ EXT7	7:0	LOAD_STEP	00000000	RW	0 : 150mA/μs (default) 1 : 500mA/μs Bit1 to Bit7 are reserved and shall not be used.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x5C	1	PRO_ SNKCAP_ EXT8	7:0	SNK_LOAD [7:0]	00000000	RW	Bit[4:0] Percent overload in 10% increments Values higher than 25 (11001b) are clipped to 250%. 00000b is the default. Bit[7:5] Overload period in 20ms when bits 0-4 non-zero.
0x5D	1		7:0	SNK_LOAD [15:8]	10000000	RW	Bit[1:0] Overload period in 20ms when bits 0-4 non-zero. Bit[6:2] Duty cycle in 5% increments when bits 0-4 are non-zero Bit[7] Can tolerate VBUS Voltage droop
0x5E	1	PRO_ SNKCAP_ EXT9	7:0	COMPLIANCE	00000000	RW	Bit 0 Requires LPS Source when set Bit 1 Requires PS1 Source when set Bit 2 Requires PS2 Source when set 3…7 bits are Reserved and Shall be set to zero
0x5F	1	PRO_ SNKCAP_ EXT10	7:0	TOUCH_ TEMP	00000000	RW	Temperature conforms to : 00000000 = Not applicable (default) 00000001 = [IEC 60950-1] 00000010 = [IEC 62368-1] TS1 00000011 = [IEC 62368-1] TS2 Note : All other values Reserved
0x60	1	PRO_ SNKCAP_ EXT11	7:0	BATTERY_ INFO	00000000	RW	Upper Nibble = Number of Hot Swappable Battery Slots (0…4) Lower Nibble = Number of Fixed Batteries (0…4)
0x61	1	PRO_ SNKCAP_ EXT12	7:0	SNK_MODES	00000010	RW	Bit 0 1 : PPS charging supported Bit 1 1 : VBUS powered Bit 2 1 : Mains powered Bit 3 1 : Battery powered Bit 4 1 : Battery essentially unlimited Bit 5 1 : AVS supported Bit 6 and 7 are reserved and shall be set to zero
0x62	1	PRO_SNKC AP_EXT13	7:0	SNK_PDP	00000000	RW	Manual setting for Sink Cap Extended message. Bit 0 to Bit 6 : The Minimum PDP required by the Sink to operate without consuming any power from its Battery(s) should it have one. Bit 7 is reserved and shall be set to zero
0x65	1	PRO_ SNKCAP_ CTRL	7	SNKCAPEXT_ CTRL_EN	0	RW	Sink Cap Extended message's content 0 : From the default values of 0x50 to 0x61 no matter what 0x50 to 0x61 are modified. The Sink PDP is from 0x62. (default) 1: From the values of 0x50 to 0x62.
			6:0	Reserved	0000000	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x72	1	SNKCAP1	7:0	PSEL_MCU_CUR_L	00000000	R	Manual determined operating current. 0x73[7] = 0b : 0x72 and 0x73[1:0] will be zero. 0x73[7] = 1b : 0x72 and 0x73[1:0] are from Received SRCPDO of selected OBJ number (0x10[2:0]). The current step is 10mA.
0x73	1	SNKCAP2	7	PSEL_MCU	0	R	Indication of PSEL_MCU_VOLT/PSEL_MCU_CUR is used for SNKCAP message and evaluation of power with Source. 0 : MCU Selected SNKCAP is not in used. (default) 1 : MCU Selected SNKCAP is in used.
			6:2	PSEL_PDP [4:0]	00000	R	Reveal PDP information in sink cap ext message. 0x65[7] = 0b : 0x73[6:2] and 0x75[4:2] are determined by PSEL1/PSEL2/TABLE_SET setting. 0x65[7] = 1b : 0x73[6:2] and 0x75[4:2] are determined by control register 0x62.
			1:0	PSEL_MCU_CUR_H	00	R	Manual determined operating current. 0x73[7] = 0b : 0x72 and 0x73[1:0] will be zero. 0x73[7] = 1b : 0x72 and 0x73[1:0] are from Received SRCPDO of selected OBJ number (0x10[2:0]). The current step is 10mA.
0x74	1	SNKCAP3	7:0	PSEL_MCU_VOLT_L	00000000	R	Manual determined operating voltage. 0x73[7] = 0b : 0x74 and 0x75[1:0] are zero. 0x73[7] = 1b : 0x74 and 0x75[1:0] are from the received SRCPDO of selected OBJ number (0x10[2:0]). The voltage step is 50mV.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x75	1	SNKCAP4	7	EVASCAP_CTRL_EN	0	R	Determination of which sink capabilities is from and used for evaluation of source PDO. 0 : PSEL1/PSEL2/TABLE_SET determined (default) 1 : MCU selected VOL/CUR from SRCPDOs MCU selected method is entered when MCU initiated TX Request (0x04[7] = 1b) with correct setting (0x03[4] = 1b and selected object (0x03[2:0]) is not zero or larger than received SPDO number). MCU selected method is cleared when Source detached, unchanged response from source (Wait, Reject) for "Request" message is received, or the updated sink cap by MCU selected VOL/CUR evaluated is capability mismatched with new Source Capabilities received.
			6:5	Reserved	00	R	Reserved
			4:2	PSEL_PDP[7:5]	000	R	Reveal PDP information in sink cap ext message. 0x65[7] = 0b : 0x73[6:2] and 0x75[4:2] are determined by PSEL1/PSEL2/TABLE_SET setting. 0x65[7] = 1b : 0x73[6:2] and 0x75[4:2] are determined by control register 0x62.
			1:0	PSEL_MCU_VOLT_H	00	R	Manual determined operating voltage. 0x73[7] = 0b : 0x74 and 0x75[1:0] are zero. 0x73[7] = 1b : 0x74 and 0x75[1:0] are from the received SRCPDO of selected OBJ number (0x10[2:0]). The voltage step is 50mV.
0x76	1	SNKCAP5	7:0	PSEL_5V_CUR_L	00000000	R	0x73[7] = 0b : 0x76 and 0x77[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : If OBJ1 is selected (0x10[2:0] = 1), 0x76 and 0x77[1:0] are from the received SRCPDO OBJ1. If OBJ1 is not selected (0x10[2:0]! = 1), 0x76 and 0x77[1:0] are from PSEL1/PSEL2/TABLE_SET settings. The current step is 10mA.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x77	1	SNKCAP6	7	PSEL_5V	0	R	0x73[7] = 0b : 0 : 5V Sink PDO is not the candidate for the evaluation of Source PDO. (default) 1 : 5V Sink PDO is the candidate for the evaluation of Source PDO. 0x73[7] = 1b : 5V Sink PDO is not used for the evaluation of Source PDO. 0x77[7] = 0b.
			6:2	PSEL_ TXBYTE	00000	R	Indication of transmit bytes for SNK_CAP message. 0x77[6:2] = 4 * Sink PDO number + 2. 2 bytes are Header.
			1:0	PSEL_5V_ CUR_H	00	R	0x73[7] = 0b : 0x76 and 0x77[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : If OBJ1 is selected (0x10[2:0] = 1), 0x76 and 0x77[1:0] are from the received SRCPDO OBJ1. If OBJ1 is not selected (0x10[2:0]! = 1), 0x76 and 0x77[1:0] are from PSEL1/PSEL2/TABLE_SET settings. The current step is 10mA.
0x78	1	SNKCAP7	7:0	PSEL_9V_ CUR_L	00000000	R	0x73[7] = 0b : 0x78 and 0x79[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x78 = 00h and 0x79[1:0] = 00b. The current step is 10mA.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x79	1	SNKCAP8	7	PSEL_9V	0	R	0x73[7] = 0b : 0 : 9V Sink PDO is not the candidate for the evaluation of Source PDO. (default) 1 : 9V Sink PDO is the candidate for the evaluation of Source PDO. 0x73[7] = 1b : 9V Sink PDO is not used for the evaluation of Source PDO. 0x79[7] = 0b.
			6:2	Reserved	00000	R	Reserved
			1:0	PSEL_9V_CUR_H	00	R	0x73[7] = 0b : 0x78 and 0x79[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x78 = 00h and 0x79[1:0] = 00b. The current step is 10mA.
0x7A	1	SNKCAP9	7:0	PSEL_12V_CUR_L	00000000	R	0x73[7] = 0b : 0x7A and 0x7B[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7A = 00h and 0x7B[1:0] = 00b. The current step is 10mA.
0x7B	1	SNKCAP10	7	PSEL_12V	0	R	0x73[7] = 0b : 0 : 12V Sink PDO is not the candidate for the evaluation of Source PDO. (default) 1 : 12V Sink PDO is the candidate for the evaluation of Source PDO. 0x73[7] = 1b : 12V Sink PDO is not used for the evaluation of Source PDO. 0x7B[7] = 0b.
			6:2	Reserved	00000	R	Reserved
			1:0	PSEL_12V_CUR_H	00	R	0x73[7] = 0b : 0x7A and 0x7B[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7A = 00h and 0x7B[1:0] = 00b. The current step is 10mA.
0x7C	1	SNKCAP11	7:0	PSEL_15V_CUR_L	00000000	R	0x73[7] = 0b : 0x7C and 0x7D[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7C = 00h and 0x7D[1:0] = 00b. The current step is 10mA.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x7D	1	SNKCAP12	7	PSEL_15V	0	R	0x73[7] = 0b : 0 : 15V Sink PDO is not the candidate for the evaluation of Source PDO. (default) 1 : 15V Sink PDO is the candidate for the evaluation of Source PDO. 0x73[7] = 1b : 15V Sink PDO is not used for the evaluation of Source PDO. 0x7D[7] = 0b.
			6:2	Reserved	00000	R	Reserved
			1:0	PSEL_15V_CUR_H	00	R	0x73[7] = 0b : 0x7C and 0x7D[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7C = 00h and 0x7D[1:0] = 00b. The current step is 10mA.
0x7E	1	SNKCAP13	7:0	PSEL_20V_CUR_L	00000000	R	0x73[7] = 0b : 0x7E and 0x7F[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7E = 00h and 0x7F[1:0] = 00b. The current step is 10mA.
0x7F	1	SNKCAP14	7	PSEL_20V	0	R	0x73[7] = 0b : 0 : 20V Sink PDO is not the candidate for the evaluation of Source PDO. (default) 1 : 20V Sink PDO is the candidate for the evaluation of Source PDO. 0x73[7] = 1b : 20V Sink PDO is not used for the evaluation of Source PDO. 0x7F[7] = 0b.
			6:2	Reserved	00000	R	Reserved
			1:0	PSEL_20V_CUR_H	00	R	0x73[7] = 0b : 0x7E and 0x7F[1:0] are from PSEL1/PSEL2/TABLE_SET settings. 0x73[7] = 1b : 0x7E = 00h and 0x7F[1:0] = 00b. The current step is 10mA.
0x80	1	DEVICE_ID	7:0	DID[7:0]	10010001	R	DEVICE ID
0x81	1		7:0	DID[15:8]	01000110	R	
0x82	1	PRODUCT_ID	7:0	PID[7:0]	00011001	R	PRODUCT ID
0x83	1		7:0	PID[15:8]	00010111	R	

Application Information

USB_PD

The PD function of the RT1719 complies with USB Power Delivery spec 3.0-controller.

Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the CC1, CC2 pins. This status information provides the host processor all of the information required to determine attach and detach status of the cable.

The USB_PD has three threshold comparators, which match the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device.

Dead Battery Mode

When VBUS is off, RT1719 shall apply Rd on both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. Circuitry to present Rd in this case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide VBUS.

I²C Interface

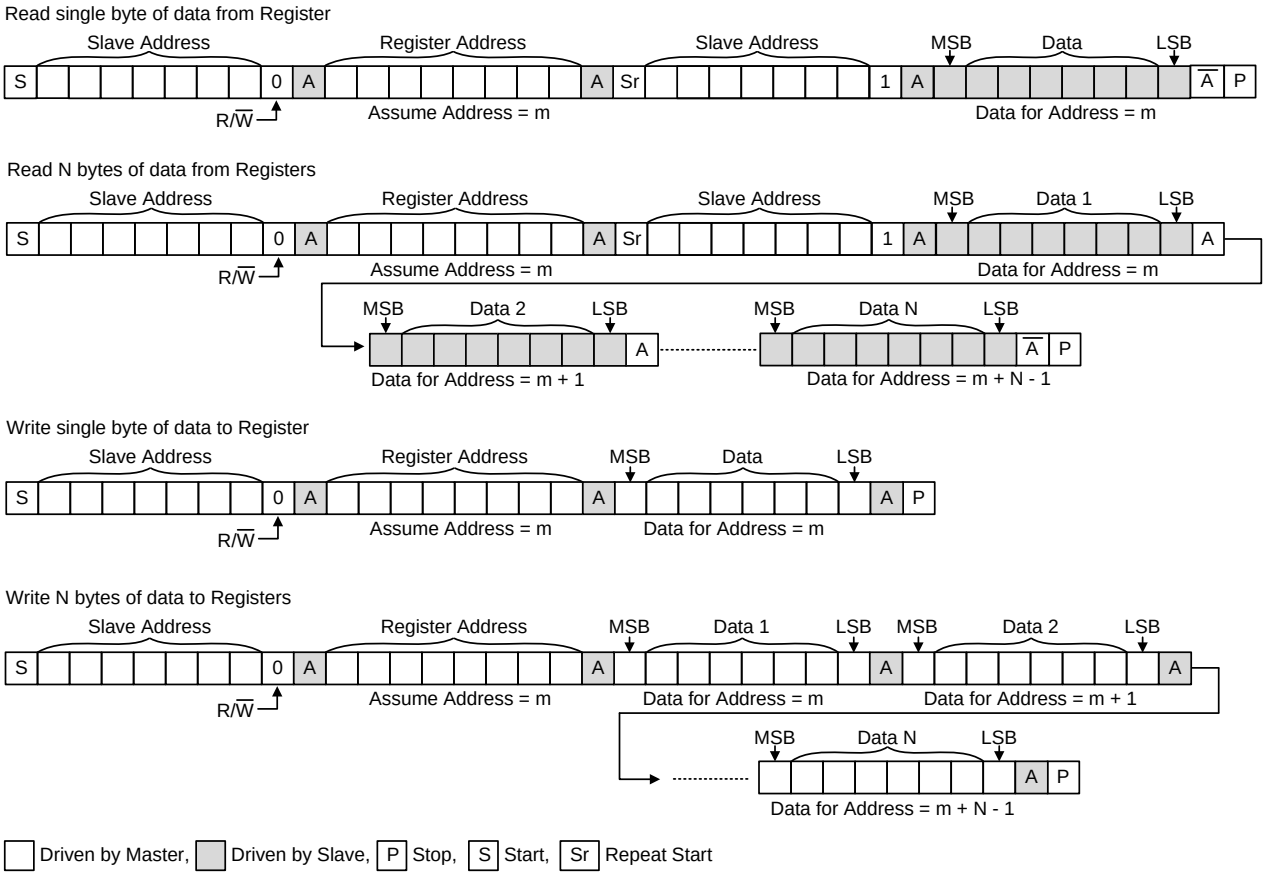
The RT1719 can be configured to four slave addresses by setting the resistance between ADDR (pin 12) and GND.

I²C Address in 7bit	Resistance between ADDR and GND (unit : kΩ)
0x40	0
0x41	309
0x42	649
0x43	open

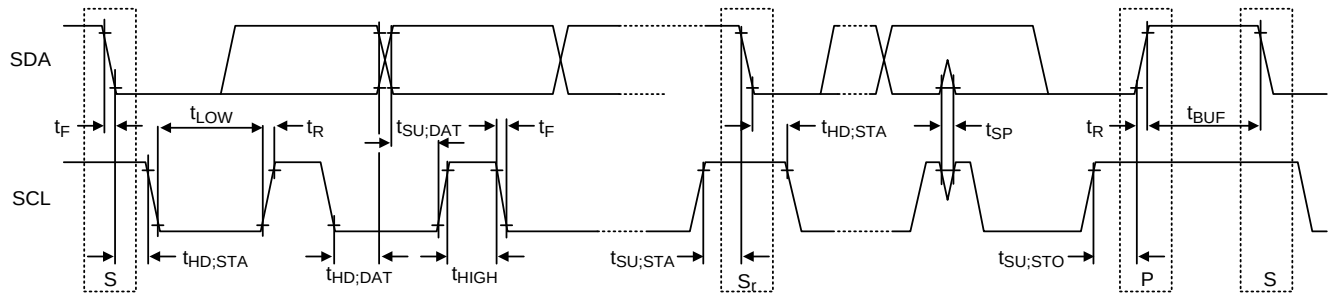
The I²C interface bus must be connect a resistor 1kΩ to power node and independent connection to processor, individually.

The I²C timing diagrams are listed below.

- **Read and Write Function**



- **I²C Waveform Information**



USB Setting

The USB ability of RT1719 can be set by USB_SET (pin 13).

USB Setting	Resistance between USB_SET and GND (unit : kΩ)	0x3E[1:0]	Behavior
USB Ability, Data Role Swap	Open	11b	1. Respond “DR_Swap” by sending “Accept,” and 0x35[7] will be 1b if “DR_Swap” is received. 2. USB Communications Capable in “Sink_Capabilities” is 1b. 3. MCU can send “DR_Swap” by 0x03[7] = 1b.
USB Ability, No Data Role Swap (UFP Only)	309	01b	1. Respond “DR_Swap” by sending “Reject,” and 0x35[6] will be 1b if “DR_Swap” is received. 2. USB Communications Capable in “Sink_Capabilities” is 1b.
No USB Ability	0	00b	1. Respond “DR_Swap” by sending “Reject,” and 0x35[6] will be 1b if “DR_Swap” is received. 2. USB Communications Capable in “Sink_Capabilities” is 0b.

The RT1719 will respond DR Swap from port partner according to the setting of US_SET and report the result in the register 0x35[7:6].

Address	Bit	Bit Name	Default	Type	Description
0x2F	7	M_RX_DRSW_ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	6	M_RX_DRSW_REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
0x35	7	INT_RX_DRSW_ACCEPT	0	WC	0 : no DR_Swap received or no Accept transmitted. Cleared. (default) 1 : DR_Swap received and Accept transmitted.
	6	INT_RX_DRSW_REJECT	0	WC	0 : no DR_Swap received or no Reject transmitted. Cleared. (default) 1 : DR_Swap received and Reject transmitted.

Table Select

There are 128 Sink_Capabilities to be able to configure. There are 64 Sink_Capabilities in Table 1. The sink currents of each Sink PDO in the Sink capability are the same. There are the other 64 Sink_Capabilities in Table 0. The sink powers of each Sink PDO in the Sink capability are the same except for the one which the sink current is over 5A.

Table Setting	Configure in Pin 18	0x3C[6]
Table 1	10kΩ to VCAP (pin 10)	1b
Table 0	10kΩ to GND	0b

PSEL

PSEL2 (pin 3) and PSEL1 (pin 4) can configure 64 settings. The sink capability can be configured according to Table select, PSEL2, and PSEL1.

PSEL2 Setting	Resistance between PSEL2 and GND (unit : kΩ)	0x3C[5:3]
111	Open	111b
110	887	110b
101	649	101b
100	453	100b
011	324	011b
010	143	010b
001	56.2	001b
000	0	000b

PSEL1 Setting	Resistance between PSEL1 and GND (unit : kΩ)	0x3C[2:0]
111	Open	111b
110	887	110b
101	649	101b
100	453	100b
011	324	011b
010	143	010b
001	56.2	001b
000	0	000b

The Min V in the following 2 tables means that the sink system cannot operate if VBUS is under than the Min V. Taking (Table_Sel, PSEL2, PSEL1) = (1,101,011) as example, the PDO1 (5V/1000mA) will not be the candidate to match with Source PDO or Rp level.

Table 1

Table_Sel Setting	PSEL2 Setting	PSEL1 Setting	Min. V	Max. V	PDO1		PDO2		PDO3		PDO4		PDO5	
					V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)
1	111	111	5	9	5	500	9	500	NA	NA				
1	111	110	5	9	5	1000	9	1000	NA	NA				
1	111	101	5	9	5	1500	9	1500	NA	NA				
1	111	100	5	9	5	2000	9	2000	NA	NA				
1	111	011	5	9	5	2500	9	2500	NA	NA				
1	111	010	5	9	5	3000	9	3000	NA	NA				
1	111	001	5	9	5	3500	9	3500	NA	NA				
1	111	000	5	9	5	4000	9	4000	NA	NA				
1	110	111	5	9	5	4500	9	4500	NA	NA				
1	110	110	5	9	5	5000	9	5000	NA	NA				
1	110	101	5	12	5	500	9	500	12	500	NA	NA		
1	110	100	5	12	5	1000	9	1000	12	1000	NA	NA		
1	110	011	5	12	5	1500	9	1500	12	1500	NA	NA		
1	110	010	5	12	5	2000	9	2000	12	2000	NA	NA		
1	110	001	5	12	5	2500	9	2500	12	2500	NA	NA		
1	110	000	5	12	5	3000	9	3000	12	3000	NA	NA		
1	101	111	5	12	5	3500	9	3500	12	3500	NA	NA		
1	101	110	5	12	5	4000	9	4000	12	4000	NA	NA		
1	101	101	5	12	5	4500	9	4500	12	4500	NA	NA		
1	101	100	5	12	5	5000	9	5000	12	5000	NA	NA		
1	101	011	12	12	5	1000	12	1000	NA	NA				
1	101	010	12	12	5	1500	12	1500	NA	NA				
1	101	001	12	12	5	2000	12	2000	NA	NA				
1	101	000	12	12	5	2500	12	2500	NA	NA				
1	100	111	12	12	5	3000	12	3000	NA	NA				
1	100	110	12	12	5	3500	12	3500	NA	NA				
1	100	101	12	12	5	4000	12	4000	NA	NA				
1	100	100	12	12	5	4500	12	4500	NA	NA				
1	100	011	12	12	5	5000	12	5000	NA	NA				
1	100	010	5	15	5	500	9	500	12	500	15	500	NA	NA
1	100	001	5	15	5	1000	9	1000	12	1000	15	1000	NA	NA
1	100	000	5	15	5	1500	9	1500	12	1500	15	1500	NA	NA

Table_Sel Setting	PSEL2 Setting	PSEL1 Setting	Min. V	Max. V	PDO1		PDO2		PDO3		PDO4		PDO5	
					V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)
1	011	111	5	15	5	2000	9	2000	12	2000	15	2000	NA	NA
1	011	110	5	15	5	2500	9	2500	12	2500	15	2500	NA	NA
1	011	101	5	15	5	3000	9	3000	12	3000	15	3000	NA	NA
1	011	100	5	15	5	3500	9	3500	12	3500	15	3500	NA	NA
1	011	011	5	15	5	4000	9	4000	12	4000	15	4000	NA	NA
1	011	010	5	15	5	4500	9	4500	12	4500	15	4500	NA	NA
1	011	001	5	15	5	5000	9	5000	12	5000	15	5000	NA	NA
1	011	000	15	15	5	1000	15	1000	NA	NA				
1	010	111	15	15	5	1500	15	1500	NA	NA				
1	010	110	15	15	5	2000	15	2000	NA	NA				
1	010	101	15	15	5	2500	15	2500	NA	NA				
1	010	100	15	15	5	3000	15	3000	NA	NA				
1	010	011	15	15	5	3500	15	3500	NA	NA				
1	010	010	15	15	5	4000	15	4000	NA	NA				
1	010	001	15	15	5	4500	15	4500	NA	NA				
1	010	000	15	15	5	5000	15	5000	NA	NA				
1	001	111	5	20	5	1000	9	1000	12	1000	15	1000	20	1000
1	001	110	5	20	5	2000	9	2000	12	2000	15	2000	20	2000
1	001	101	5	20	5	2500	9	2500	12	2500	15	2500	20	2500
1	001	100	5	20	5	3000	9	3000	12	3000	15	3000	20	3000
1	001	011	5	20	5	3500	9	3500	12	3500	15	3500	20	3500
1	001	010	5	20	5	4000	9	4000	12	4000	15	4000	20	4000
1	001	001	5	20	5	4500	9	4500	12	4500	15	4500	20	4500
1	001	000	5	20	5	5000	9	5000	12	5000	15	5000	20	5000
1	000	111	20	20	5	1000	20	1000	NA	NA				
1	000	110	20	20	5	2000	20	2000	NA	NA				
1	000	101	20	20	5	2500	20	2500	NA	NA				
1	000	100	20	20	5	3000	20	3000	NA	NA				
1	000	011	20	20	5	3500	20	3500	NA	NA				
1	000	010	20	20	5	4000	20	4000	NA	NA				
1	000	001	20	20	5	4500	20	4500	NA	NA				
1	000	000	20	20	5	5000	20	5000	NA	NA				

Table 0

Table_Sel Setting	PSEL2 Setting	PSEL1 Setting	Min. V	Max. V	PDO1		PDO2		PDO3		PDO4		PDO5	
					V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)
0	111	111	5	5	5	500	NA	NA						
0	111	110	5	5	5	1500	NA	NA						
0	111	101	5	5	5	2000	NA	NA						
0	111	100	5	5	5	3000	NA	NA						
0	111	011	5	9	5	1500	9	830	NA	NA				
0	111	010	5	9	5	2000	9	1110	NA	NA				
0	111	001	5	9	5	3000	9	1660	NA	NA				
0	111	000	5	9	5	4000	9	2220	NA	NA				
0	110	111	5	9	5	5000	9	2770	NA	NA				
0	110	110	5	12	5	1500	9	830	12	620	NA	NA		
0	110	101	5	12	5	2000	9	1110	12	830	NA	NA		
0	110	100	5	12	5	3000	9	1660	12	1250	NA	NA		
0	110	011	5	12	5	4000	9	2220	12	1660	NA	NA		
0	110	010	5	12	5	5000	9	2770	12	2080	NA	NA		
0	110	001	5	15	5	1500	9	830	12	620	15	500	NA	NA
0	110	000	5	15	5	2000	9	1110	12	830	15	660	NA	NA
0	101	111	5	15	5	3000	9	1660	12	1250	15	1000	NA	NA
0	101	110	5	15	5	4000	9	2220	12	1660	15	1330	NA	NA
0	101	101	5	15	5	5000	9	2770	12	2080	15	1660	NA	NA
0	101	100	5	20	5	1500	9	830	12	620	15	500	20	370
0	101	011	5	20	5	2000	9	1110	12	830	15	660	20	500
0	101	010	5	20	5	3000	9	1660	12	1250	15	1000	20	750
0	101	001	5	20	5	4000	9	2220	12	1660	15	1330	20	1000
0	101	000	5	20	5	5000	9	2770	12	2080	15	1660	20	1250
0	100	111	9	12	5	1800	9	1000	12	750	NA	NA		
0	100	110	9	12	5	2400	9	1330	12	1000	NA	NA		
0	100	101	9	12	5	3600	9	2000	12	1500	NA	NA		
0	100	100	9	12	5	4800	9	2660	12	2000	NA	NA		
0	100	011	9	12	5	5000	9	3000	12	2250	NA	NA		
0	100	010	9	12	5	5000	9	4000	12	3000	NA	NA		
0	100	001	9	12	5	5000	9	5000	12	3750	NA	NA		
0	100	000	9	15	5	1800	9	1000	12	750	15	600	NA	NA
0	011	111	9	15	5	3000	9	1660	12	1250	15	1000	NA	NA
0	011	110	9	15	5	4000	9	2220	12	1660	15	1330	NA	NA
0	011	101	9	15	5	5000	9	3000	12	2250	15	1800	NA	NA
0	011	100	9	15	5	5000	9	4000	12	3000	15	2400	NA	NA

Table_Sel Setting	PSEL2 Setting	PSEL1 Setting	Min. V	Max. V	PDO1		PDO2		PDO3		PDO4		PDO5	
					V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)	V (V)	I (mA)
0	011	011	9	15	5	5000	9	5000	12	3750	15	3000	NA	NA
0	011	010	9	20	5	1800	9	1000	12	750	15	600	20	450
0	011	001	9	20	5	3000	9	1660	12	1250	15	1000	20	750
0	011	000	9	20	5	4000	9	2220	12	1660	15	1330	20	1000
0	010	111	9	20	5	5000	9	3000	12	2250	15	1800	20	1350
0	010	110	9	20	5	5000	9	4000	12	3000	15	2400	20	1800
0	010	101	9	20	5	5000	9	5000	12	3750	15	3000	20	2250
0	010	100	12	15	5	2000	12	830	15	660	NA	NA		
0	010	011	12	15	5	3000	12	1250	15	1000	NA	NA		
0	010	010	12	15	5	4800	12	2000	15	1600	NA	NA		
0	010	001	12	15	5	5000	12	2500	15	2000	NA	NA		
0	010	000	12	15	5	5000	12	3000	15	2400	NA	NA		
0	001	111	12	15	5	5000	12	3750	15	3000	NA	NA		
0	001	110	12	15	5	5000	12	5000	15	4000	NA	NA		
0	001	101	12	20	5	2000	12	830	15	660	20	500	NA	NA
0	001	100	12	20	5	3000	12	1250	15	1000	20	750	NA	NA
0	001	011	12	20	5	4800	12	2000	15	1600	20	1200	NA	NA
0	001	010	12	20	5	5000	12	3000	15	2400	20	1800	NA	NA
0	001	001	12	20	5	5000	12	3750	15	3000	20	2250	NA	NA
0	001	000	12	20	5	5000	12	5000	15	4000	20	3000	NA	NA
0	000	111	15	20	5	2000	15	660	20	500	NA	NA		
0	000	110	15	20	5	3000	15	1000	20	750	NA	NA		
0	000	101	15	20	5	4000	15	1330	20	1000	NA	NA		
0	000	100	15	20	5	5000	15	1660	20	1250	NA	NA		
0	000	011	15	20	5	5000	15	2000	20	1500	NA	NA		
0	000	010	15	20	5	5000	15	3000	20	2250	NA	NA		
0	000	001	15	20	5	5000	15	4000	20	3000	NA	NA		
0	000	000	15	20	5	5000	15	5000	20	3750	NA	NA		

Path Option

Path Option Setting	Resistance between Path_Opt and GND (unit : kΩ)	0x3F[2:0]	Behavior	HV Bound	LV Bound
Option 7	Open	111b	The same with Path option = 000	The same with Path option 0	The same with Path option 0
Option 6	887	110b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	20V	5V
Option 5	649	101b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	15V	5V
Option 4	453	100b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	12V	5V
Option 3	324	011b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	9V	5V
Option 2	143	010b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	5V	5V
Option 1	56.2	001b	PATHEN is low no matter if Sink PDO is matched with Source DPO.	Depending on Max. V of the Sink capability	1. Match : Depending on the requested PDO. 2. Mismatch : 5V
Option 0	0	000b	1. Match : PATHEN is low. 2. Mismatch : PATHEN is high.	Depending on Max. V of the Sink capability	1. Match : Depending on the requested PDO. 2. Mismatch : 5V

The RT1719 will compare the source ability with the sink capability according to Table_Sel, PSEL2, and PSEL1. The match condition is that the one voltage in source ability exactly meets the one in sink capability and the current of the voltage in source ability is higher or equal to the current of the voltage in sink capability.

Source Type		No Rp (VBUS Only)	Type-C Only	PD
Source Ability	Voltage	5V	5V	Depending on “Source_Capabilities”
	Current	500mA	Depending on Rp	Depending on “Source_Capabilities”

HV Bound and LV Bound

When VBUS is higher than HV bound, PATHEN will be floating to turn off PMOS for power path, CC pins will be open and INT_VBUS_HV will be 1b (0x33[7] = 1b). When VBUS is lower than LV bound, PATHEN will be floating to turn off PMOS for power path and INT_VBUS_LV will be 1b (0x33[6] = 1b).

MCU Control

The system master can get port information and access PD message through I^2C bus. The followings introduce CC status, DR Swap, reading Source Capability, Request Source PDO, and editing Sink Capability Extend.

- **CC Status**

  The CC status is reported in register 0x38[3:0]. Please refer to the register map for more detail information.

- **DR Swap**

  Except for responding to DR Swap automatically according to USB setting (at pin 13), the system master can initiate DR Swap by writing 0x03[7] = 1b. Please make sure that the DR Swap is supported (0x3E[1:0] = 11b) before initiate DR Swap (0x03[7] = 1b) or I^2C error will be triggered (0x30[0] = 1b.) If Rp = 1.5A at PD3.0, initiating DR Swap (0x30[7] = 1b) will also trigger I^2C error (0x30[0] = 1b). After initiating DR Swap successfully, there will be four results as reported in 0x34[7:4].

Address	Bit	Bit Name	Default	Type	Description
0x03	7	TX_DRSWAP	0	RW	Initiated Date Role Swap request to source. To request change data role from DFP to UFP or UFP to DFP is controlled by MCU. Requesting Data Role Swap when USBSET configuration to not a dual role data will trigger INT_I2C_ERR. Requesting Data Role Swap when TXNG(RP 1.5A) and negotiated at PD3.0 will trigger INT_I2C_ERR. 0 : No DR_Swap sent. (default) 1 : DR_Swap sent and then 0x03[7] returns to 0b.
0x2E	7	M_DRSW_ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	6	M_DRSW_REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	5	M_DRSW_WAIT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	4	M_DRSW_TIMEOUT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
0x30	0	M_I2C_ERR	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked

Address	Bit	Bit Name	Default	Type	Description
0x34	7	INT_DRSW_ACCEPT	0	WC	0 : No DR_Swap transmitted, or Accept not received. Cleared. (default) 1 : Transmit DR_Swap and Accept received.
	6	INT_DRSW_REJECT	0	WC	0 : No DR_Swap transmitted, or Reject not received. Cleared. (default) 1 : Transmit DR_Swap and Reject received.
	5	INT_DRSW_WAIT	0	WC	0 : No DR_Swap transmitted, or Wait not received. Cleared. (default) 1 : Transmit DR_Swap and Wait received.
	4	INT_DRSW_TIMEOUT	0	WC	0 : No DR_Swap transmitted. Cleared. (default) 1: Transmit DR_Swap and no any response.
0x36	0	INT_I2C_ERR	0	WC	0 : Cleared (default) 1 : Transmit "Request" with invalid Object setting. E.g. Obj = 0, or Not Existing Obj number. Transmit "DR_Swap" when Pins are configured to not a dual role data. Transmit "Request", "DR_Swap" and "Get_Source_Cap" when RP level is 1.5A in PD 3.0 communication.

- **Reading Source Capability**

  The RT1719 saves the Source Capability in registers from 0x11 to 0x2C. Please refer to “USB Power Delivery Specification” for the more information about Source Capability.

- **Request Source PDO**

  After reading Source Capability, the system master can request the other source PDO through I^2C.

  Set the evaluation mode as evaluating per register setting by 0x03[4] = 1b.

  Set the PDO number in 0x03[2:0].

  Initiate a Request for the source PDO by 0x04[7] = 1b.

  Please note that 0x03[2:0] = 000b or the invalid values (0x03[2:0] = 110b but only five source PDOs) will trigger I^2C error (0x36[0] = 1b).

  After initiating Request successfully, there will be three results as reported in 0x34[3:1].

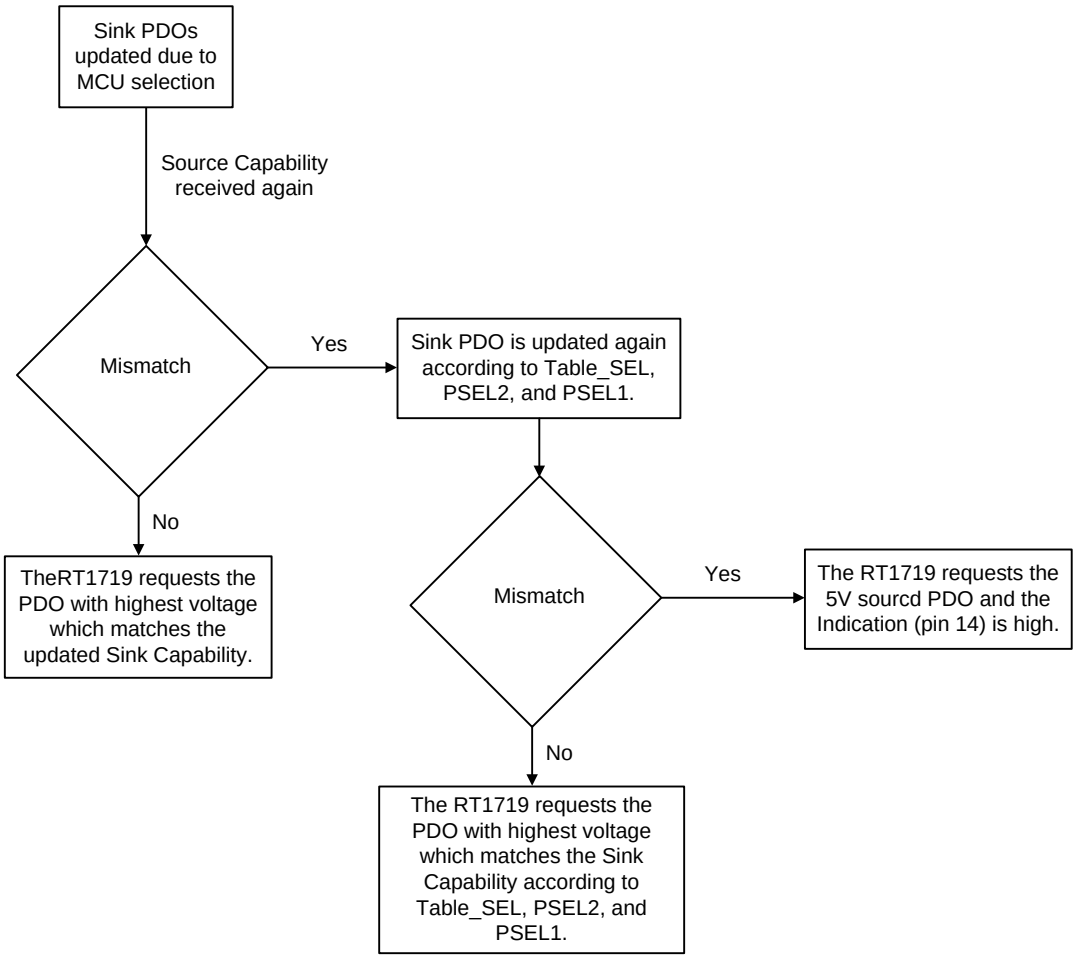
  Besides the response to message, the sink capability will be modified. If the system master requests the first PDO (5V), the sink capability will be modified to 5V/(current is according to 5V Source PDO).

  If the system master requests the other valid PDO (9V for example), the sink capability will be modified to 5V/(current is according to Table_SEL, PSEL2 and PSLE1) and 9V/(current is according to 5V Source PDO).

  The following table shows the update result of related registers.

MCU Selection	MCU Select Current 0x73[1:0] (MSB) and 0x72 (LSB)	MCU Select Voltage 0x75[1:0] (MSB) and 0x74 (LSB)	5V Current 0x77[1:0] (MSB) and 0x76 (LSB)	Currents of other PDO 0x79[1:0] (MSB) and 0x78 (LSB) 0x7B[1:0] (MSB) and 0x7A (LSB) 0x7D[1:0] (MSB) and 0x7C (LSB) 0x7F[1:0] (MSB) and 0x7E (LSB)
The 1st PDO	According to the requested Source PDO	5V	According to the requested Source PDO	0A
The other valid PDO	According to the requested Source PDO	According to the requested Source PDO	According to Table_SEL, PSEL2 and PSEL1	0A

After the sink capability is updated according to MCU selection, the request scenario is shown as the following flow. Please note that if the mismatch happens with the source capability received again, the sink capability will be updated according to (Table_SEL, PSEL2, and PSLE1) and then the RT1719 will compare the sink capability and source capability again.



Address	Bit	Bit Name	Default	Type	Description
0x03	4	EVASCAP_MODE	0	RW	Enable Source Cap evaluation based on the REQ_SRCPDO_NO(0x03[2:0]) or MCU selected capability instead of PSEL. 0 : Evaluation per PSEL setting. (default) 1 : Evaluation per register setting.
	2:0	REQ_SRCPDO_NO	000	RW	Selected SRCPDO number in the request message which is initiated by TX_SPDO_REQ. Set to 000 or invalid object number will trigger INT_I2C_ERR when set TX_SPDO_REQ = 1 000 : No PDO selected (default) 001 : Select the first PDO. … 111 : Select the seventh PDO.
0x04	7	TX_SPDO_REQ	0	RW	Set EVASCAP_MODE = 1 (0x03[4]) when try to initiate Request message to source. Initiated Fixed power supply Request of select SRCPDO (0x03[2:0]) to source. When initiated, it will update Sink Capabilities to 2 objects which contain 5V/PSEL_5V current and selected SRC PDO's voltage/current when REQ_SRCPDO_NO not 1. Or update Sink Capabilities to 1 object which is the same as 1st SRC PDO when REQ_SRCPDO_NO = 1. Requesting TX_SPDO_REQ when TXNG(RP 1.5A) and negotiated at PD3.0 will trigger INT_I2C_ERR. 0 : No Request sent. (default) 1 : Request sent and then 0x04[7] returns to 0b.
0x2E	3	M_REQ_ACCEPT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	2	M_REQ_REJECT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
	1	M_REQ_WAIT	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked
0x30	0	M_I2C_ERR	0	RW	0 : Interrupt masked (default) 1 : Interrupt unmasked

Address	Bit	Bit Name	Default	Type	Description
0x34	3	INT_REQ_ACCEPT	0	WC	0 : No DR_Swap transmitted, or Accept not received. Cleared. (default) 1 : Transmit DR_Swap and Accept received.
	2	INT_REQ_REJECT	0	WC	0 : No DR_Swap transmitted, or Reject not received. Cleared. (default) 1 : Transmit DR_Swap and Reject received.
	1	INT_REQ_WAIT	0	WC	0 : No DR_Swap transmitted, or Wait not received. Cleared. (default) 1 : Transmit DR_Swap and Wait received.
0x36	0	INT_I2C_ERR	0	WC	0 : Cleared (default) 1 : Transmit "Request" with invalid Object setting. E.g. Obj = 0, or Not Existing Obj number. Transmit "DR_Swap" when Pins are configured to not a dual role data. Transmit "Request", "DR_Swap" and "Get_Source_Cap" when RP level is 1.5A in PD 3.0 communication.

- **Editing Sink Capability Extend**

  The system master can modify the Sink Capabilities Extended (0x50 to 0x62) through I^2C (0x65[7] = 1b).

	Content of Sink Capabilities Extended (except for Sink PDP)	Sink PDP
0x65[7] = 0b	From the default values of 0x50 to 0x61 no matter if 0x50 to 0x61 are modified.	According to the Table_SEL, PSEL2, and PSEL1.
0x65[7] = 1b	From the register values of 0x50 to 0x61.	From the register value of 0x62

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3.5x3.5 package, the thermal resistance, θ_{JA}, is 28.5°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (28.5°C/W) = 3.5W for a WQFN-20L 3.5x3.5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

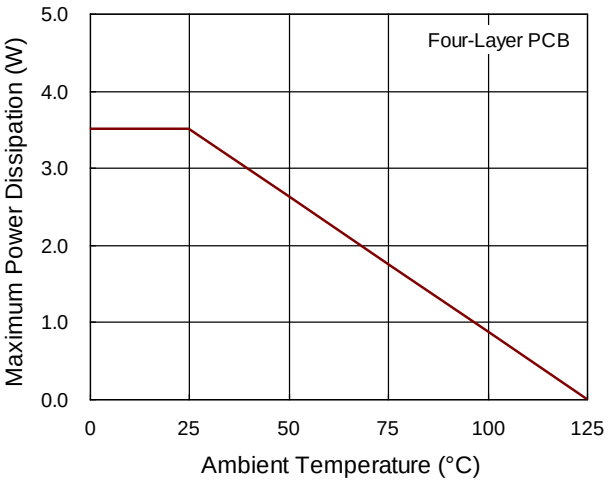
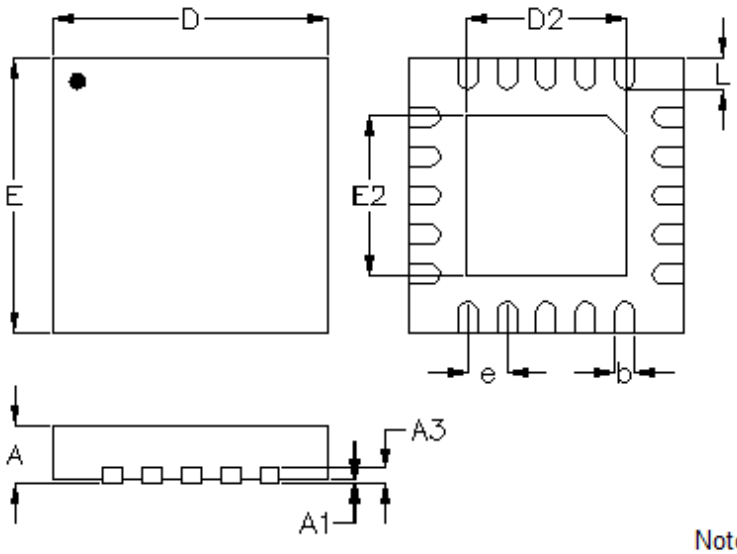
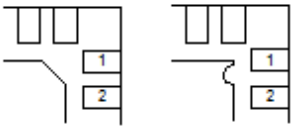


Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

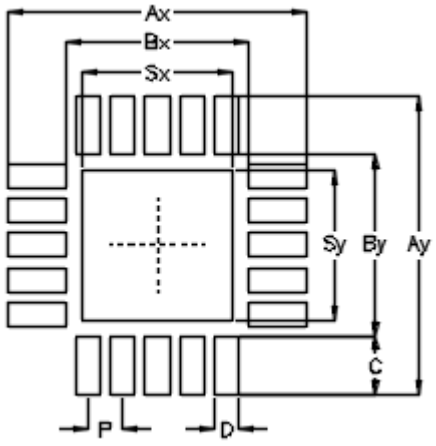
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3.5x3.5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*3.5-20	20	0.50	4.30	4.30	2.60	2.60	0.85	0.35	2.15	2.15	±0.05

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789