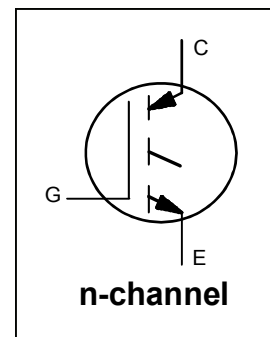


$V_{CES} = 1200V$
 $I_{C(Nominal)} = 5A$
 $T_{J(max)} = 175^{\circ}C$
 $V_{CE(on)} \text{ typ} = 1.7V @ I_C = 5A$



Applications

- Industrial Motor Drives
- UPS
- HEV Inverter
- Welding

| G | C | E |
|------|-----------|---------|
| Gate | Collector | Emitter |

| Features | Benefits |
|---|---|
| Low $V_{CE(on)}$ Trench IGBT Technology | High Efficiency in a Wide Range of Applications |
| Low Switching Losses | Suitable for a Wide Range of Switching Frequencies |
| Very Soft Turn-off Characteristics | Reduced EMI and Overvoltage in Motor Drive Applications |
| 10 μ s Short Circuit SOA | Rugged Transient Performance for Increased Reliability |
| Square RBSOA | |
| Tight Parameter Distribution | Excellent Current Sharing in Parallel Operation |
| Positive $V_{CE(on)}$ Temperature Coefficient | |
| $T_{j(max)} = 175^{\circ}C$ | Increased Reliability |

| Base part number | Package Type | Standard Pack | | Orderable part number |
|------------------|--------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IRG8CH10K10F | Die on Film | Wafer | 1 | IRG8CH10K10F |

Mechanical Parameter

| | | |
|----------------------------------|---|-----------------|
| Die Size | 3.2 x 3.1 | mm ² |
| Minimum Street Width | 95 | μ m |
| Emitter Pad Size | See Die Drawing | mm ² |
| Gate Pad Size | 0.5 x 0.5 | |
| Area Total / Active | 9.79 / 3.33 | |
| Thickness | 140 | μ m |
| Wafer Size | 200 | mm |
| Notch Position | 0 | Degrees |
| Maximum-Possible Chips per Wafer | 2850 pcs. | |
| Passivation Front side | Silicon Nitride, Polyimide | |
| Front Metal | Al, Si (5.6 μ m) | |
| Backside Metal | Al, Ti, Ni, Ag | |
| Die Bond | Electrically conductive epoxy or solder | |
| Reject Ink Dot Size | 0.25 mm diameter minimum | |

Maximum Ratings

| | Parameter | Max. | Units |
|----------------|---|-------------|------------------|
| V_{CE} | Collector-Emitter Voltage, $T_J=25^\circ\text{C}$ | 1200 | V |
| I_C | DC Collector Current | ① | A |
| I_{LM} | Clamped Inductive Load Current ② | 15 | A |
| V_{GE} | Gate Emitter Voltage | ± 30 | V |
| T_J, T_{STG} | Operating Junction and Storage Temperature | -40 to +175 | $^\circ\text{C}$ |

Static Characteristics (Tested on wafers) @ $T_J=25^\circ\text{C}$

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------|--|------|------|-----------|---------------|--|
| $V_{(BR)CES}$ | Collector-to-Emitter Breakdown Voltage | 1200 | — | — | V | $V_{GE} = 0\text{V}, I_C = 250\mu\text{A}$ ③ |
| $V_{CE(sat)}$ | Collector-to-Emitter Saturated Voltage | — | — | 2.0 | | $V_{GE} = 15\text{V}, I_C = 5\text{A}, T_J = 25^\circ\text{C}$ ④ |
| $V_{GE(th)}$ | Gate-Emitter Threshold Voltage | 5.0 | — | 6.5 | | $I_C = 200\mu\text{A}, V_{GE} = V_{CE}$ |
| I_{CES} | Zero Gate Voltage Collector Current | — | 1.0 | 25 | μA | $V_{CE} = 1200\text{V}, V_{GE} = 0\text{V}$ |
| I_{GES} | Gate Emitter Leakage Current | — | — | ± 100 | nA | $V_{CE} = 0\text{V}, V_{GE} = \pm 30\text{V}$ |

Electrical Characteristics (Not subject to production test- Verified by design/characterization)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------|--|-------------|------|------|---------------|--|
| $V_{CE(sat)}$ | Collector-to-Emitter Saturated Voltage | — | 1.7 | — | V | $V_{GE} = 15\text{V}, I_C = 5\text{A}, T_J = 25^\circ\text{C}$ ⑤ |
| | | — | 2.1 | — | | $V_{GE} = 15\text{V}, I_C = 5\text{A}, T_J = 175^\circ\text{C}$ ⑤ |
| SCSOA | Short Circuit Safe Operating Area | 10 | — | — | μs | $V_{GE} = 15\text{V}, V_{CC} = 600\text{V}$ $V_P \leq 1200\text{V}, T_J = 150^\circ\text{C}$ |
| RBSOA | Reverse Bias Safe Operating Area | FULL SQUARE | | | | $T_J = 175^\circ\text{C}, I_C = 15\text{A}$ $V_{CC} = 960\text{V}, V_P \leq 1200\text{V}$ $V_{GE} = +20\text{V to } 0\text{V}$ |
| C_{iss} | Input Capacitance | — | 720 | — | pF | $V_{GE} = 0\text{V}$ |
| C_{oss} | Output Capacitance | — | 30 | — | | $V_{CE} = 30\text{V}$ |
| C_{rss} | Reverse Transfer Capacitance | — | 15 | — | | $f = 1.0\text{MHz}$ |
| Q_g | Total Gate Charge (turn-on) | — | 30 | — | nC | $I_C = 5\text{A}$ ⑤ |
| Q_{ge} | Gate-to-Emitter Charge (turn-on) | — | 1.1 | — | | $V_{GE} = 15\text{V}$ |
| Q_{gc} | Gate-to-Collector Charge (turn-on) | — | 20 | — | | $V_{CC} = 600\text{V}$ |

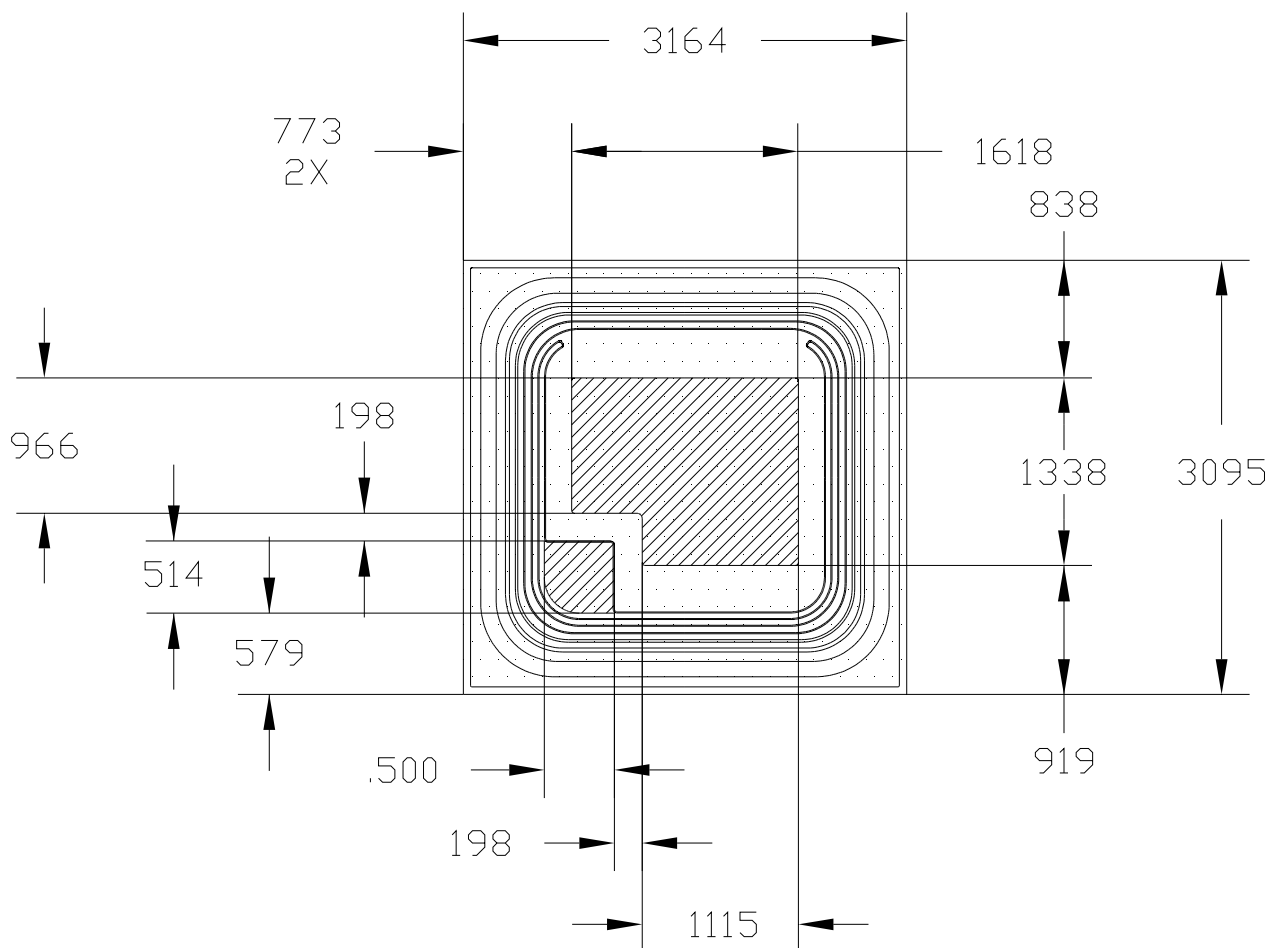
Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)

| | Parameter | Min. | Typ. | Max. | Units | Conditions ⑥ |
|--------------|---------------------|------|------|------|-------|---|
| $t_{d(on)}$ | Turn-On delay time | — | 20 | — | ns | $I_C = 5\text{A}, V_{CC} = 600\text{V}$ $R_G = 47\Omega, V_{GE} = 15\text{V}$ $T_J = 25^\circ\text{C}$ |
| t_r | Rise time | — | 20 | — | | |
| $t_{d(off)}$ | Turn-Off delay time | — | 160 | — | | |
| t_f | Fall time | — | 240 | — | | |
| $t_{d(on)}$ | Turn-On delay time | — | 20 | — | | $I_C = 5\text{A}, V_{CC} = 600\text{V}$ $R_G = 47\Omega, V_{GE} = 15\text{V}$ $T_J = 150^\circ\text{C}$ |
| t_r | Rise time | — | 20 | — | | |
| $t_{d(off)}$ | Turn-Off delay time | — | 300 | — | | |
| t_f | Fall time | — | 290 | — | | |

Notes:

- ① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
- ② $V_{CC} = 80\% (V_{CES}), V_{GE} = 20\text{V}$.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ Actual test limits take into account additional losses in the measurement setup.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ Values influenced by parasitic L and C in measurement.

Die Drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MICRO-METER
2. CONTROLLING DIMENSION: MICRO-METER
3. DIE WIDTH AND LENGTH TOLERANCE: $-50\mu\text{m}$
4. DIE THICKNESS = 140 MICRO-METER

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non-standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Further Information

For further information please contact your local IR Sales office.

Revision History

| Date | Comments |
|------------|--|
| 09/26/2014 | <ul style="list-style-type: none"> • Updated Front Metal from “Al, Si(4um)” to “Al, Si (5.6um)” on page 1. • Removed reference part number from Die drawing on page 3. |
| 06/03/2015 | <ul style="list-style-type: none"> • Updated Switch time on page 2. • Updated IFX logo on page1 & 4. |