

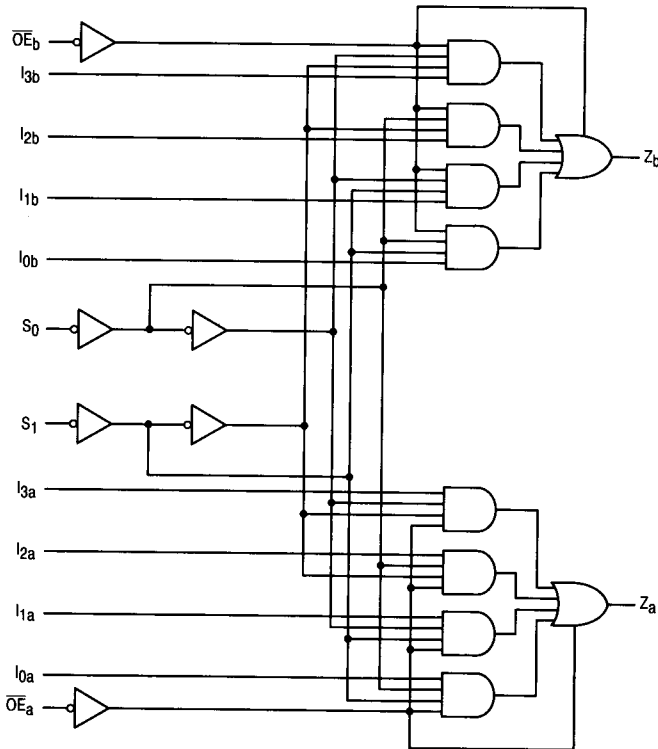


# Dual 4-Input Data Selector/Multiplexer With 3-State Outputs

ELECTRICALLY TESTED PER:  
MIL-M-38510/33908

The 54F253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable  $\overline{OE}$  inputs, allowing the outputs to interface directly with bus oriented systems.

LOGIC DIAGRAM



**Military 54F253**



**AVAILABLE AS:**

- 1) JAN: JM38510/33908BXA
- 2) SMD: N/A
- 3) 883: 54F253/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

**PIN ASSIGNMENTS**

| FUNCT.            | DIL 620-09 | FLATS 650-05 | LCC 756A-02 | BURN-IN (COND. A) |
|-------------------|------------|--------------|-------------|-------------------|
| $\overline{OE}_a$ | 1          | 1            | 2           | VCC               |
| S1                | 2          | 2            | 3           | VCC               |
| I3a               | 3          | 3            | 4           | VCC               |
| I2a               | 4          | 4            | 5           | VCC               |
| I1a               | 5          | 5            | 7           | VCC               |
| I0a               | 6          | 6            | 8           | VCC               |
| Za                | 7          | 7            | 9           | OPEN              |
| GND               | 8          | 8            | 10          | GND               |
| Zb                | 9          | 9            | 12          | OPEN              |
| I0b               | 10         | 10           | 13          | VCC               |
| I1b               | 11         | 11           | 14          | VCC               |
| I2b               | 12         | 12           | 15          | VCC               |
| I3b               | 13         | 13           | 17          | VCC               |
| S0                | 14         | 14           | 18          | VCC               |
| $\overline{OE}_b$ | 15         | 15           | 19          | VCC               |
| VCC               | 16         | 16           | 20          | VCC               |

**BURN-IN CONDITIONS:**  
VCC = 5.0 V MIN/6.0 V MAX

FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-Input Multiplexers with 3-state Outputs. They select two bits from four sources selected by common Select Inputs ( $S_0, S_1$ ). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a, \overline{OE}_b$ ) inputs which when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

| TRUTH TABLE   |       |                 |       |       |       |       |        |
|---------------|-------|-----------------|-------|-------|-------|-------|--------|
| Select Inputs |       | Inputs (a or b) |       |       |       |       | Output |
| $S_0$         | $S_1$ | $\overline{OE}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | Z      |
| X             | X     | H               | X     | X     | X     | X     | (Z)    |
| L             | L     | L               | L     | X     | X     | X     | L      |
| L             | L     | L               | H     | X     | X     | X     | H      |
| H             | L     | L               | X     | L     | X     | X     | L      |
| H             | L     | L               | X     | H     | X     | X     | H      |
| L             | H     | L               | X     | X     | L     | X     | L      |
| L             | H     | L               | X     | X     | H     | X     | H      |
| H             | H     | L               | X     | X     | X     | L     | L      |
| H             | H     | L               | X     | X     | X     | H     | H      |

H = HIGH Voltage Level

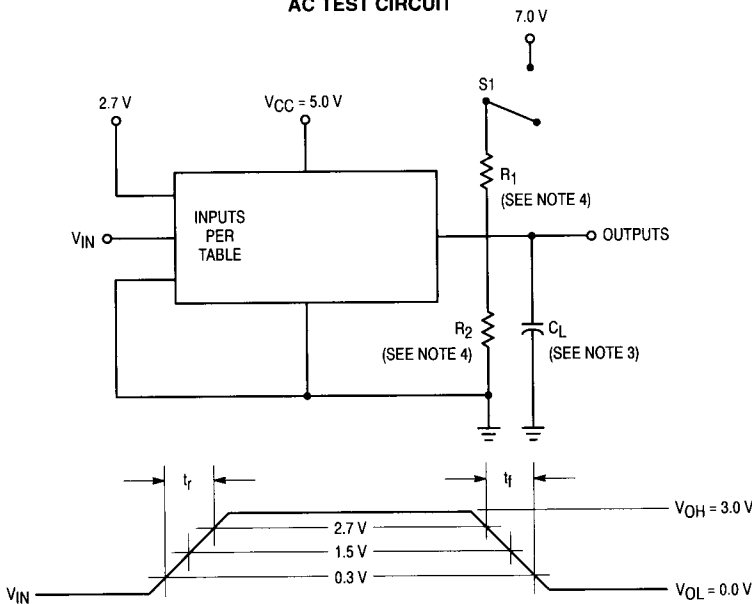
L = LOW Voltage Level

X = Immaterial

Z = High Impedance (off)

Address inputs  $S_0$  and  $S_1$  are common to both sections.

AC TEST CIRCUIT

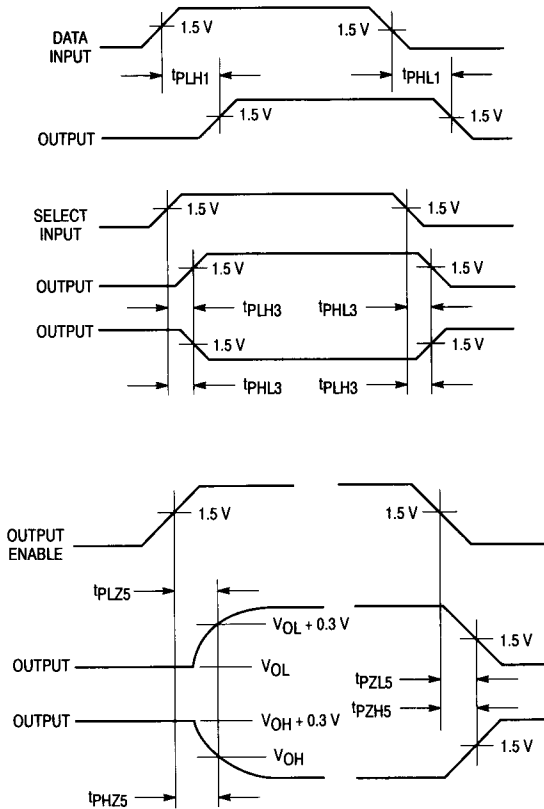


| Test Type | $S_1$  |
|-----------|--------|
| $t_{PLH}$ | open   |
| $t_{PHL}$ | open   |
| $t_{PHZ}$ | open   |
| $t_{PZH}$ | open   |
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |

REFERENCE NOTES ON PAGE 4-130

# 54F253

## WAVEFORMS



### NOTES

1.  $V_{IN}$  = input pulse and has the following characteristics:  
 $PRR \leq 1.0 \text{ MHz}$ ,  $t_r = t_f \leq 2.5 \text{ ns}$ ,  $Z_{OUT} \approx 50 \Omega$
2. Terminal conditions (pins not designated may be high  $\geq 2.0 \text{ V}$ , low  $\leq 0.8 \text{ V}$ , or open).
3.  $C_L = 50 \text{ pF} \pm 10\%$ , including scope probe, wiring and stray capacitance without package in test fixture.
4.  $R_1 = R_2 = 499 \Omega \pm 5.0\%$ .
5. Voltage measurements are to be made with respect to network ground terminal.

## 54F253

| Symbol           | Parameter                    | Limits     |      |             |      |             |      | Unit | Test Condition<br>(Unless Otherwise Specified)                                                                                             |
|------------------|------------------------------|------------|------|-------------|------|-------------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------|
|                  |                              | + 25°C     |      | + 125°C     |      | - 55°C      |      |      |                                                                                                                                            |
|                  |                              | Subgroup 1 |      | Subgroup 2  |      | Subgroup 3  |      |      |                                                                                                                                            |
|                  |                              | Min        | Max  | Min         | Max  | Min         | Max  |      |                                                                                                                                            |
| V <sub>OH</sub>  | Logical "1" Output Voltage   | 2.4        |      | 2.4         |      | 2.4         |      | V    | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3.0 mA, V <sub>IH</sub> = 2.0 V, S = 0.8 V or 2.0 V, $\overline{OE}$ = 0.8 V or open.          |
| V <sub>OL</sub>  | Logical "0" Output Voltage   |            | 0.5  |             | 0.5  |             | 0.5  | V    | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IL</sub> = 0.8 V, S = 0.8 V or 2.0 V, $\overline{OE}$ = 0.8 V or open.            |
| V <sub>IC</sub>  | Input Clamp Diode            |            | -1.2 |             |      |             |      | V    | V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.                                                                  |
| I <sub>IH</sub>  | Logical "1" Input Current    |            | 20   |             | 20   |             | 20   | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open, S = 4.5 V, 0 V or (2.7 V).                                        |
| I <sub>IHH</sub> | Logical "1" Input Current    |            | 100  |             | 100  |             | 100  | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, other inputs are open, S = 4.5 V, 0 V or (7.0 V).                                       |
| I <sub>IL</sub>  | Logical "0" Input Current    | -0.03      | -0.6 | -0.03       | -0.6 | -0.03       | -0.6 | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V, other inputs are open, S = 4.5 V, 0 V or (0.5 V).                                        |
| I <sub>OD</sub>  | Diode Current                | 35         |      | 35          |      | 35          |      | mA   | V <sub>CC</sub> = 4.5 V, V <sub>IN</sub> = 0 V, S = 0 V, other inputs are open, V <sub>OUT</sub> = 2.5 V, $\overline{OE}$ = 0 V.           |
| I <sub>OS</sub>  | Output Short Circuit Current | -60        | -150 | -60         | -150 | -60         | -150 | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, all other inputs are open, V <sub>OUT</sub> = 0 V, S = 0 V, $\overline{OE}$ = 0 V.       |
| I <sub>OZH</sub> | Output Off Current High      |            | 50   |             | 50   |             | 50   | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V, all other inputs are open, V <sub>OUT</sub> = 2.7 V, S = 0 V, $\overline{OE}$ = 2.0 V.     |
| I <sub>OZL</sub> | Output Off Current Low       |            | -50  |             | -50  |             | -50  | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, all other inputs are open, V <sub>OUT</sub> = 0.5 V, S = 4.5 V, $\overline{OE}$ = 2.0 V. |
| I <sub>CCH</sub> | Power Supply Current         |            | 16   |             | 16   |             | 16   | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V or 0 V (all inputs).                                                                      |
| I <sub>CCL</sub> | Power Supply Current         |            | 23   |             | 23   |             | 23   | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (all inputs).                                                                               |
| I <sub>CCZ</sub> | Power Supply Current         |            | 23   |             | 23   |             | 23   | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (all inputs), $\overline{OE}$ = 4.5 V.                                                      |
| V <sub>IH</sub>  | Logical "1" Input Voltage    | 2.0        |      | 2.0         |      | 2.0         |      | V    | V <sub>CC</sub> = 4.5 V.                                                                                                                   |
| V <sub>IL</sub>  | Logical "0" Input Voltage    |            | 0.8  |             | 0.8  |             | 0.8  | V    | V <sub>CC</sub> = 4.5 V.                                                                                                                   |
|                  | Functional Tests             | Subgroup 7 |      | Subgroup 8A |      | Subgroup 8B |      |      | per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at) V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.4 V. |
|                  |                              |            |      |             |      |             |      |      |                                                                                                                                            |

## 54F253

| Symbol            | Parameter                                                                               | Limits     |      |             |     |             |     | Unit | Test Condition<br>(Unless Otherwise Specified)                                               |
|-------------------|-----------------------------------------------------------------------------------------|------------|------|-------------|-----|-------------|-----|------|----------------------------------------------------------------------------------------------|
|                   |                                                                                         | + 25°C     |      | + 125°C     |     | - 55°C      |     |      |                                                                                              |
|                   |                                                                                         | Subgroup 9 |      | Subgroup 10 |     | Subgroup 11 |     |      |                                                                                              |
|                   |                                                                                         | Min        | Max  | Min         | Max | Min         | Max |      |                                                                                              |
| t <sub>PHL1</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> to Z <sub>n</sub>                   | 2.5        | 7.0  | 2.5         | 8.0 | 2.5         | 8.0 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PLH1</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> to Z <sub>n</sub>                   | 3.0        | 7.0  | 2.5         | 9.0 | 2.5         | 9.0 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PHL3</sub> | Propagation Delay<br>/Data-Output<br>S <sub>n</sub> to Z <sub>n</sub>                   | 3.0        | 9.0  | 2.5         | 11  | 2.5         | 11  | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PLH3</sub> | Propagation Delay<br>/Data-Output<br>S <sub>n</sub> to Z <sub>n</sub>                   | 4.5        | 11.5 | 3.5         | 15  | 3.5         | 15  | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PZH5</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> or S <sub>n</sub> to Z <sub>n</sub> | 3.0        | 8.0  | 2.5         | 10  | 2.5         | 10  | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PZL5</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> or S <sub>n</sub> to Z <sub>n</sub> | 3.0        | 8.0  | 2.5         | 10  | 2.5         | 10  | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PHZ5</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> or S <sub>n</sub> to Z <sub>n</sub> | 2.0        | 5.0  | 2.0         | 6.5 | 2.0         | 6.5 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |
| t <sub>PLZ5</sub> | Propagation Delay<br>/Data-Output<br>I <sub>n</sub> or S <sub>n</sub> to Z <sub>n</sub> | 2.0        | 6.0  | 2.0         | 8.0 | 2.0         | 8.0 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = R <sub>2</sub> = 499 Ω. |

4