

74F651 • 74F652 Transceivers/Registers

General Description

These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
 - 'F651 inverting
 - 'F652 non-inverting
- Guaranteed 4000V minimum ESD protection

Ordering Code:

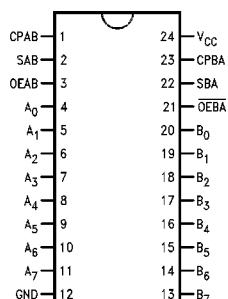
| Commercial | Military | Package Number | Package Description |
|-------------------|--------------------|----------------|---|
| 74F651SPC | | N24C | 24-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F651SDM (Note 2) | J24F | 24-Lead (0.300" Wide) Ceramic Dual-In-Line |
| 74F651SC (Note 1) | | M24B | 24-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| | 54F651FM (Note 2) | W24C | 24-Lead Cerpack |
| | 54F651LM (Note 2) | E28A | 24-Lead Ceramic Leadless Chip Carrier, Type C |
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Note 1: Devices also available in 13" reel. Use suffix = SCX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

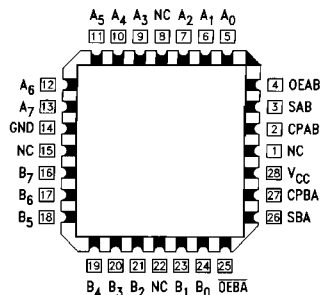
Connection Diagrams

Pin Assignment
DIP, SOIC and Flatpak



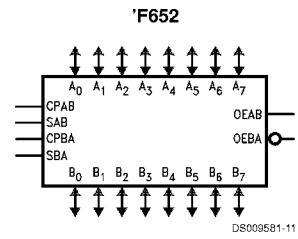
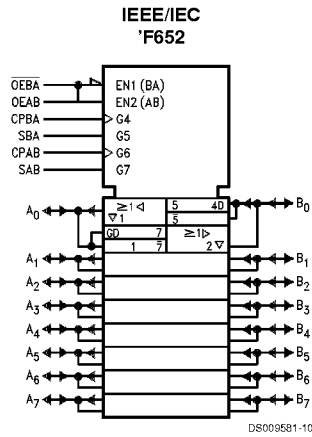
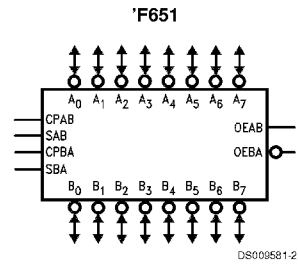
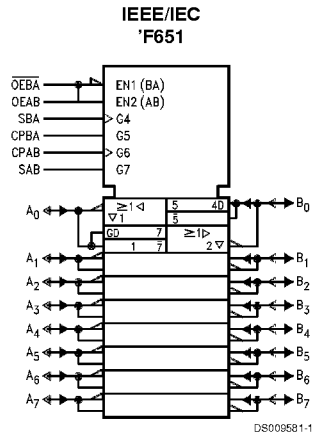
DS009581-3

Pin Assignment
for LCC



DS009581-4

Logic Symbols

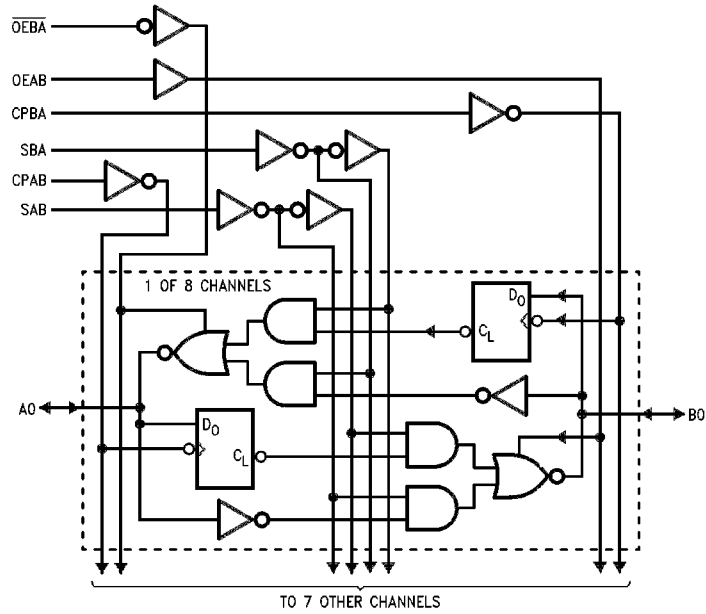


Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|-------------------------------|------------------------------------|---------------------------|---|
| | | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| A_0 - A_7 , B_0 - B_7 | A and B Inputs/ 3-STATE Outputs | 1.0/1.0 600/106.6 (80) | 20 μA /-0.6 mA -12 mA/64 mA (48 mA) |
| CPAB, CPBA | Clock Inputs | 1.0/1.0 | 20 μA /-0.6 mA |
| SAB, SBA | Select Inputs | 1.0/1.0 | 20 μA /-0.6 mA |
| OEAB, OEBA | Output Enable Inputs | 1.0/1.0 | 20 μA /-0.6 mA |

Logic Diagrams

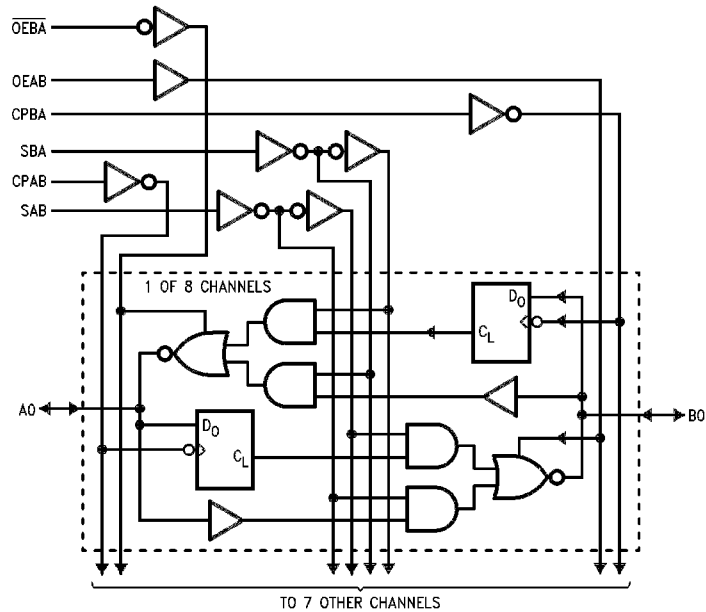
'F652



DS006581-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'F651



DS006581-12

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

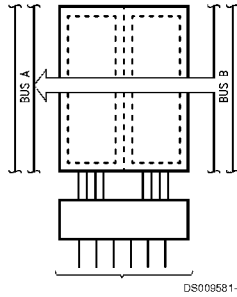
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropri-

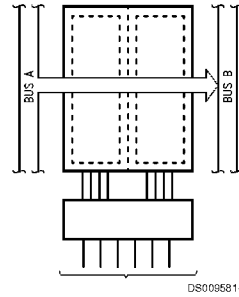
ate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note A: Real-Time Transfer Bus B to Bus A



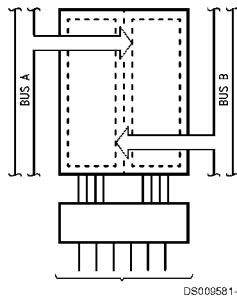
| OEAB | OEBA | CPAB | CPBA | SAB | SBA |
|------|------|------|------|-----|-----|
| L | L | X | X | X | L |

Note B: Real-Time Transfer Bus A to Bus B



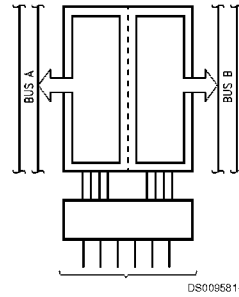
| OEAB | OEBA | CPAB | CPBA | SAB | SBA |
|------|------|------|------|-----|-----|
| H | H | X | X | L | X |

Note C: Storage



| OEAB | OEBA | CPAB | CPBA | SAB | SBA |
|------|------|------|------|-----|-----|
| X | H | ↗ | X | X | X |
| L | X | X | ↗ | X | X |
| L | H | ↗ | ↗ | X | X |

Note D: Transfer Storage Data to A or B



| OEAB | OEBA | CPAB | CPBA | SAB | SBA |
|------|------|--------|--------|-----|-----|
| H | L | H or L | H or L | H | X |

FIGURE 1.

Functional Description (Continued)

| Inputs | | | | | | Inputs/Outputs (Note 3) | | Operating Mode |
|--------|------|--------|--------|-----|-----|------------------------------------|------------------------------------|--|
| OEAB | OEBA | CPAB | CPBA | SAB | SBA | A ₀ thru A ₇ | B ₀ thru B ₇ | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↗ | ↗ | X | X | | | Store A and B Data |
| X | H | ↗ | H or L | X | X | Input | Not Specified | Store A, Hold B |
| H | H | ↗ | ↗ | X | X | Input | Output | Store A in Both Registers |
| L | X | H or L | ↗ | X | X | Not Specified | Input | Hold A, Store B |
| L | L | ↗ | ↗ | X | X | Output | Input | Store B in Both Registers |
| L | L | X | X | X | L | Output | Input | Real-Time B Data to A Bus |
| L | L | X | H or L | X | H | | | Store B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real-Time A Data to B Bus |
| H | H | H or L | X | H | X | | | Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW to HIGH Clock Transition

Note 3: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 4)

| | |
|---|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 5) | -0.5V to +7.0V |
| Input Current (Note 5) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |

ESD Last Passing Voltage (Min)

4000V

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 5: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

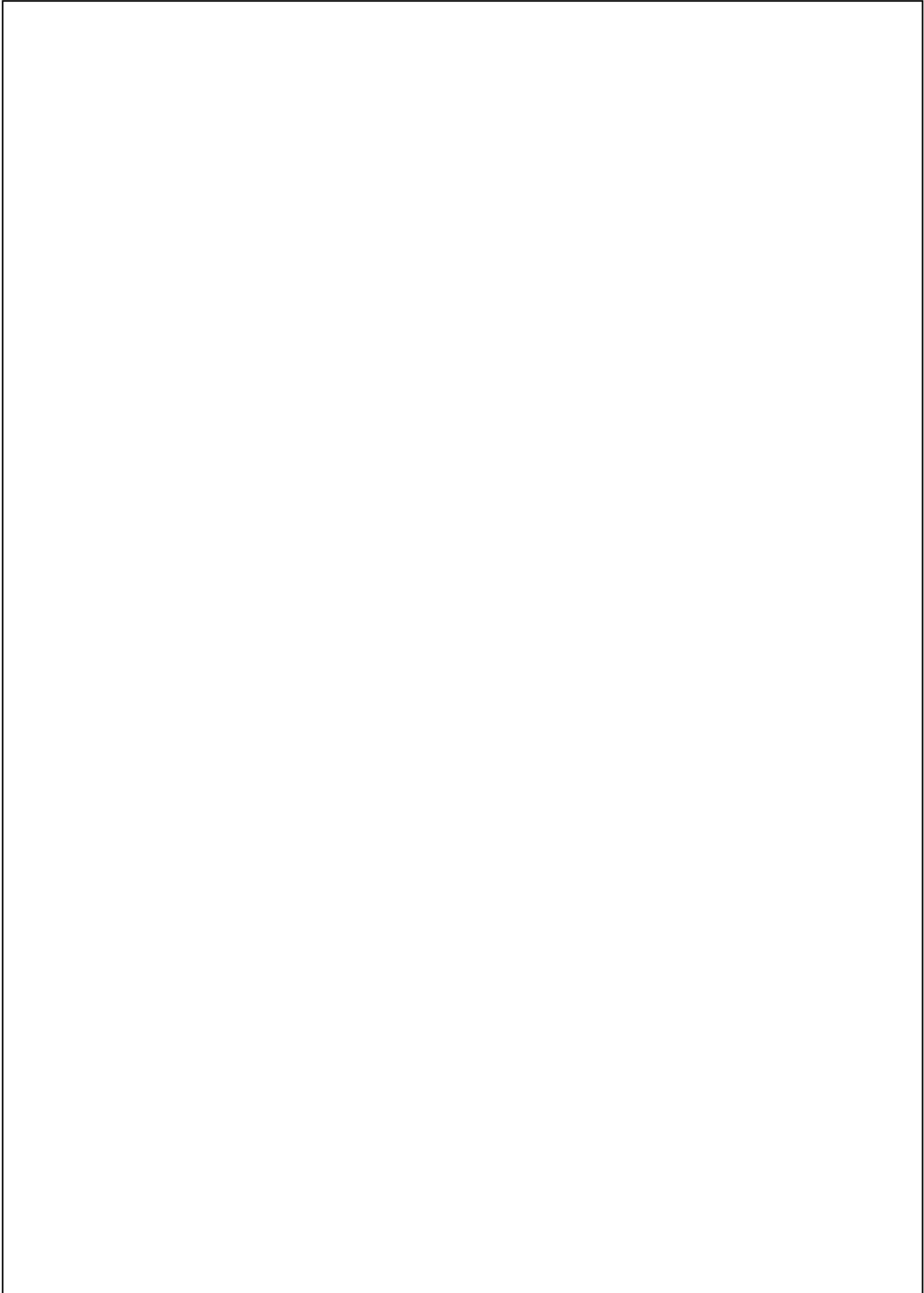
| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------------------------|------------------------------------|-------------------------|------|------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | | V | Min | I _{IN} = -18 mA (Non I/O Pins) |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} | 2.0 | | V | Min | I _{OH} = -12 mA (A _n , B _n) |
| | 74F 10% V _{CC} | 2.0 | | | | | I _{OH} = -15 mA (A _n , B _n) |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} | 0.55 | | V | Min | I _{OL} = 48 mA (A _n , B _n) |
| | 74F 10% V _{CC} | 0.55 | | | | | I _{OL} = 64 mA (A _n , B _n) |
| I _{IH} | Input HIGH Current | 54F | 20.0 | | μA | Max | V _{IN} = 2.7V |
| | 74F | 5.0 | | | | | (Non I/O Pins) |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F | 100 | | μA | Max | V _{IN} = 7.0V |
| | 74F | 7.0 | | | | | |
| I _{BVIT} | Input HIGH Current Breakdown (I/O) | 54F | 1.0 | | mA | Max | V _{IN} = 5.5V |
| | 74F | 0.5 | | | | | (A _n , B _n) |
| I _{CEX} | Output HIGH Leakage Current | 54F | 250 | | μA | Max | V _{OUT} = V _{CC} |
| | 74F | 50 | | | | | |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA |
| | | | | | | | All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | 3.75 | | μA | 0.0 | V _{I_{OD}} = 150 mV |
| | | | | | | | All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | | mA | Max | V _{IN} = 0.5V (Non I/O Pins) |
| I _{IH} + I _{OZH} | Output Leakage Current | | | | μA | Max | V _{OUT} = 2.7V (A _n , B _n) |
| I _{IL} + I _{OZL} | Output Leakage Current | | | | μA | Max | V _{OUT} = 0.5V (A _n , B _n) |
| I _{OS} | Output Short-Circuit Current | -100 | | -225 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | 105 | | 135 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | 118 | | 150 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | 115 | | 150 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics

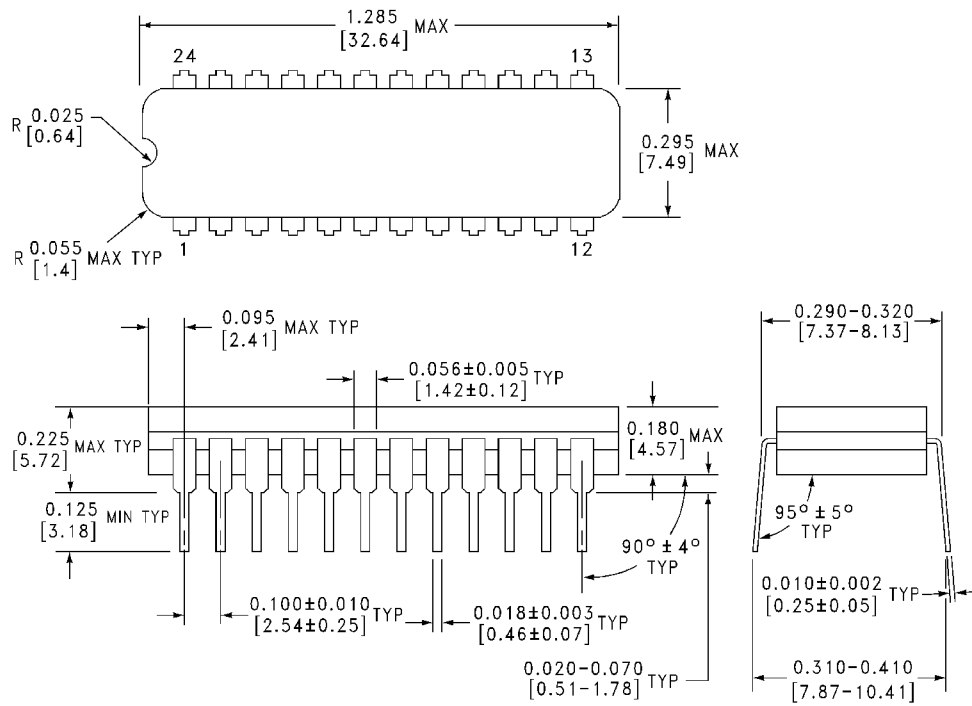
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|------------------|----------------------|--|-----|--|------|--|-----|-------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | $T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$ | | $T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$ | | |
| | | Min | Max | Min | Max | Min | Max | |
| f_{max} | Max. Clock Frequency | 90 | | 75 | | 90 | | MHz |
| t_{PLH} | Propagation Delay | 2.0 | 7.0 | 2.0 | 8.5 | 2.0 | 8.0 | ns |
| t_{PHL} | Clock to Bus | 2.0 | 8.0 | 2.0 | 9.5 | 2.0 | 9.0 | |
| t_{PLH} | Propagation Delay | 2.0 | 8.5 | 1.0 | 9.0 | 2.0 | 9.0 | ns |
| t_{PHL} | Bus to Bus ('F651) | 1.0 | 7.5 | 1.0 | 8.0 | 1.0 | 8.0 | |
| t_{PLH} | Propagation Delay | 1.0 | 7.0 | 1.0 | 8.0 | 1.0 | 7.5 | ns |
| t_{PHL} | Bus to Bus ('F652) | 1.0 | 6.5 | 1.0 | 8.0 | 1.0 | 7.0 | |
| t_{PLH} | Propagation Delay | 2.0 | 8.5 | 2.0 | 11.0 | 2.0 | 9.5 | ns |
| t_{PHL} | SBA or SAB to A or B | 2.0 | 8.0 | 2.0 | 10.0 | 2.0 | 9.0 | |

AC Operating Requirements

| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|------------------|---------------------|--|------|----------------------------|------|----------------------------|------|-------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ | | $T_A, V_{CC} = \text{Mil}$ | | $T_A, V_{CC} = \text{Com}$ | | |
| | | Min | Max | Min | Max | Min | Max | |
| t_{PZH} | Enable Time | 2.0 | 9.5 | 2.0 | 10.0 | 2.0 | 10.0 | ns |
| t_{PZL} | *OEBA to A | 2.0 | 12.0 | 2.0 | 10.0 | 2.0 | 12.5 | |
| t_{PHZ} | Disable Time | 1.0 | 7.5 | 1.0 | 9.0 | 1.0 | 8.0 | |
| t_{PLZ} | *OEBA to A | 2.0 | 8.5 | 1.0 | 9.0 | 2.0 | 9.0 | |
| t_{PZH} | Enable Time | 2.0 | 9.5 | 2.0 | 10.0 | 2.0 | 10.0 | |
| t_{PZL} | OEAB to B | 3.0 | 13.0 | 2.0 | 12.0 | 3.0 | 14.0 | |
| t_{PHZ} | Disable Time | 2.0 | 9.0 | 1.0 | 9.0 | 2.0 | 10.0 | ns |
| t_{PLZ} | OEAB to B | 2.0 | 10.5 | 1.0 | 12.0 | 2.0 | 11.0 | |
| $t_s(\text{H})$ | Setup Time, HIGH or | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_s(\text{L})$ | LOW, Bus to Clock | 5.0 | | 5.0 | | 5.0 | | |
| $t_h(\text{H})$ | Hold Time, HIGH or | 2.0 | | 2.5 | | 2.0 | | ns |
| $t_h(\text{L})$ | LOW, Bus to Clock | 2.0 | | 2.5 | | 2.0 | | |
| $t_w(\text{H})$ | Clock Pulse Width | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_w(\text{L})$ | HIGH or LOW | 5.0 | | 5.0 | | 5.0 | | |



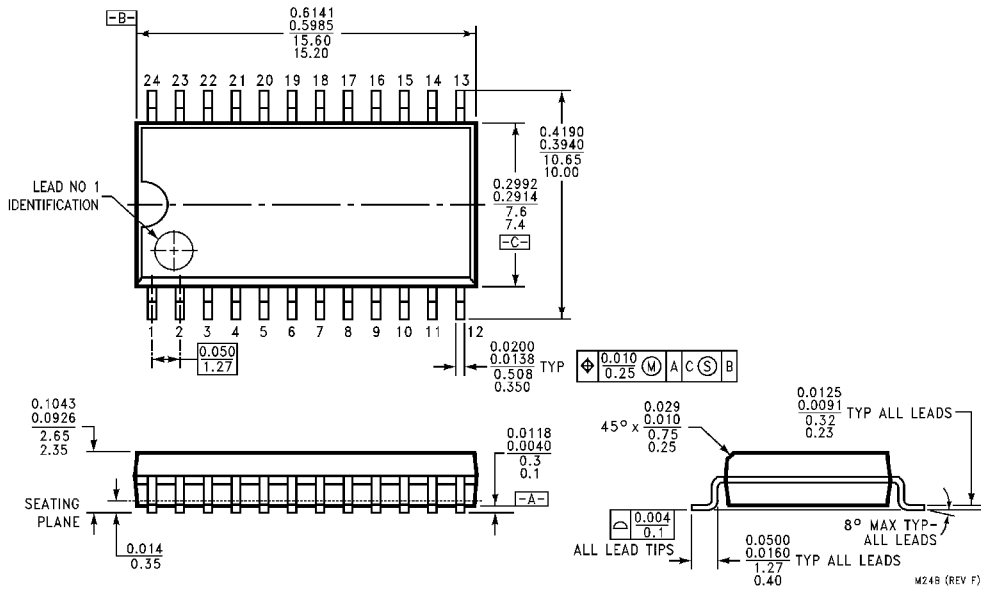
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



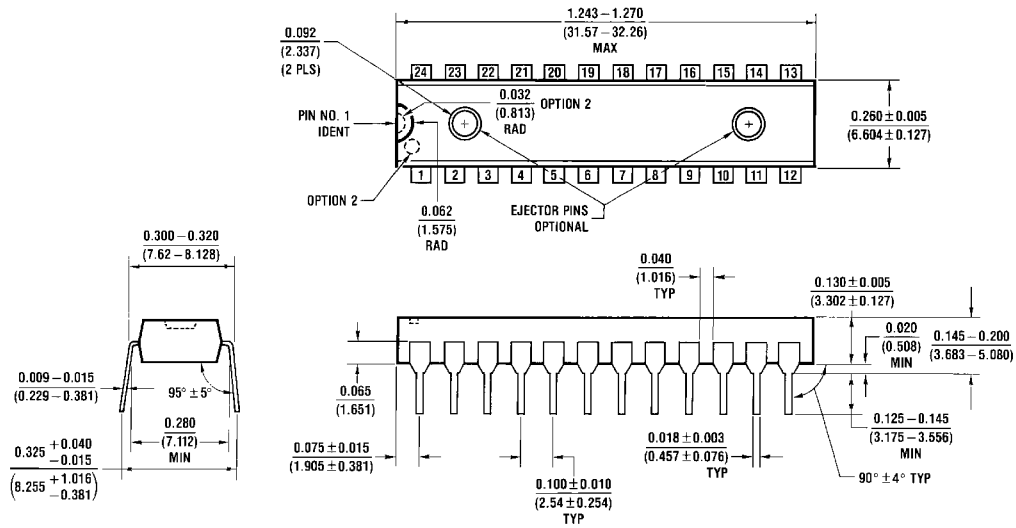
J24F (REV. H)

**24 Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
Package Number J24F**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

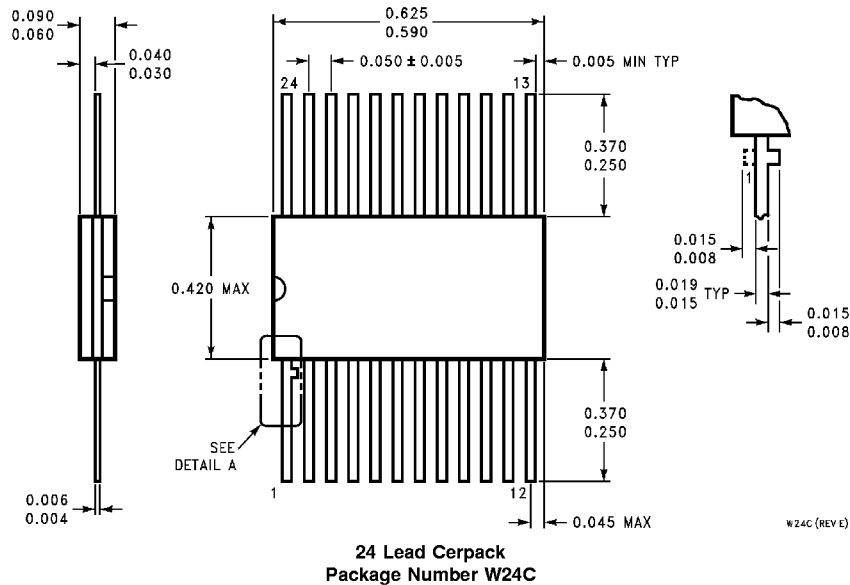


**24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M24B**



**24 Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
Package Number N24C**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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