ULN2803C Darlington Transistor Array

1 Features

- 500-mA-rated collector current (single output)
- High-voltage outputs: 50 V
- Output clamp diodes
- Inputs compatible with various types of logic

2 Applications

- Factory automation and control
- Building automation
- Appliances
- IP network camera
- HVAC valve & actuator control
- Relay, solenoid, and lamp driving
- Stepper motor driving

3 Description

The ULN2803C device is a 50-V, 500-mA Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairscan be connected in parallel for higher current capability.

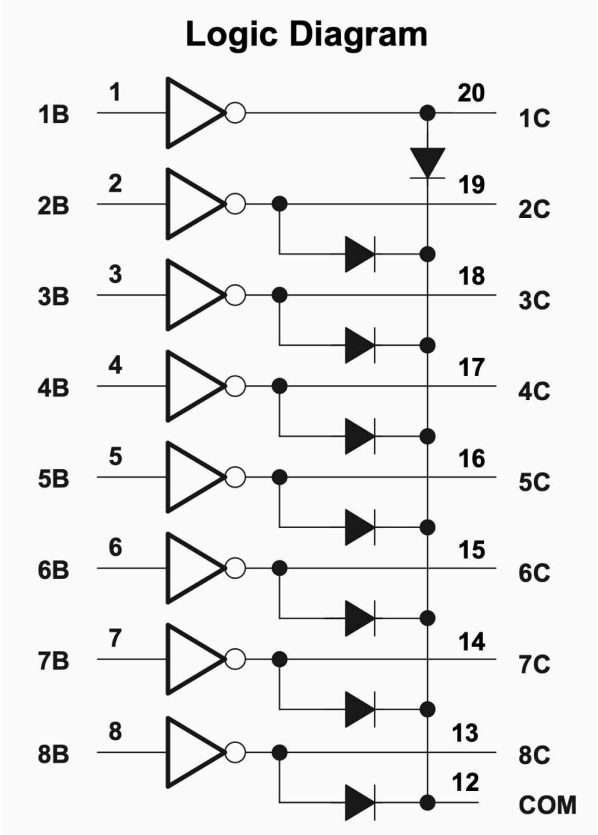
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803C device has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULN2803CDW	DW (SOIC, 20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2022	*	Initial release.

5 Pin Configuration and Functions

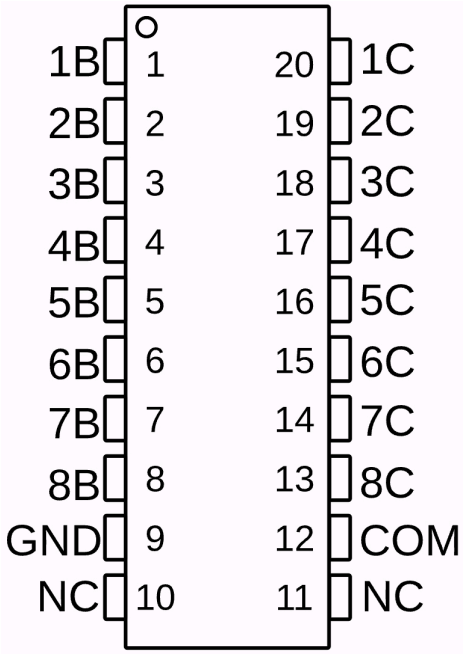


Figure 5-1. DW Package 20-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 8 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
8B	8		
1C	20	O	Channel 1 through 8 Darlington collector output
2C	19		
3C	18		
4C	17		
5C	16		
6C	15		
7C	14		
8C	13		
GND	9	—	Common emitter shared by all channels (typically tied to ground)
COM	12	I/O	Common cathode node for flyback diodes (required for inductive loads)
NC	10, 11	—	No connect pin

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage		50	V
V_I	Input voltage(2)		30	V
	Peak collector current		500	mA
I(clamp)	Output clamp current		500	mA
	Total substrate-terminal current		–2.5	A
T_J	Junction temperature	–65	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute MaximumRatings do not imply functional operation of the device at these or any other conditions beyond those listedunder Recommended Operating Conditions. If used outside the Recommended Operating Conditions but withinthe Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,functionality, performance, and shorten the device lifetime.
(2) All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage	0	50	V
T_A	Ambient temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		ULN2803C DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ULN2803C			UNIT
				MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, see Figure 7-1	I_I = 0			50	µA
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA, see Figure 7-2	50	65		µA
$I_{I(on)}$	Input current	V_I = 3.85 V,	See Figure 7-3		0.93	1.35	mA
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see Figure 7-4	I_C = 200 mA			2.4	V
			I_C = 250 mA			2.7	
			I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, see Figure 7-5	I_C = 100 mA		0.9	1.1	V
		I_I = 350 µA, see Figure 7-5	I_C = 200 mA		1	1.3	
		I_I = 500 µA, see Figure 7-5	I_C = 350 mA		1.3	1.6	
I_R	Clamp diode reverse current	V_R = 50 V,	see Figure 7-6			50	µA
V_F	Clamp diode forward voltage	I_F = 350 mA	see Figure 7-7		1.7	2	V
C_i	Input capacitance	V_I = 0,	f = 1 MHz		15	25	pF

6.6 Switching Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω, See Figure 7-8		130		ns
t_{PHL}	Propagation delay time, high- to low-level output			20		
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, see Figure 7-9	V_S – 20			mV

6.7 Typical Characteristics

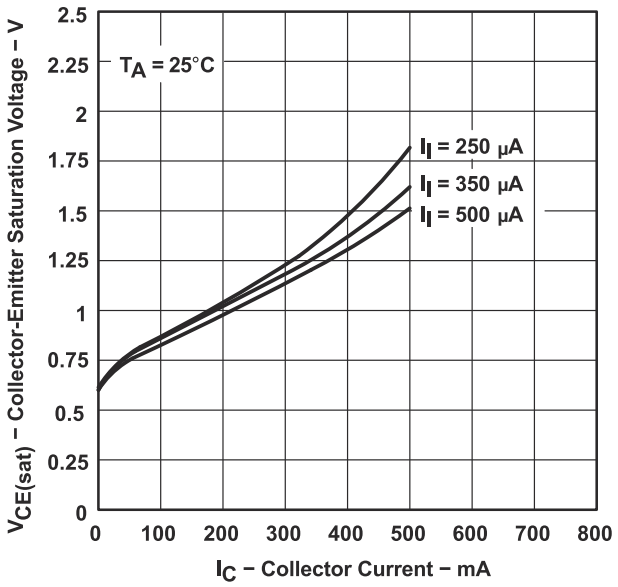


Figure 6-1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

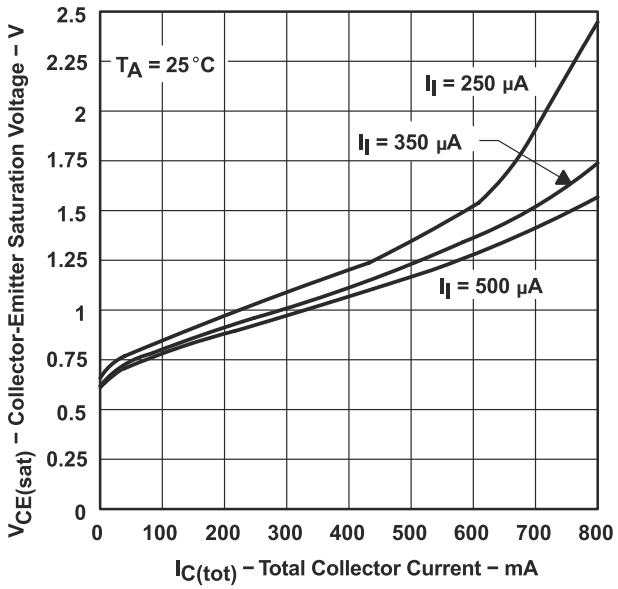


Figure 6-2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

7 Parameter Measurement Information

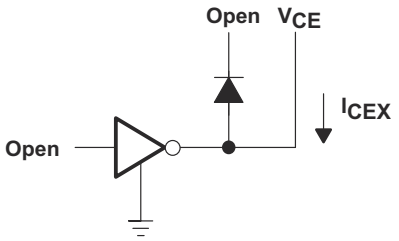


Figure 7-1. I_{CEX} Test Circuit

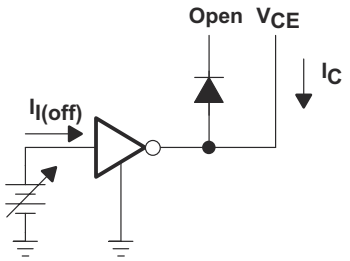


Figure 7-2. $I_{I(off)}$ Test Circuit

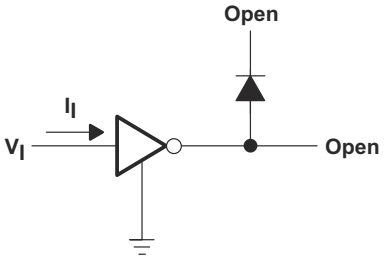


Figure 7-3. $I_{I(on)}$ Test Circuit

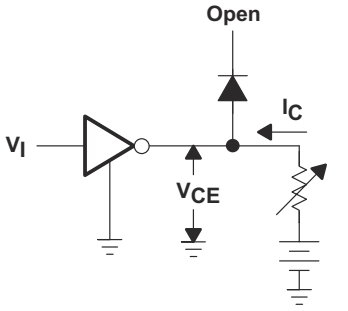


Figure 7-4. $V_{I(on)}$ Test Circuit

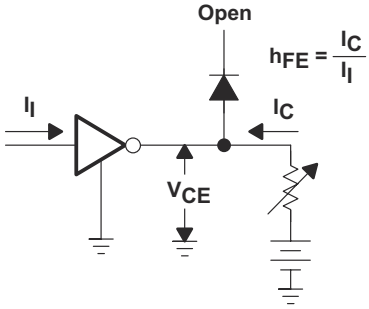


Figure 7-5. h_{FE}, $V_{CE(sat)}$ Test Circuit

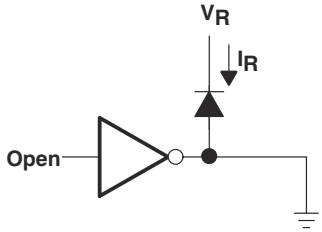


Figure 7-6. I_R Test Circuit

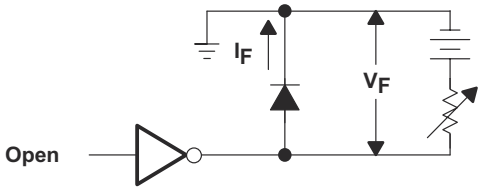
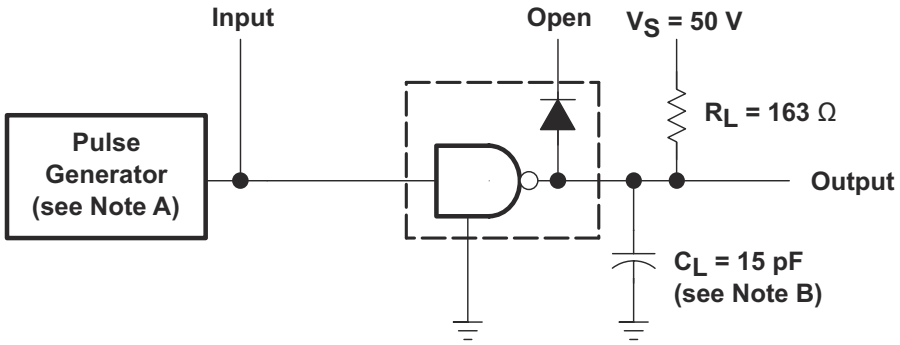
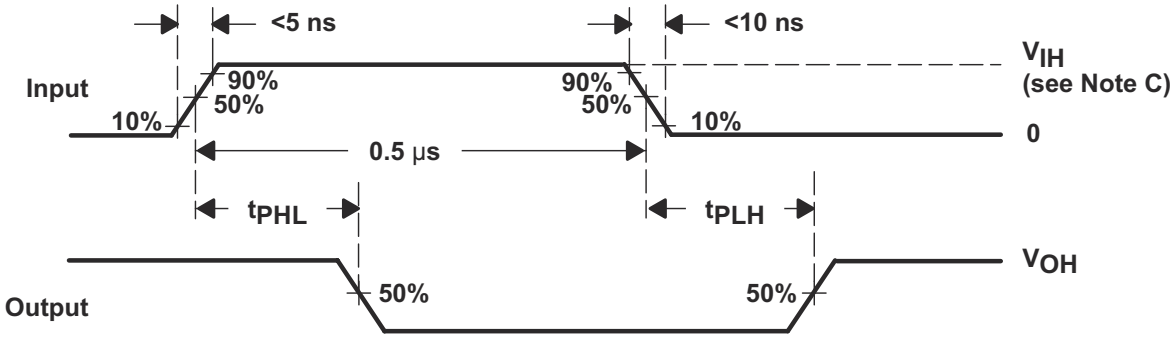


Figure 7-7. V_F Test Circuit



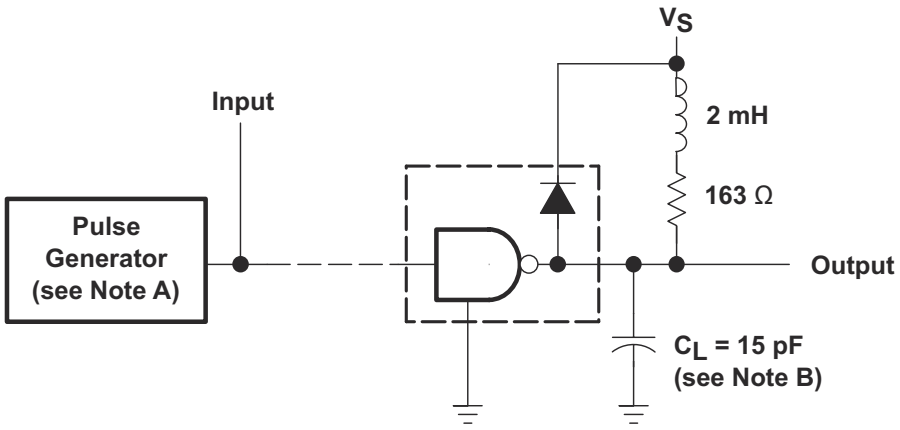
Test Circuit



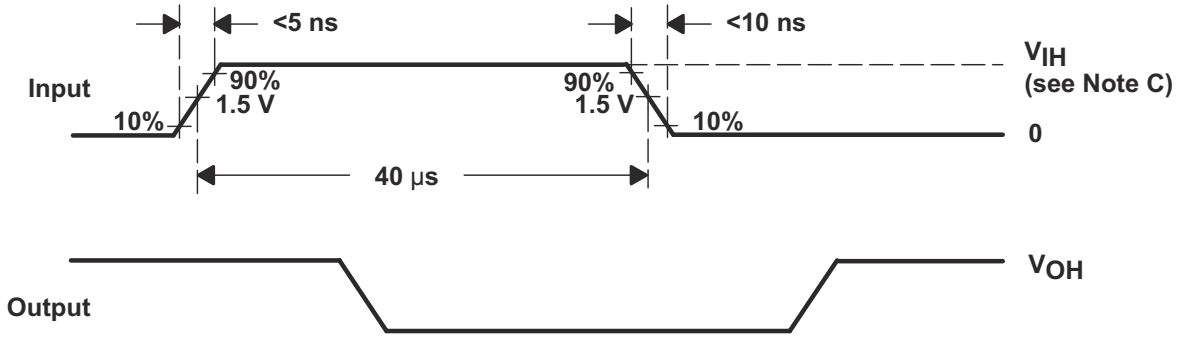
Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 7-8. Propagation Delay Times



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 7-9. Latch-Up Test

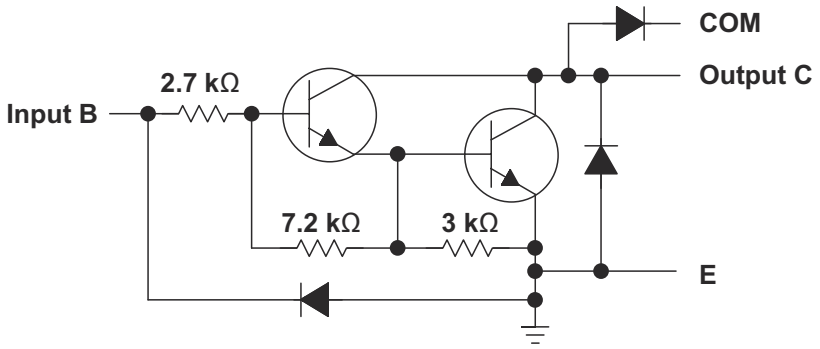
8 Detailed Description

8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This feature is due to its integration of eight Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803C is comprised of eight high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803C has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2803C offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output can be accommodated by paralleling the outputs.

8.2 Functional Block Diagram



8.3 Feature Description

Each channel of ULN2803C consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very-high current gain. The very high β allows for high output current drive with a very-low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN.

The diodes connected between the output and COM pin are used to suppress the kickback voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kickback diode.

In normal operation, the diodes on base and collector pins to emitter are reverse biased. If these diodes are forward biased, internal parasitic NPN transistors draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803C can drive inductive loads and suppress the kickback voltage through the internal free wheeling diodes.

8.4.2 Resistive Load Drive

When driving resistive loads, COM can be left unconnected or connected to the load voltage supply. If multiple supplies are used, connect to the highest voltage supply.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

ULN2803C is typically used to drive a high-voltage or current peripherals from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803C, driving inductive loads. This includes motors, solenoids, and relays. Each load type can be modeled by what is seen in Figure 9-1.

9.2 Typical Application

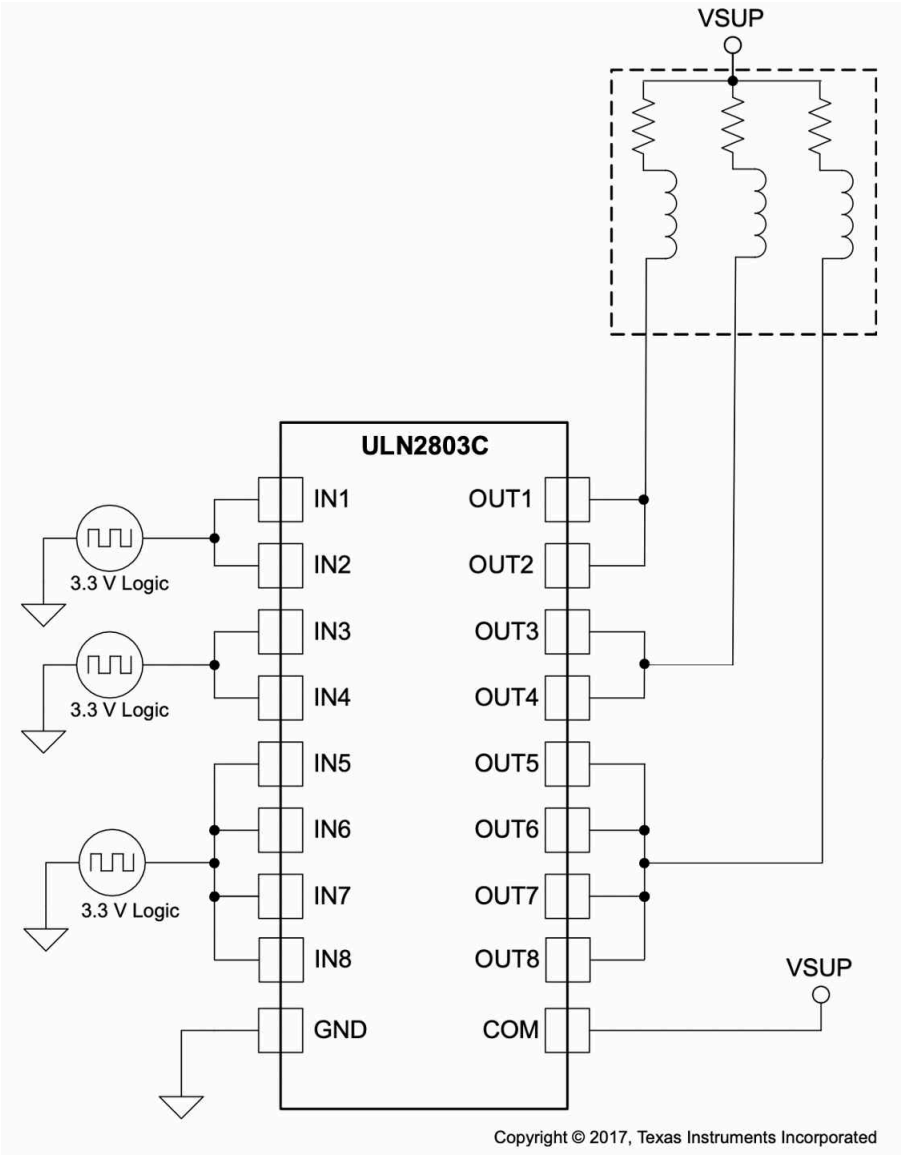


Figure 9-1. ULN2803C as Inductive Load Driver

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 or 5 V
Coil supply voltage	12 to 50 V
Number of channels	8
Output current (R_{COIL})	20 to 300 mA per channel
Duty cycle	100%

9.2.2 Detailed Design Procedure

When using ULN2803C in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

9.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance, and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

9.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by Figure 6-1, Figure 6-2, or *Electrical Characteristics*.

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use Equation 2 to calculate ULN2803C on-chip power dissipation P_D.

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (2)$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$.

To ensure the reliability of ULN2803C and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (P_D) dictated by Equation 3.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \quad (3)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance.

TI recommends to limit the ULN2803C IC die junction temperature to < 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curves

The following curves are generated with ULN2803C driving an OMRON G5NB relay – V_{in} = 5.0 V; V_{sup}= 12 V and R_{COIL}= 2.8 kΩ.

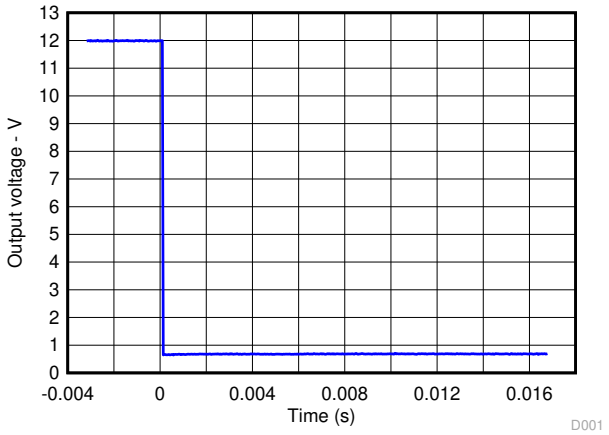


Figure 9-2. Output Response with Activation of Coil (Turn-On)

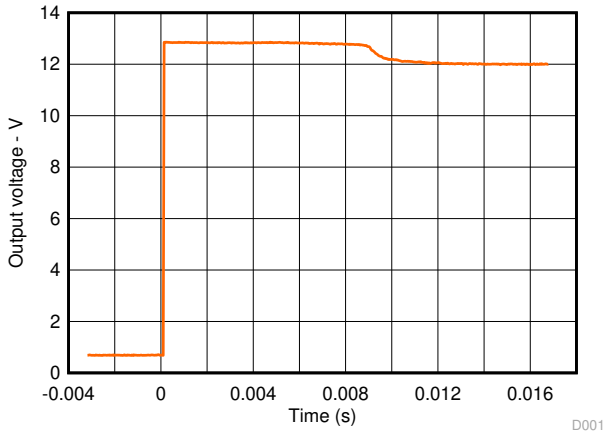


Figure 9-3. Output Response with De-activation of Coil (Turn Off)

9.3 Power Supply Recommendations

This devicedoes not need a power supply; however, the COM pin is typically tied to the system power supply. With this case, make sure that the output voltage does not heavily exceed the COM pin voltage. This action can heavily forward bias the flyback diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or overheating the part.

9.4 Layout

9.4.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803C. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive high currents as desired. Wire thickness can be determined by the trace material current density and desired drive current.

Because all of the channels currents return to a common emitter, size that trace width to be very wide. Some applications require up to 2.5 A.

9.4.2 Layout Example

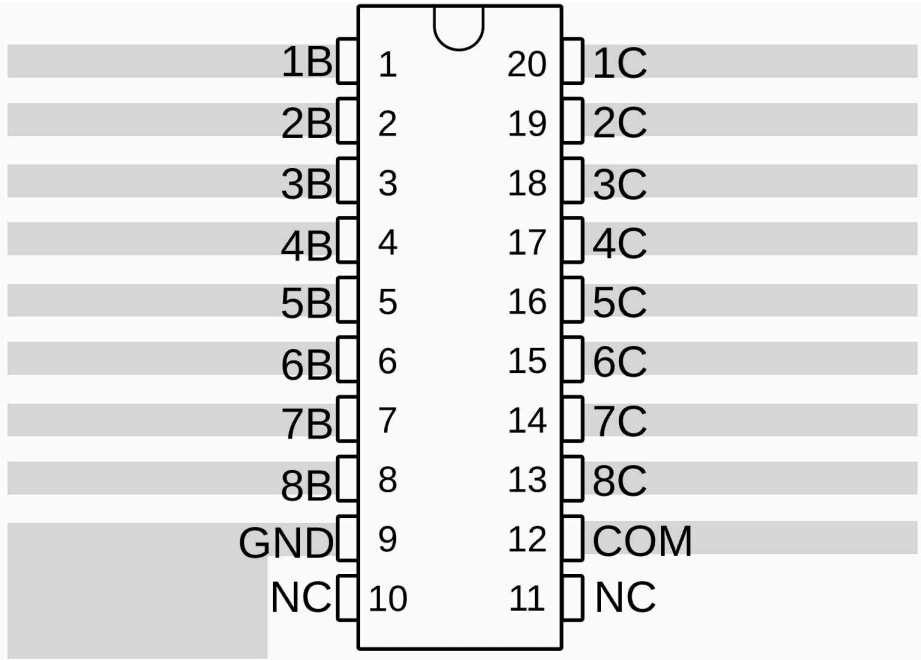


Figure 9-4. ULN2803C Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2803CDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ULN2803C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

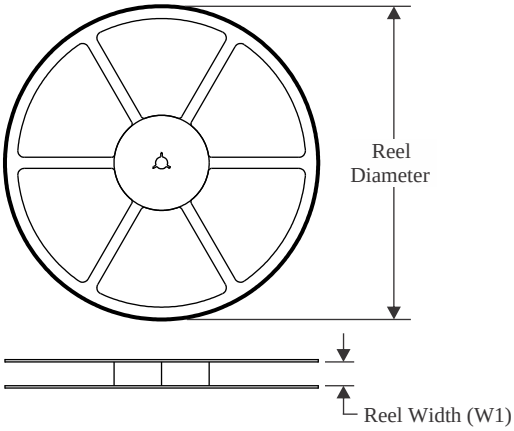
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

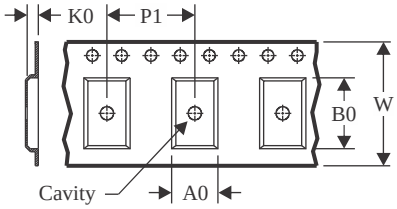
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

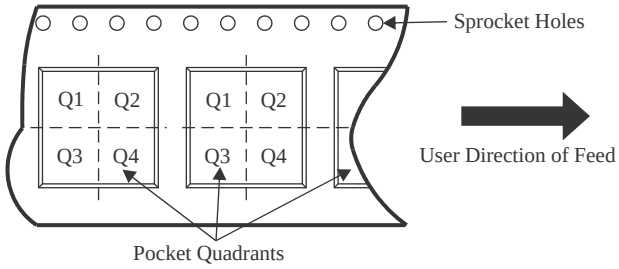


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

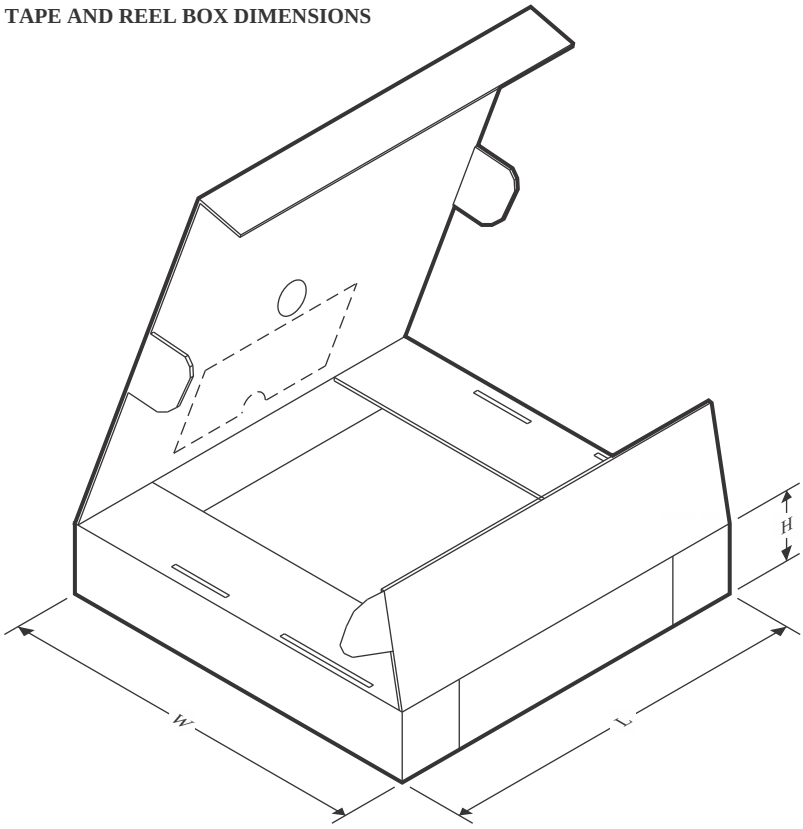
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

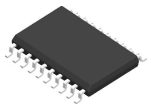
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803CDWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2803CDWR	SOIC	DW	20	2000	356.0	356.0	41.0

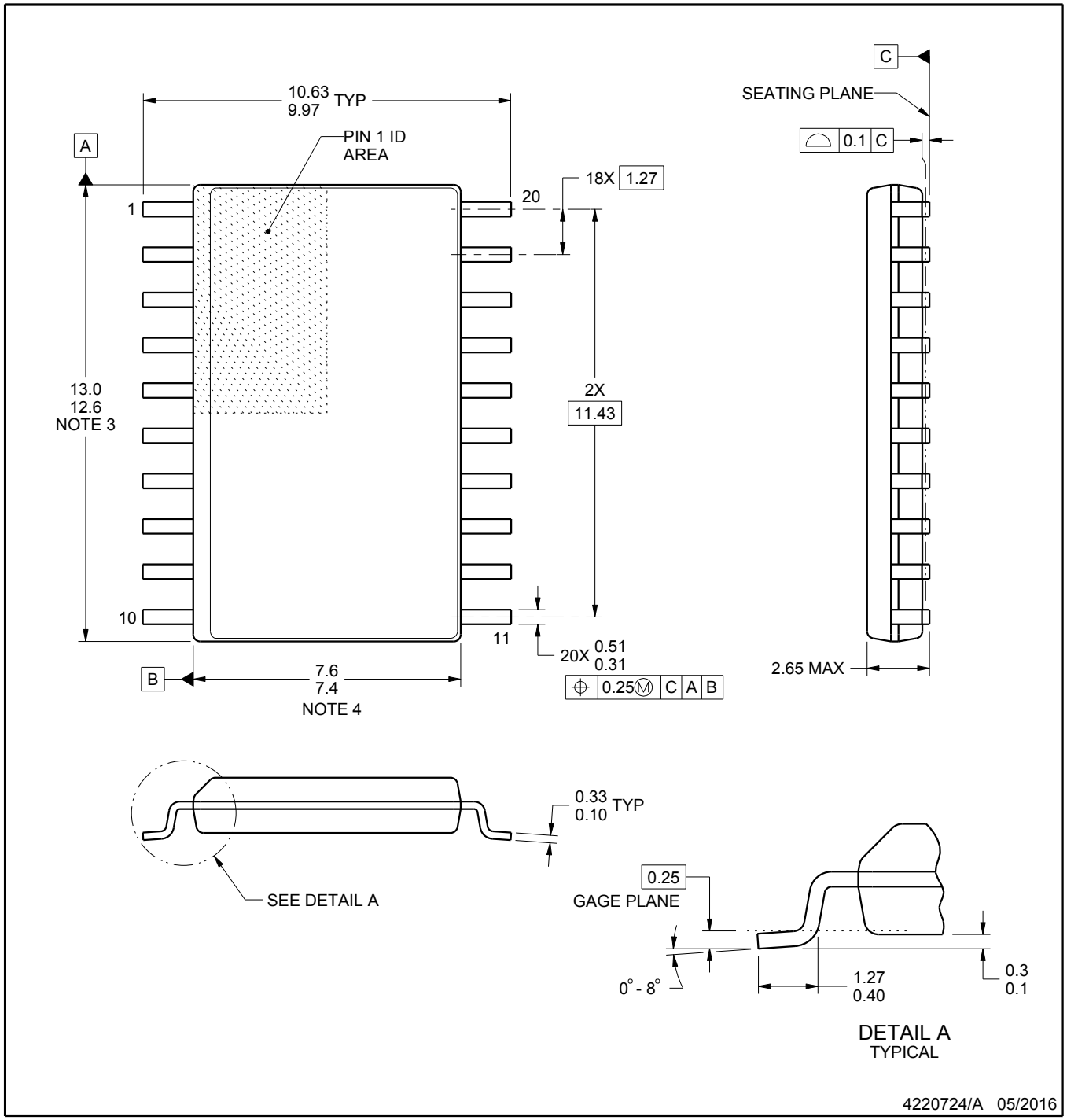


PACKAGE OUTLINE

DW0020A

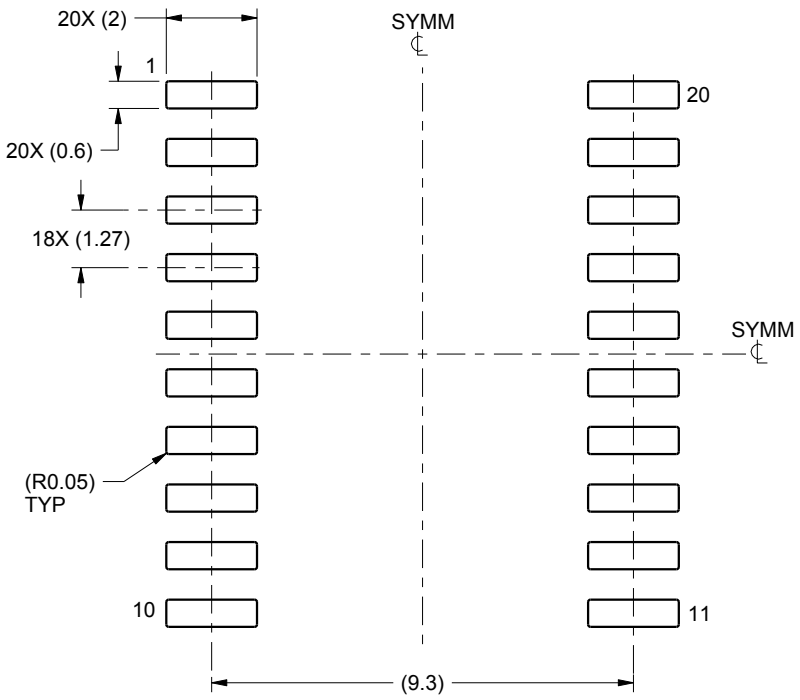
SOIC - 2.65 mm max height

SOIC

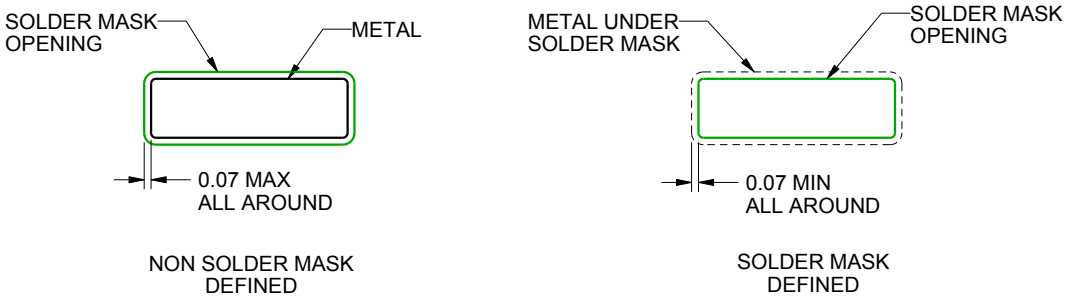


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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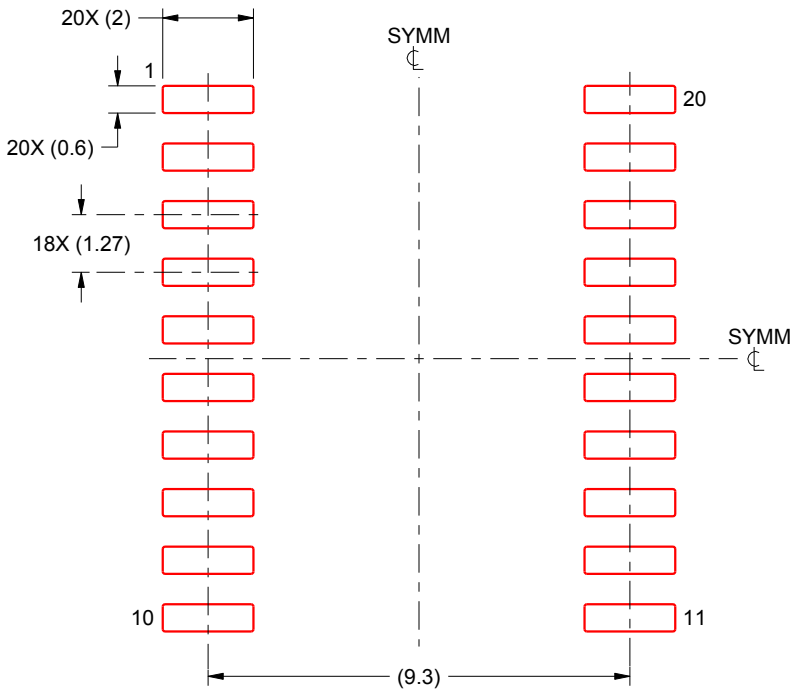
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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