



SAMSUNG
ARTIK[™] Modules

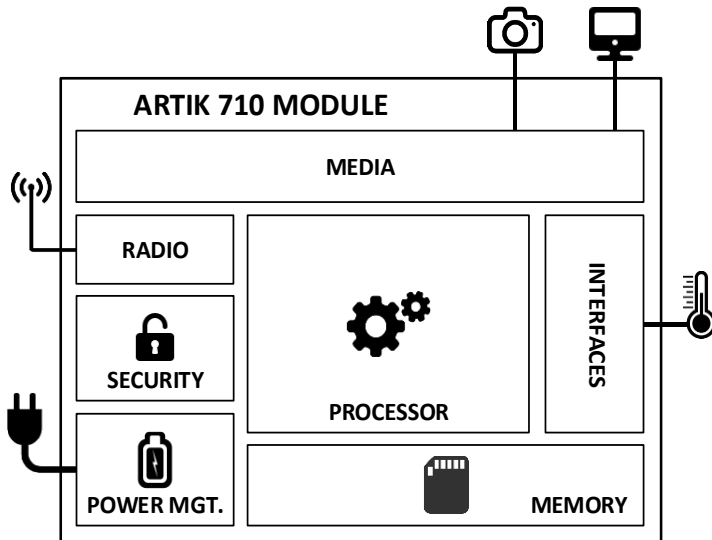
7

710 Datasheet



ARTIK 710 Module Top View

Samsung’s ARTIK™ 710 Module is a highly-integrated System-in-Module that utilizes an octa-core ARM® Cortex®-A53 processor packaged DRAM and Flash memory, a hardware Secure Element and a wide range of wireless communication options such as 802.11a/b/g/n/ac, Bluetooth® 4.1 (Classic+BLE), and 802.15.4 (ZigBee® or Thread) communications all into an extremely compact footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module’s capabilities. With the combination of Wi-Fi, Bluetooth, ZigBee/Thread, the ARTIK 710 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability with the camera and display support options. The hardware based Secure Element works with the ARM® TrustZone® and Trustware’s Trusted Execution Environment (TEE) to provide enhanced end-to-end security.



ARTIK 710 Module Block Diagram

| Processor | |
|-------------------------------|--|
| CPU | 8x ARM® Cortex®-A53@1.4GHz |
| GPU | 3D graphics accelerator |
| Media | |
| Camera I/F | 4-Lane MIPI CSI |
| Display | 4-Lane MIPI DSI up to FHD@24bpp |
| Audio | I ² S audio interface |
| Memory | |
| DRAM | 1GB DDR3 @ 800MHz |
| FLASH | 4GB eMMC |
| Security | |
| Secure Element | Secure point to point authentication and data transfer |
| Trusted Execution Environment | Trustware |
| Radio | |
| WLAN | IEEE 802.11a/b/g/n/ac |
| Bluetooth | 4.1 (Classic+BLE) |
| 802.15.4 | ZigBee/Thread |
| Power Management | |
| PMIC | Provides all power of the ARTIK 710 Module using on board bucks and LDOs |
| Interfaces | |
| Analog and Digital I/O | GPIO, I ² C, SPI, UART, SDIO, USB 2.0, JTAG, Analog Input |

SAMSUNG ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE. Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind. This document and all information discussed herein remain the sole and exclusive property of Samsung Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or other-wise. Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply. For updates or additional information about Samsung products, contact your nearest Samsung office. All brand names, trademarks and registered trademarks belong to their respective owners.

TABLE OF CONTENTS

| | |
|--|----|
| Table of Contents | 3 |
| List of Figures | 5 |
| List of Tables | 5 |
| <i>Version History</i> | 7 |
| ARTIK 710 Module Block Diagram and Component Placement | 8 |
| <i>ARTIK 710 Module ZigBee or Thread</i> | 10 |
| <i>ARTIK 710 Module 802.15.4 Front End</i> | 10 |
| <i>ARTIK 710 Module Memory</i> | 10 |
| <i>ARTIK 710 Module PMIC</i> | 10 |
| <i>ARTIK 710 Module Wi-Fi/Bluetooth</i> | 11 |
| <i>ARTIK 710 Module Secure Element</i> | 11 |
| <i>ARTIK 710 Module Secure JTAG</i> | 12 |
| <i>ARTIK 710 Module Processor System</i> | 12 |
| ARTIK 710 Module PADS | 21 |
| ARTIK 710 Module Functional Interfaces | 29 |
| ADC | 29 |
| Booting | 29 |
| Bluetooth PCM | 29 |
| MIPI CSI | 29 |
| MIPI DSI | 30 |
| GMAC | 30 |
| GPIO | 30 |
| HDMI | 31 |
| HSIC | 31 |
| I ² C | 31 |
| I ² S | 32 |
| JTAG | 32 |
| Key | 32 |
| LVDS | 32 |
| Miscellaneous | 33 |
| Power | 33 |
| PWM | 34 |
| SD/MMC | 34 |
| SPI | 34 |
| UART | 35 |
| USB HOST/USB OTG | 35 |
| ZIGBEE | 35 |
| ARTIK 710 Module GPIO Alternate Functions | 36 |
| ARTIK 710 Module Booting Sequence | 40 |
| ARTIK 710 Module Power States | 41 |
| ARTIK 710 Module Antenna Connections | 42 |
| ARTIK 710 Module Electrical Specifications | 43 |
| <i>Absolute Maximum Ratings</i> | 43 |
| <i>Recommended Operating Conditions</i> | 43 |
| <i>DC Module Use Case Characteristics</i> | 44 |
| <i>Power Supply Requirements</i> | 44 |
| <i>ESD Ratings</i> | 49 |
| <i>DC Electrical Characteristics</i> | 50 |
| <i>AC Electrical Characteristics</i> | 52 |
| <i>RF Electrical Characteristics</i> | 57 |
| ARTIK 710 Module Mechanical Specifications | 64 |

Ordering Information 66
Legal Information 67

LIST OF FIGURES

| | |
|---|----|
| Figure 1. ARTIK 710 Module Functional Block Diagram | 8 |
| Figure 2. ARTIK 710 Module Component Placement - Top View | 9 |
| Figure 3. Front and Back of the certified ARTIK 710 Module | 9 |
| Figure 4. Processor System Block Schematic | 13 |
| Figure 5. ARTIK 710 Module Top View BALL Organization | 21 |
| Figure 6. ARTIK 710 Module Power Management State Diagram | 41 |
| Figure 7. RF Connector for BT/Wi-Fi and ZigBee/Thread | 42 |
| Figure 8. ARTIK 710 Module Power Distribution | 44 |
| Figure 9. High Speed SDMMC Interface Timing | 52 |
| Figure 10. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A)) | 53 |
| Figure 11. I ² C Interface Timing | 56 |
| Figure 12. ARTIK 710 Module Mechanical Dimensions | 64 |
| Figure 13. Mechanical Bottom View and Top View | 64 |
| Figure 14. L-Shaped PAD Pins | 65 |

LIST OF TABLES

| | |
|----------------------------------|----|
| Table 1. TOP BALL ARRAY | 22 |
| Table 2. BOTTOM BALL ARRAY | 24 |
| Table 3. LEFT BALL ARRAY | 26 |
| Table 4. RIGHT BALL ARRAY | 27 |
| Table 5. ADC | 29 |
| Table 6. Booting | 29 |
| Table 7. Bluetooth PCM | 29 |
| Table 8. MIPI CSI | 29 |
| Table 9. MIPI DSI | 30 |
| Table 10. GMAC | 30 |
| Table 11. GPIO | 30 |
| Table 12. HDMI | 31 |
| Table 13. HSIC | 31 |
| Table 14. I ² C | 31 |
| Table 15. I ² S | 32 |
| Table 16. JTAG | 32 |
| Table 17. Key | 32 |
| Table 18. LVDS | 32 |
| Table 19. Miscellaneous | 33 |
| Table 20. Power | 33 |
| Table 21. PWM | 34 |
| Table 22. SD/MMC | 34 |
| Table 23. SPI | 34 |

| | |
|---|----|
| Table 24. UART..... | 35 |
| Table 25. USB Host/USB OTG | 35 |
| Table 26. ZigBee | 35 |
| Table 27. GPIO Alternate Functions TOP PART | 36 |
| Table 28. GPIO Alternate Functions BOTTOM PART | 37 |
| Table 29. GPIO Alternate Functions LEFT PART | 39 |
| Table 30. GPIO Alternate Functions RIGHT PART | 39 |
| Table 31. Booting Scenarios | 40 |
| Table 32. Booting Options..... | 40 |
| Table 33. Absolute Maximum Ratings..... | 43 |
| Table 34. Recommended Operating Conditions..... | 43 |
| Table 35. DC-DC Converter Description | 44 |
| Table 36. PMIC LDOs..... | 45 |
| Table 37. AC/DC Characteristics LDO1, LDO2, LDO4..... | 46 |
| Table 38. AC/DC Characteristics LDO1, LDO2, LDO4 Eco Mode | 46 |
| Table 39. AC/DC Characteristics LDO5 | 47 |
| Table 40. AC/DC Characteristics LDO5 Eco Mode | 47 |
| Table 41. AC/DC Characteristics LDO7, LDO8, LDO9, LDO10..... | 48 |
| Table 42. ESD Ratings | 49 |
| Table 43. Shock and Vibration Ratings | 49 |
| Table 44. I/O DC Electrical Characteristics GPIO | 50 |
| Table 45. I/O DC Electrical Characteristics GPIO | 50 |
| Table 46. I/O DC Electrical Characteristics PMIC | 51 |
| Table 47. I/O DC Electrical Characteristics GPIO | 51 |
| Table 48. GPIO Pull-up Resistor Current | 51 |
| Table 49. Power on Reset Timing Specifications..... | 51 |
| Table 50. High Speed SDMMC Interface Transmit/Receive Timing Constants | 52 |
| Table 51. SPI Interface Transmit/ Receive Timing Constants with 15pF Load | 54 |
| Table 52. SPI Interface Transmit/ Receive Timing Constants with 30pF Load | 55 |
| Table 53. I ² C BUS Controller Module Signal Timing..... | 56 |
| Table 54. Wi-Fi WLAN 2.4GHz Receiver RF Specifications | 57 |
| Table 55. Wi-Fi WLAN 2.4GHz Transmitter RF Specifications | 58 |
| Table 56. Wi-Fi WLAN 5GHz Receiver RF Specifications | 58 |
| Table 57. Wi-Fi WLAN 5GHz Transmitter RF Specifications | 60 |
| Table 58. Bluetooth Receiver RF Specifications | 61 |
| Table 59. Bluetooth Transmitter RF Specifications..... | 61 |
| Table 60. BLE RF Specifications | 61 |
| Table 61. 802.15.4 RF Receive Specifications | 62 |
| Table 62. ZigBee/Thread RF Transmit Specifications | 63 |
| Table 63. ZigBee/Thread RF Receive Specifications..... | 63 |
| Table 64. L-Shaped Ball Locations | 65 |

ARTIK 710 MODULE BLOCK DIAGRAM AND COMPONENT PLACEMENT

Figure 1 shows the functional block diagram of the ARTIK 710 Module. It consists of an octa-core ARM® Cortex®-A53 application processor with 1GB of DDR3 and 4GB eMMC Flash, PMIC power management SoC, Secure Element, Wi-Fi/BT chipset, ZigBee/Thread chipset and RF connectors.

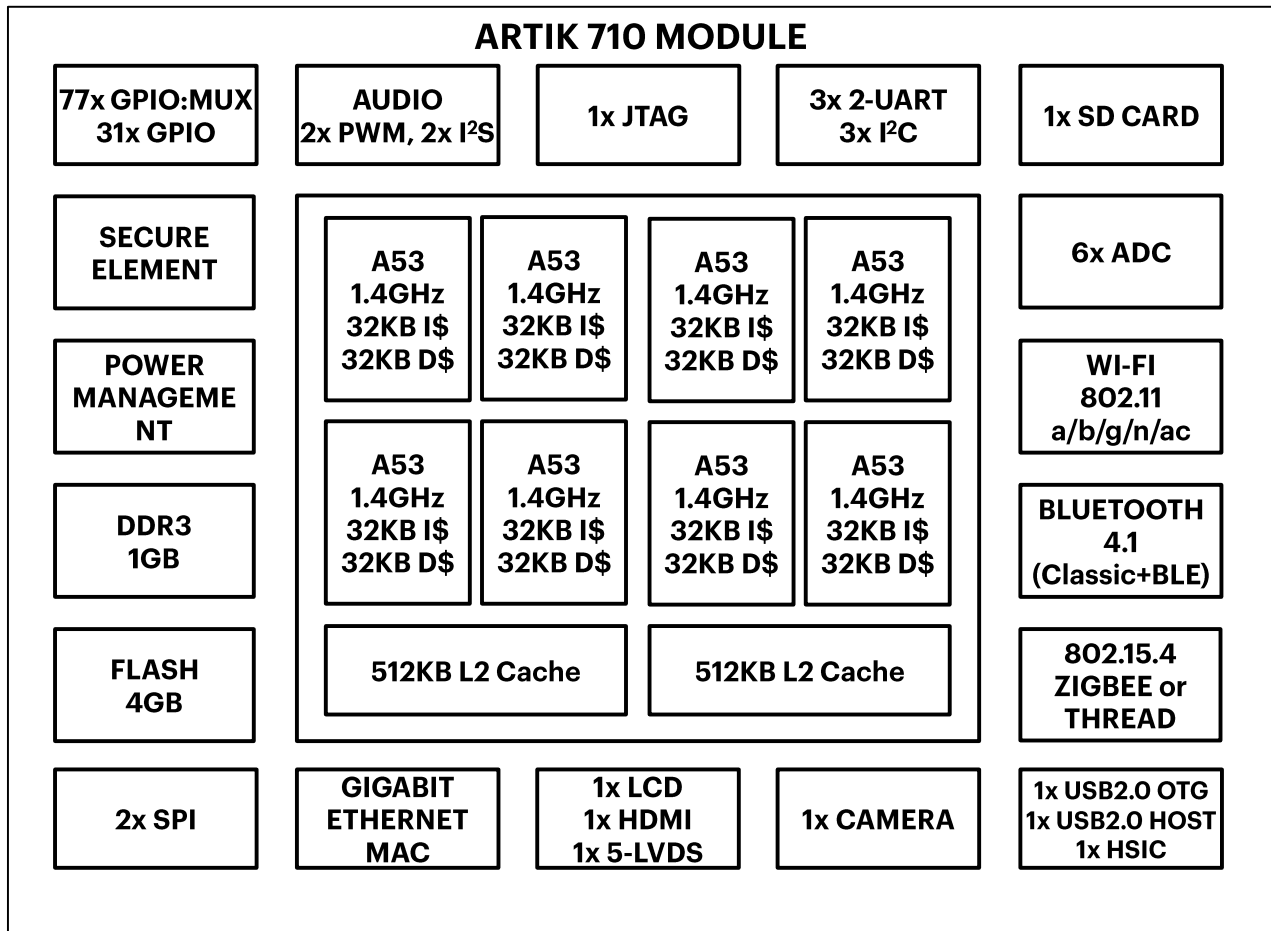


Figure 1. ARTIK 710 Module Functional Block Diagram

Figure 2 shows the Top View with component placement of the ARTIK 710 Module. The top side of the ARTIK 710 Module is populated with the octa-core ARM® A53 application processor, 2x 512MB of DDR3 memory chips, PMIC power manager, Wi-Fi/BT combo chipset, 4GB of Flash, 802.15.4 chipset to support ZigBee or Thread, PA and RF connectors for Wi-Fi/BT and 802.15.4 antennas. In addition Figure 3 shows the front and back of the certified ARTIK 710 Module.

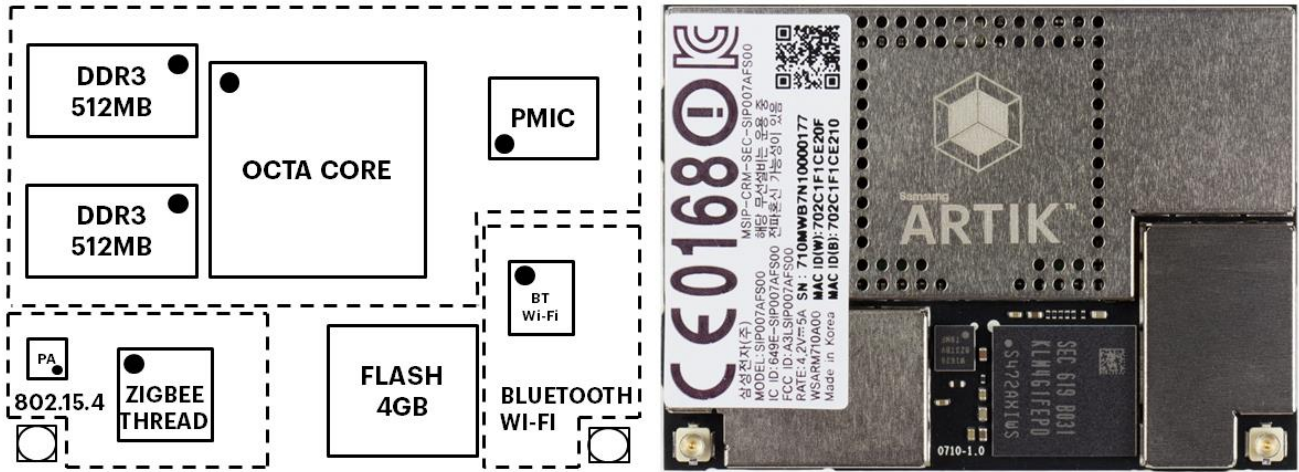


Figure 2. ARTIK 710 Module Component Placement - Top View

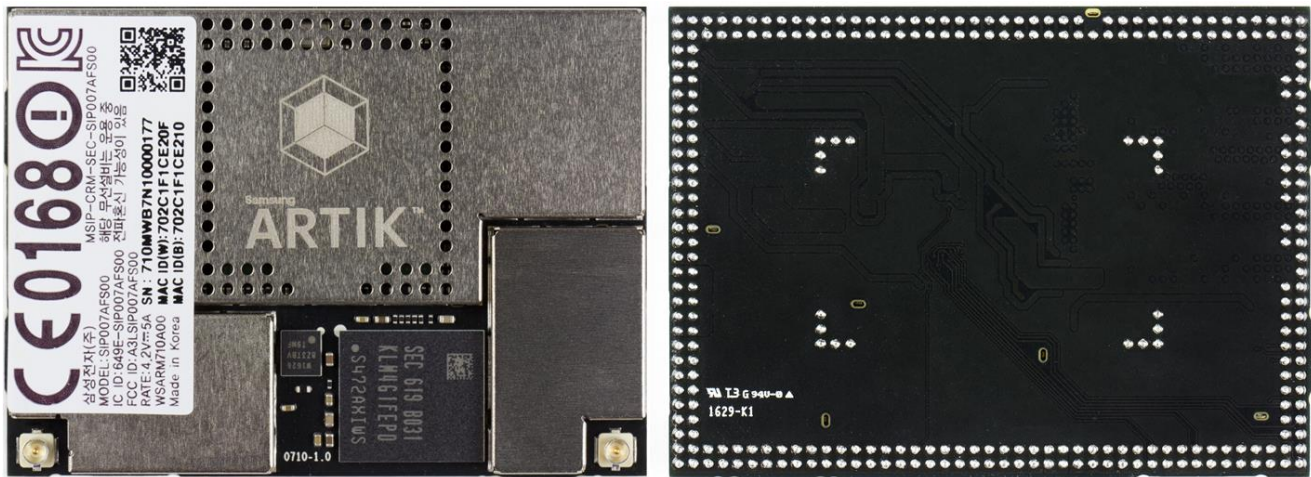


Figure 3. Front and Back of the certified ARTIK 710 Module

ARTIK 710 MODULE ZIGBEE OR THREAD

The ARTIK 710 Module carries a fully-integrated 802.15.4 device. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM[®] Cortex[®]-M3 microprocessor, flash and RAM memory and peripherals. The most important hardware features of the ZigBee or Thread module are:

- Complete system-on-chip using 32-bit ARM[®] Cortex[®]-M3 processor.
- Single-voltage operation

ARTIK 710 MODULE 802.15.4 FRONT END

The ARTIK 710 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for low power sensitive IoT environments. The most important hardware features of the front-end are:

- Combined Tx/Rx transceiver port and single antenna port
- 2.4GHz high power amplifier with low pass harmonic filter
- Low noise amplifier
- Transmit/Receive switch
- Integrated power detector monitoring and controlling transmit power
- CMOS control logic
- 50Ω input output matching

ARTIK 710 MODULE MEMORY

The ARTIK 710 Module has 2x 512MB DDR3 memory chips running at 800MHz each. In addition the ARTIK 710 module has 1x 4GB eMMC Flash memory chip based on the JEDEC MMC 4.51/5.0 standard. The interface speed varies from 200MB/s using MMC4.51 to 400MB/s when using the MMC5.0 standard.

ARTIK 710 MODULE PMIC

The ARTIK 710 Module has a fully-integrated PMIC containing 5 High efficiency DC-DC converters and 10 LDOs. This unit provides all power requirements for the ARTIK 710 Module in one compact form factor. In addition, various stable power outputs are offered at the connectors, such that additional customer-defined use cases can be defined and efficiently implemented.

ARTIK 710 MODULE WI-FI/BLUETOOTH

The ARTIK 710 Module has a fully-integrated IEEE 802.11 a/b/g/n/ac MAC baseband radio, Bluetooth 4.1 and an FM receiver. The most important hardware features of the Wireless LAN/Bluetooth combo SoC are:

- IEEE802.11 Features
 - WLAN 802.11 ac compliant:
 - Single-stream spatial multiplexing up to 433Mbps
 - Support for 20, 40 and 80 MHz channels including 256 QAM
 - Supports explicit 802.11ac transmit beamforming
 - On chip PA for both bands
- Bluetooth Features
 - Support v4.1 with provisions to support future specifications
 - Bluetooth Class 1 or Class 2 transmitter operation
 - Support for Adaptive Frequency Hopping (reduce interference)
 - Using a 4-wire UART interface

ARTIK 710 MODULE SECURE ELEMENT

The ARTIK 710 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The Secure Element provides an ISO/IEC 7816 14443 compliant interface. The most important hardware features of the Secure Element are:

- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
 - Modular exponential accelerator
 - RSA 2080bits
 - ECC 512 bits
- Data security
 - Memory encryption for all memory
 - 256B read only and 256B non erasable flash area
 - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
 - 32KB ROM
 - 264KB FLASH
 - 8.5KB Static RAM including 2.5KB crypto memory
- Serial interfaces:
 - ISO 7816-3 compliant interface
 - Asynchronous half-duplex character receive/transmit serial interface

ARTIK 710 MODULE SECURE JTAG

Our secure JTAG core that is part of the ARTIK 710 Module provides debug capabilities for the developer. The secure JTAG core has an authentication, authorization and an access provider module to assure that only authorized developers have access to the hardware. The main features of the secure JTAG core are:

- Dedicated authentication process through password mechanism
- Dedicated Hash engine with hash sequencer
- Industry standard JTAG capabilities

ARTIK 710 MODULE PROCESSOR SYSTEM

The processor system architecture that resides on the ARTIK 710 Module is a system-on-a-chip (SoC) based on a dual 32/64-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using an octa-core CORTEX[®]-A53 CPU. The ARTIK 710 Module contains 3D graphics hardware, image signal-processor hardware and a variety of high-speed interfaces such as eMMC5.0.

The ARTIK 710 Module allows for heavy traffic operations with a bandwidth up to 7.4GB/s such as 1080p video encoding and decoding, 3D graphics display and high resolution image signal processing with full HD display.

The application processor supports dynamic virtual-address mapping aiding software engineers to fully utilize the memory resources. The ARTIK 710 Module provides 3D graphics performance with a wide range of APIs such as OpenGL[®] ES1.1 and 2.0. The key features of the ARTIK 710 Module are:

- Octa-core ARM[®] Cortex[®]-A53 with 32KB I\$/32KB D\$ per core and shared 2x 512KB (per 4x cores) L2 Cache
- Memory subsystem:
 - DDR3 up to 800MHz
 - MLC/SLC NAND Flash support with hardwired ECC
- Supports 2D and 3D graphics hardware with OpenGL ES 1.1 and 2.0 software API
- Supports dual display up to 1920x1080 with TFT-LCD, LVDS, HDMI 1.4a and MIPI-DSI output
- Supports 10/100/1000M Ethernet MAC
- Supports a wide variety of interfaces such as S/PDIF, SPI, I²S, I²C, UART, USB, GPIOs, GMAC, PWM
- Supports up to 6 channels of ADC
- Supports MPEG-TS HW Parser
- Supports 1x USB Host, 1x USB OTG and 1x HSIC Host
- Supports secure JTAG
- Supports ARM TrustZone Technology
- Supports a variety of Power Modes (Normal, Sleep, Stop Modes)
- Supports a variety of Booting Options

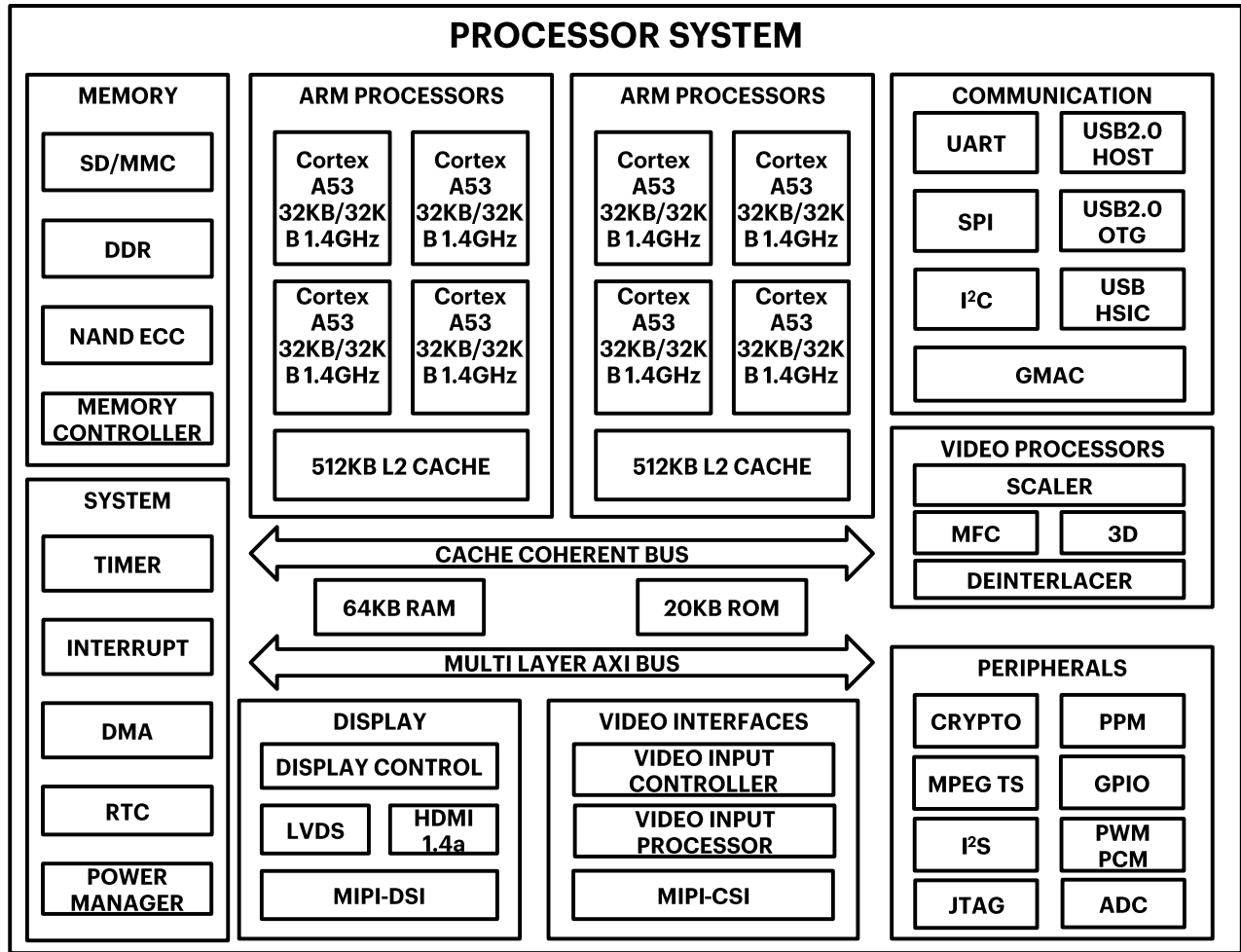


Figure 4. Processor System Block Schematic

SD/MMC

The ARTIK 710 Module provides 1x SD/MMC interface. The Mobile Storage Host is an interface between the system and SD/MMC card. The key features of mobile storage host sub-system are:

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support for Embedded Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support 8-bit DDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

MEMORY CONTROLLER

The most important features of the Memory module are:

- System Memory Controller
 - Support for 1GB DDR3 SDRAM
 - Maximum operating frequency of 800MHz
 - 32-bit data bus
- Static Memory Controller

- Multiplexed address up to 24-bit
- Support for SRAM, ROM and NAND flash
- Support for burst read/write
- NAND Flash Controller
 - Support for SLC/MLC Nand flash
 - ECC algorithm support

TIMER/WATCHDOG TIMER

The most important features of the Timer/Watchdog module are:

- 4x dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

INTERRUPT CONTROLLER

The most important features of the Interrupt Controller module are:

- Vectored Interrupt Controller
- Support for 4x interrupt types
 - 16x software generated interrupts
 - 6x External Private Peripheral Interrupt (PPI) per processor
 - 1x Internal PPI for each processor
 - 128x Shared peripheral interrupts
- For each interrupt source the following properties are available:
 - Fixed hardware interrupt priority level
 - Programmable interrupt priority level
 - Hardware interrupt priority level masking
 - IRQ and FIQ generation
 - Software interrupt generation
 - Test registers
 - Raw interrupt status
 - Interrupt request status

DMA

The most important features of the Scatter-Gather DMA module are:

- 16x channels of dedicated DMA
- 16x DMA request lines
- Various operating modes
 - Single DMA mode
 - Burst DMA mode
 - Memory 2 memory transfer
 - Memory to peripheral transfer
 - Peripheral to memory transfer
- Support for 8/16/32 bit wide transactions
- Big-Endian and Little-Endian (default) support

REAL TIME CLOCK (RTC) & POWER MANAGER

The most important features of the RTC and Power Manager module are:

- 4x spread spectrum PLLs
- 2x external crystals : 1x 24MHz crystal for PLL, 1x 32.768KHz crystal for RTC
- 32-bit RTC counter
- Support for alarm interrupt using RTC
- Support for various power modes
 - Normal, Idle, Stop, Sleep (Suspend to RAM)

ARM PROCESSORS

The most important features of the CPU module are:

- 8x Cortex A53 cores running at 1.4GHz
- Each core has 32KB of I-Cache (I\$) and 32KB of D-Cache (D\$)
- 2x 512KB of L2 Cache is shared between 2x4 cores
- Dedicated Vector Floating Point Processor (VFPP), Neon processor

LVDS

The ARTIK 710 Module provides 5x LVDS output channels with 1x clock channel. The key features of the LVDS channel system are:

- Output clock range 30-160MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

MIPI DSI

The ARTIK 710 Module provides 1x 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to WUXGA 1920x1200
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
 - 16bpp, 18bpp packed, 18bpp loosely-packed (3 byte), 24bpp
- Supported interfaces are:
 - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
 - RGB Interface for video image input from display controller
 - An I80 interface for Command Mode Image input from display controller
 - PMS control interface for PLL to configure byte clock frequency
 - Pre-scaler to generate escape clock from byte clock

HDMI CONTROLLER

The ARTIK 710 Module provides 1x HDMI v1.4a interface. The key features of the HDMI sub-system are:

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
 - 480p@59.94/60Hz
 - 576p@50Hz
 - 720p@50/59.94/60Hz
 - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color
- HDMI-CEC compliant
- Integrated HDCP 1.4 compliant

MIPI CSI

The ARTIK 710 Module provides 1x 4-lane MIPI interface that complies with the MIPI CSI standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are:

- Supports 1, 2, 3 or 4 data lanes
- Supported image formats are:
 - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
 - RGB565, RGB666, RGB888

- RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Compressed format : 10-6-10, 10-7-10, 10-8-10
- User defined Byte based data packet
- Compatible to PPI (Protocol to PHY interface)

VIDEO INPUT PROCESSOR

The ARTIK 710 Module provides 1x Video Input Processor (VIP). The key features of the VIP sub-system are:

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI CSI
- Support of images up to 8192x8192
- Support for clipping and scale-down
- Support for YUV420, YUV422 and YUV444 memory format and linear YUV422 memory format

UART

The ARTIK 710 Module provides 3x2-pin UART with just RxD and TxD signals. The key features of the UART sub-system are:

- Separate 32x8 Tx and 32x12 Rx FIFO memory buffers
- Support for DMA and interrupt based mode of operation
- All independent channels support IrDA 1.0
- Support for modem control functions CTS, DCD, DSR, RTS, DTR and RI
- Each UART channel contains:
 - Programmable baud-rates
 - 1 or 2 stop bit insertion
 - 5-bit, 6-bit, 7-bit, or 8-bit data width
 - Parity checking

SPI

The ARTIK 710 Module provides 2x Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial, National Semiconductor's Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Complies with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Max operating frequency :
 - Master Mode : Support Tx up to 50MHz, Rx up to 20MHz
 - Slave Mode : Support Tx up to 8MHz, Rx up to 8MHz

I²C

The ARTIK 710 Module provides 3x generic I²C blocks supporting both 100kb/s and 400kb/s speed modes. The key features of the I²C sub-system are:

- Supporting multi-master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

USB OTG

The ARTIK 710 Module provides 1x USB2.0 OTG interface supporting both device and host functionality. The key features of the USB2.0 OTG sub-system are:

- In compliance with the USB 2.0 On-The-Go specification revision 1.3a
- Operates in High Speed (480Mbps) Mode
- Operates in Full Speed (12Mbps) Mode
- Operates in Low Speed (1.5Mbps, host only) Mode
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 1 control endpoint 0 for control transfer
- Supports up to 15 device-programmable endpoints:
 - Programmable endpoint type: Bulk, Isochronous, Interrupt
 - Programmable In/Out direction
- Supports 16 host channels

USB HOST/HSIC

The ARTIK 710 Module provides 1x USB2.0 Host controller that is fully compliant with the USB 2.0 specifications, and the Enhanced Host Controller Interface (EHCI) specification. The controller also provides a High Speed Inter Chip (HSIC) version 1.0 module. The key features of the USB2.0 OTG sub-system are:

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level3 revision 1.0
- Controlling the association to either the Open Host Controller Interface or the EHCI via a port router
- Root Hub functionality to support up/down stream port
- Support for HSIC version 1.0

ETHERNET MAC CONTROLLER

The most important features of the Ethernet MAC module are:

- Standard compliance
 - IEEE 802.3az-2010 (Energy Efficient Ethernet EEE)
 - RGMII v2.6
- MAC supports the following features:
 - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external gigabit PHY
 - Full duplex operation
 - Half duplex operation
 - Flexible address filtering
 - Additional frame filtering

SCALER

The ARTIK 710 Module provides a universal scaler. The key features of the scaler are:

- Support for different input formats
 - YUV420, YUV422, YUV444, interleaved UV
- Flexible size, from 8x8 up to 4096x4096 with a granularity of 8
- Upscale ratio from 8x8 to 4096x4096
- Downscale ratio from 4096x4096 to 8x8
- Low-pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

DE-INTERLACER

The ARTIK 710 Module provides a de-interlacer. The key features of the de-interlacer are:

- Support a maximum image width of 1920, image height is not limited

- Y, Cb and Cr are executed separately
- Separated YUV420, YUV422 and YUV444 format support

MULTI FORMAT CODEC

The ARTIK 710 Module provides an integrated Multi Format Codec (MFC) module. The key features of the MFC sub-system are:

- Decoder
 - H.264 : BP, MP, HP Level 4.2 up to 1920x1080, up to 50MBps
 - MPEG4 : Advanced Simple Profile (ASP) up to 1920x1080, up to 40Mbps
 - H.263 : Profile 3 up to 1920x1080, up to 20Mbps
 - VC-1 : SP, MP, AP profile, Level 3 up to 1920x1080, Level 3 up to 2048x1024, up to 45Mbps
 - MPEG 1,2 : Main Profile, High Level up to 1920x1080, up to 80Mbps
 - VP8 : up to 1920x1080, up to 20Mbps
 - Theora : up to 1920x1080, up to 20Mbps
 - AVS : jizhun profile, Level 6.2 up to 1920x1080, up to 40Mbps
 - RV8/9/10 : up to 1920x1080, up to 40Mbps
 - MJPEG : Baseline profile up to 8192x8292
- Encoder
 - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
 - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
 - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps
 - MJPEG : Baseline profile up to 8192x8192

GRAPHICS CONTROLLER

The ARTIK 710 Module provides 1x 2D and 1x 3D graphics accelerator. The key features of the graphics subsystem are:

- 2x pixel processors
 - Tile oriented processing
 - Alpha blending
 - Texture support, non-power-of-2
 - Cube mapping
 - Fast dynamic branching
 - Trigonometric acceleration
 - Full floating point arithmetic
 - Line, quad, triangle and point sprites
 - Perspective correct texturing
 - Point sampling, bilinear and trilinear filtering
 - 8-bit stencil buffering
 - 4-level hierarchical Z and stencil operation
- 1x geometry processor
 - Programmable vertex shader
 - Flexible input and output formats
 - Autonomous operation tile list generation
 - Indexed and non-indexed geometry input
 - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0
- Support for OpenVG 1.1

SECURITY IP

In addition to the Secure Element that is part of the ARTIK 710 Module, the main processor on the module provides additional security features:

- Secure 128-bit die ID
- On chip secure JTAG
 - Secure 128-bit JTAG ID
- On chip secure boot



- Secure 128-bit boot ID
- ARM TrustZone
 - TZPC (TrustZone Platform Controller)
 - TZASC (TrustZone Address Space Controller)
 - TZMA (TrustZone Memory Adapter)
- Hardware crypto accelerators
 - DES, Triple DES
 - AES
 - SHA-1
 - MD5
 - PRNG

PPM PULSE PERIOD MEASUREMENT

The ARTIK 710 Module has a Pulse Period Measurement (PPM) IP-block that can measure the duration of a high level or low level from a GPIO pin. The PPM has a 16-bit counter that is tied to a clock that can vary between 843.750kHz-13.5MHz. For more details on how to relate a PPM to a GPIO please refer to the ARTIK 710 software developer's guide.

MPEG TS

The ARTIK 710 Module provides 1x MPEG Transport Stream de-multiplexer. The most important features of the MPEG-TS are:

- Support for 8-bit parallel mode
- Support for internal and external DMA
- Support for encoding and decoding of AES and CAS based streams
- Support for 2x channel MPEG-TS input with simultaneous 1x channel MPEG-TS output

I²S

The ARTIK 710 Module provides 2x 5-line Inter-IC Sound (I²S) channel. I²S is one of the most popular digital audio interfaces. The I²S bus handles audio data and other signals, such as sub-coding and control. It is possible to transmit data between two I²S buses. The key features of the I²S sub-system are:

- Supports 1-port stereo (1 channel) I²S-bus for audio with DMA based operation
- Supports serial data transfer of 16/24-bit per channel in Master and Slave mode
- Supports a variety of interface modes
 - I²S, Left justified, Right justified, DSP mode

PCM

The ARTIK 710 Module provides 1x PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio codec. The key features of the PCM sub-system are:

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2s complement, left justified, clock MSB first

PWM

The ARTIK 710 Module provides 2x PWM instances. The key features of the PWM sub-system are:

- 2x individual PWM channels with independent duty control and polarity
- 2x 32-bit PWM timers, 1x per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one-shot pulse mode
- Dead zone generator
- Level interrupt generation

GPIO

The ARTIK 710 Module provides a GPIO system with up to 108 GPIOs (77 multiplexed, 31 dedicated) to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- All GPIOs have programmable pull-up control
- All GPIOs have edge detect and level detect
- All GPIOs support programmable pull-up resistance
- All GPIOs can be set for Fast Slew or Normal Slew operation
- All GPIOs can be set for Default Drive Strength or High Drive Strength set by
- All GPIOs support individual interrupt generation and can be triggered on:
 - Rising edge
 - Falling edge
 - High level detection
 - Low level detection
- GPIO data is clocked in at 50MHz

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are:

- Up to 6-channels of analog input can be selected
- Converts analog input into 12-bit binary code up to 1MSPS
- Power consumption 1.0mW when running 1MSPS
- Input frequency up to 100kHz

ARTIK 710 MODULE PADS

The ARTIK 710 Module utilizes 271 signal and ground BALLs providing all the relevant signaling. *Figure 5* shows how the BALLs are oriented and how signal coordinates are assigned to the PADS of the ARTIK 710 Module. *Table 1, Table 2, Table 3* and *Table 4* describe the relation between the BALL coordinates and the BALL signal names. *Table 1, Table 2, Table 3* and *Table 4* also provide detailed characteristics for each BALL signal name.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|---------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|------|------|
| PA1 | PA2 | PA3 | PA4 | PA5 | PA6 | PA7 | PA8 | PA9 | PA10 | PA11 | PA12 | PA13 | PA14 | No Ball | PA16 | PA17 | PA18 | PA19 | PA20 | PA21 | PA22 | PA23 | PA24 | PA25 | PA26 | PA27 | PA28 | PA29 | PA30 | PA31 | PA32 | PA33 | PA34 | PA35 | PA36 | PA37 | PA38 | PA39 | PA40 | PA41 | PA42 | PA43 | | | | | | | | | | | | | | | | | | | | | | |
| PB1 | PB2 | PB3 | PB4 | PB5 | PB6 | PB7 | PB8 | PB9 | PB10 | PB11 | PB12 | PB13 | PB14 | PB15 | PB16 | PB17 | PB18 | PB19 | PB20 | PB21 | PB22 | PB23 | PB24 | PB25 | PB26 | PB27 | PB28 | PB29 | PB30 | PB31 | PB32 | PB33 | PB34 | PB35 | PB36 | PB37 | PB38 | PB39 | PB40 | PB41 | PB42 | PB43 | | | | | | | | | | | | | | | | | | | | | | |
| PC1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PC42 | PC43 | | | | | | | | | | | | | | | | | | | | | | |
| PD1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PD42 | PD43 | | | | | | | | | | | | | | | | | | | | | | |
| PE1 | PE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PE42 | PE43 | | | | | | | | | | | | | | | | | | | | | | |
| PF1 | PF2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PF42 | PF43 | | | | | | | | | | | | | | | | | | | | | | |
| PG1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PG42 | PG43 | | | | | | | | | | | | | | | | | | | | | | |
| PH1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PH42 | PH43 | | | | | | | | | | | | | | | | | | | | | | |
| PI1 | PI2 | | | | | | | | | | | TP282 | TP283 | TP284 | | | | | | | | | | | | | | | | TP285 | TP286 | TP287 | | | | | | | | | | | PI42 | PI43 | | | | | | | | | | | | | | | | | | | | |
| PK1 | PK2 | | | | | | | | | | | TP301 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | TP288 | | | | | | | | | | | PK42 | PK43 |
| PL1 | PL2 | | | | | | | | | | | TP300 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | TP289 | | | | | | | | | | | PL42 | PL43 |
| PM1 | PM2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PM42 | PM43 | | | | | | | | | | | | | | | | | | | | | |
| PN1 | PN2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PN42 | PN43 | | | | | | | | | | | | | | | | | | | | | |
| PP1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PP42 | PP43 | | | | | | | | | | | | | | | | | | | | | | |
| PR1 | PR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PR42 | PR43 | | | | | | | | | | | | | | | | | | | | | | |
| PT1 | PT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PT42 | PT43 | | | | | | | | | | | | | | | | | | | | | | |
| PU1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PU42 | PU43 | | | | | | | | | | | | | | | | | | | | | | |
| PV1 | No Ball | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PV42 | PV43 | | | | | | | | | | | | | | | | | | | | | | |
| PW1 | PW2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PW42 | PW43 | | | | | | | | | | | | | | | | | | | | | | |
| PY1 | PY2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PY42 | PY43 | | | | | | | | | | | | | | | | | | | | | | |
| PAA1 | PAA2 | | | | | | | | | | | TP299 | | | | | | | | | | | | | | | | TP290 | | | | | | | | | | | PAA42 | PAA43 | | | | | | | | | | | | | | | | | | | | | | | | |
| PAB1 | PAB2 | | | | | | | | | | | TP298 | | | | | | | | | | | | | | | | TP291 | | | | | | | | | | | PAB42 | PAB43 | | | | | | | | | | | | | | | | | | | | | | | | |
| PAC1 | PAC2 | | | | | | | | | | | TP297 | TP296 | TP295 | | | | | | | | | | | | | | | | TP294 | TP293 | TP292 | | | | | | | | | | | PAC42 | PAC43 | | | | | | | | | | | | | | | | | | | | |
| PAD1 | PAD2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAD42 | PAD43 | | | | | | | | | | | | | | | | | | | | | |
| PAE1 | PAE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAE42 | PAE43 | | | | | | | | | | | | | | | | | | | | | | |
| PAF1 | PAF2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAF42 | PAF43 | | | | | | | | | | | | | | | | | | | | | | |
| PAG1 | PAG2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAG42 | PAG43 | | | | | | | | | | | | | | | | | | | | | | |
| PAH1 | PAH2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAH42 | PAH43 | | | | | | | | | | | | | | | | | | | | | | |
| PAJ1 | PAJ2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PAJ42 | PAJ43 | | | | | | | | | | | | | | | | | | | | | | |
| PAK1 | PAK2 | PAK3 | PAK4 | PAK5 | PAK6 | PAK7 | PAK8 | PAK9 | PAK10 | PAK11 | PAK12 | PAK13 | PAK14 | PAK15 | PAK16 | PAK17 | PAK18 | PAK19 | PAK20 | PAK21 | PAK22 | PAK23 | PAK24 | PAK25 | PAK26 | PAK27 | PAK28 | PAK29 | PAK30 | PAK31 | PAK32 | PAK33 | PAK34 | PAK35 | PAK36 | PAK37 | PAK38 | PAK39 | PAK40 | PAK41 | PAK42 | PAK43 | | | | | | | | | | | | | | | | | | | | | | |
| PAL1 | PAL2 | PAL3 | PAL4 | PAL5 | PAL6 | PAL7 | PAL8 | PAL9 | PAL10 | PAL11 | PAL12 | PAL13 | PAL14 | PAL15 | PAL16 | PAL17 | PAL18 | PAL19 | PAL20 | PAL21 | PAL22 | PAL23 | PAL24 | PAL25 | PAL26 | PAL27 | PAL28 | PAL29 | PAL30 | PAL31 | PAL32 | PAL33 | PAL34 | PAL35 | PAL36 | PAL37 | PAL38 | PAL39 | PAL40 | PAL41 | PAL42 | PAL43 | | | | | | | | | | | | | | | | | | | | | | |

Figure 5. ARTIK 710 Module Top View BALL Organization

TOP BALL ARRAY

Table 1. TOP BALL ARRAY

| BAL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|---------|------------------|-------|----------------|----------|------|-------|----------|-----------------------------------|
| PA1 | GMAC_TXEN | 3V3 | GMAC_TXEN | S | GPIO | N | GMAC | GMAC Transmit Enable |
| PA2 | GMAC_TXD1 | 3V3 | GMAC_TXD1 | S | GPIO | N | GMAC | GMAC Transmit Data 1 |
| PA3 | GMAC_TXD3 | 3V3 | GMAC_TXD3 | S | GPIO | N | GMAC | GMAC Transmit Data 3 |
| PA4 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PA5 | GMAC_GTXCLK | 3V3 | GMAC_GTXCLK | S | GPIO | N | GMAC | GMAC Transmit Clock |
| PA6 | GMAC_RXDV | 3V3 | GMAC_RXDV | S | GPIO | N | GMAC | GMAC Receive Enable |
| PA7 | GMAC_RXD2 | 3V3 | GMAC_RXD2 | S | GPIO | N | GMAC | GMAC Receive Data 2 |
| PA8 | GMAC_RXD0 | 3V3 | GMAC_RXD0 | S | GPIO | N | GMAC | GMAC Receive Data 0 |
| PA9 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PA10 | AP_MIPICSI_DNCLK | 1V8 | MIPICSI_DNCLK | S | IO | N | CSI | MIPI CSI Data Negative Clock |
| PA11 | AP_MIPICSI_DN0 | 1V8 | MIPICSI_DN0 | S | IO | N | CSI | MIPI CSI Data Negative 0 |
| PA12 | AP_MIPICSI_DN1 | 1V8 | MIPICSI_DN1 | S | IO | N | CSI | MIPI CSI Data Negative 1 |
| PA13 | AP_MIPICSI_DN2 | 1V8 | MIPICSI_DN2 | S | IO | N | CSI | MIPI CSI Data Negative 2 |
| PA14 | AP_MIPICSI_DN3 | 1V8 | MIPICSI_DN3 | S | IO | N | CSI | MIPI CSI Data Negative 3 |
| PA15 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PA16 | AP_MIPIDSI_DNCLK | 1V8 | MIPIDSI_DNCLK | S | IO | N | DSI | MIPI DSI Data Negative Clock |
| PA17 | AP_MIPIDSI_DN0 | 1V8 | MIPIDSI_DN0 | S | IO | N | DSI | MIPI DSI Data Negative 0 |
| PA18 | AP_MIPIDSI_DN1 | 1V8 | MIPIDSI_DN1 | S | IO | N | DSI | MIPI DSI Data Negative 1 |
| PA19 | AP_MIPIDSI_DN2 | 1V8 | MIPIDSI_DN2 | S | IO | N | DSI | MIPI DSI Data Negative 2 |
| PA20 | AP_MIPIDSI_DN3 | 1V8 | MIPIDSI_DN3 | S | IO | N | DSI | MIPI DSI Data Negative 3 |
| PA21 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PA22 | AP_LVDS_TN0 | 1V8 | LVDS_TN0 | S | IO | N | LVDS | LVDS Transmit Channel 0 Negative |
| PA23 | AP_LVDS_TN1 | 1V8 | LVDS_TN1 | S | IO | N | LVDS | LVDS Transmit Channel 1 Negative |
| PA24 | AP_LVDS_TN2 | 1V8 | LVDS_TN2 | S | IO | N | LVDS | LVDS Transmit Channel 2 Negative |
| PA25 | AP_LVDS_TNCLK | 1V8 | LVDS_TNCLK | S | IO | N | LVDS | LVDS Transmit Negative Clock |
| PA26 | AP_LVDS_TN3 | 1V8 | LVDS_TN3 | S | IO | N | LVDS | LVDS Transmit Channel 3 Negative |
| PA27 | AP_LVDS_TN4 | 1V8 | LVDS_TN4 | S | IO | N | LVDS | LVDS Transmit Channel 4 Negative |
| PA28 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PA29 | AP_HDMI_CEC | 3V3 | SA3 | S | GPIO | N | HDMI | HDMI Consumer Electronics Control |
| PA30 | AP_HDMI_TX2N | 1V8 | HDMI_TXN2 | S | O | N | HDMI | HDMI Transmit Channel 1 Negative |
| PA31 | AP_HDMI_TX1N | 1V8 | HDMI_TXN1 | S | O | N | HDMI | HDMI Transmit Channel 0 Negative |
| PA32 | AP_HDMI_TX0N | 1V8 | HDMI_TXN0 | S | O | N | HDMI | HDMI Transmit Channel 2 Negative |
| PA33 | AP_HDMI_TXCN | 1V8 | HDMI_TXNCLK | S | O | N | HDMI | HDMI Transmit Negative Clock |
| PA34 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PA35 | AP_OTG_DM | 3V3 | USB2.0OTG_DM | S | IO | N | USB OTG | USB OTG Data Minus |
| PA36 | AP_USBH_DM | 3V3 | USB2.0HOST_DM | S | IO | N | USB HOST | USB HOST Data Plus |
| PA37 | AP_GPA13 | 3V3 | DISD12 | S | GPIO | N | GPIO | Generic GPIO |
| PA38 | AP_HSIC_STROBE | 1V2 | USBHSIC_STROBE | S | IO | N | HSIC | HSIC Strobe |
| PA39 | AP_GPA14 | 3V3 | DISD13 | S | GPIO | N | GPIO | Generic GPIO |
| PA40 | AP_GPA9 | 3V3 | DISD8 | S | GPIO | N | GPIO | Generic GPIO |
| PA41 | AP_GPA15 | 3V3 | DISD14 | S | GPIO | N | GPIO | Generic GPIO |
| PA42 | AP_GPA12 | 3V3 | DISD11 | S | GPIO | N | GPIO | Generic GPIO |
| PA43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB2 | GMAC_TXD0 | 3V3 | GMAC_TXD0 | S | GPIO | N | GMAC | GMAC Transmit Data 0 |
| PB3 | GMAC_TXD2 | 3V3 | GMAC_TXD2 | S | GPIO | N | GMAC | GMAC Transmit Data 2 |

| BAL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|---------|------------------|-------|----------------|----------|------|-------|----------|----------------------------------|
| PB4 | GMAC_MDC | 3V3 | GMAC_MDC | S | GPIO | N | GMAC | GMAC MDC |
| PB5 | GMAC_RXCLK | 3V3 | GMAC_RXCLK | S | GPIO | N | GMAC | GMAC Receive Clock |
| PB6 | GMAC_RXD3 | 3V3 | GMAC_RXD3 | S | GPIO | N | GMAC | GMAC Receive Data 3 |
| PB7 | GMAC_RXD1 | 3V3 | GMAC_RXD1 | S | GPIO | N | GMAC | GMAC Receive Data 1 |
| PB8 | GMAC_MDIO | 3V3 | GMAC_MDIO | S | GPIO | N | GMAC | GMAC MDIO |
| PB9 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB10 | AP_MIPICSI_DPCLK | 1V8 | MIPICSI_DPCLK | S | IO | N | CSI | MIPI CSI Data Positive Clock |
| PB11 | AP_MIPICSI_DP0 | 1V8 | MIPICSI_DP0 | S | IO | N | CSI | MIPI CSI Data Positive 0 |
| PB12 | AP_MIPICSI_DP1 | 1V8 | MIPICSI_DP1 | S | IO | N | CSI | MIPI CSI Data Positive 1 |
| PB13 | AP_MIPICSI_DP2 | 1V8 | MIPICSI_DP2 | S | IO | N | CSI | MIPI CSI Data Positive 2 |
| PB14 | AP_MIPICSI_DP3 | 1V8 | MIPICSI_DP3 | S | IO | N | CSI | MIPI CSI Data Positive 3 |
| PB15 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB16 | AP_MIPIDSI_DPCLK | 1V8 | MIPIDSI_DPCLK | S | IO | N | DSI | MIPI DSI Data Positive Clock |
| PB17 | AP_MIPIDSI_DP0 | 1V8 | MIPIDSI_DP0 | S | IO | N | DSI | MIPI DSI Data Positive 0 |
| PB18 | AP_MIPIDSI_DP1 | 1V8 | MIPIDSI_DP1 | S | IO | N | DSI | MIPI DSI Data Positive 1 |
| PB19 | AP_MIPIDSI_DP2 | 1V8 | MIPIDSI_DP2 | S | IO | N | DSI | MIPI DSI Data Positive 2 |
| PB20 | AP_MIPIDSI_DP3 | 1V8 | MIPIDSI_DP3 | S | IO | N | DSI | MIPI DSI Data Positive 3 |
| PB21 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB22 | AP_LVDS_TP0 | 1V8 | LVDS_TP0 | S | IO | N | LVDS | LVDS Transmit Channel 0 Positive |
| PB23 | AP_LVDS_TP1 | 1V8 | LVDS_TP1 | S | IO | N | LVDS | LVDS Transmit Channel 1 Positive |
| PB24 | AP_LVDS_TP2 | 1V8 | LVDS_TP2 | S | IO | N | LVDS | LVDS Transmit Channel 2 Positive |
| PB25 | AP_LVDS_TPCLK | 1V8 | LVDS_TPCLK | S | IO | N | LVDS | LVDS Transmit Positive Clock |
| PB26 | AP_LVDS_TP3 | 1V8 | LVDS_TP3 | S | IO | N | LVDS | LVDS Transmit Channel 3 Positive |
| PB27 | AP_LVDS_TP4 | 1V8 | LVDS_TP4 | S | IO | N | LVDS | LVDS Transmit Channel 4 Positive |
| PB28 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB29 | AP_HDMI_HPD | 3V3 | HDMI_HOT5V | S | I | N | HDMI | HDMI Hot 5V |
| PB30 | AP_HDMI_TX2P | 1V8 | HDMI_TXP2 | S | O | N | HDMI | HDMI Transmit Channel 1 Positive |
| PB31 | AP_HDMI_TX1P | 1V8 | HDMI_TXP1 | S | O | N | HDMI | HDMI Transmit Channel 0 Positive |
| PB32 | AP_HDMI_TX0P | 1V8 | HDMI_TXP0 | S | O | N | HDMI | HDMI Transmit Channel 2 Positive |
| PB33 | AP_HDMI_TXCP | 1V8 | HDMI_TXPCLK | S | O | N | HDMI | HDMI Transmit Positive Clock |
| PB34 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PB35 | AP_OTG_DP | 3V3 | USB2.0OTG_DP | S | IO | N | USB OTG | USB OTG Data Plus |
| PB36 | AP_USBH_DP | 3V3 | USB2.0HOST_D P | S | IO | N | USB HOST | USB HOST Data Minus |
| PB37 | AP_OTG_ID | - | USB2.0OTG_ID | S | IO | N | USB HOST | USB HOST ID |
| PB38 | AP_HSIC_DATA | 1V2 | USBHSIC_DATA | S | IO | N | HSIC | HSIC Data |
| PB39 | AP_GPA4 | 3V3 | DISD3 | S | GPIO | N | GPIO | Generic GPIO |
| PB40 | AP_GPA5 | 3V3 | DISD4 | S | GPIO | N | GPIO | Generic GPIO |
| PB41 | AP_GPA16 | 3V3 | DISD15 | S | GPIO | N | GPIO | Generic GPIO |
| PB42 | AP_GPA11 | 3V3 | DISD10 | S | GPIO | N | GPIO | Generic GPIO |
| PB43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |

BOTTOM BALL ARRAY

Table 2. BOTTOM BALL ARRAY

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|--------------------------|-------|------------|----------|------|-------|---------|-------------------------|
| PAK1 | AP_I2S0_DOUT | 3V3 | I2SDOUT0 | S | GPIO | N | I2S0 | I2S 0 Data Out |
| PAK2 | AP_I2S0_BCLK | 3V3 | I2SBCLK0 | S | GPIO | N | I2S0 | I2S 0 Bit Clock |
| PAK3 | AP_GPC11_SPI2_MISO | 3V3 | SA11 | S | GPIO | N | SPI2 | SPI 2 Receive Data |
| PAK4 | AP_GPC9_SPI2_CLK | 3V3 | SA9 | S | GPIO | N | SPI2 | SPI 2 Clock |
| PAK5 | AP_SPI0_MISO | 3V3 | SPIRXD0 | S | GPIO | N | SPI0 | SPI 0 Receive Data |
| PAK6 | AP_SPI0_CLK | 3V3 | SPICLK0 | S | GPIO | N | SPI0 | SPI 0 Clock |
| PAK7 | AP_GPC14_PWM2 | 3V3 | SA14 | S | GPIO | N | PWM | PWM 2 |
| PAK8 | AP_GPD6_SCL | 3V3 | SCL2 | S | GPIO | N | I2C | I2C SCL |
| PAK9 | AP_GPD4_SCL1 | 3V3 | SCL1 | S | GPIO | N | I2C | I2C SCL 1 |
| PAK10 | AP_GPD2_SCL0 | 3V3 | SCL0 | S | GPIO | N | I2C | I2C SCL 0 |
| PAK11 | AP_GPA23_HDMI_I2C_SCL | 3V3 | DISD22 | S | GPIO | N | I2C | HDMI I2C SCL |
| PAK12 | ZB_JTMS | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE JTAG TMS |
| PAK13 | ZB_JTCK | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE JTAG TCK |
| PAK14 | ZB_PC0 | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE Control |
| PAK15 | ZB_PA4 | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE Control |
| PAK16 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAK17 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | POWER | DCDC3, VCC 3V3 Power |
| PAK18 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | POWER | DCDC3, VCC 3V3 Power |
| PAK19 | AP_NBATTFF | 3V3 | AP_NBATTFF | - | NA | - | MISC | Battery |
| PAK20 | AP_GPE2 | 3V3 | VID0_6 | S | GPIO | N | MISC | Miscellaneous |
| PAK21 | AP_GPE1 | 3V3 | VID0_5 | S | GPIO | N | MISC | Miscellaneous |
| PAK22 | AP_UARTTX3 | 3V3 | UARTTXD3 | S | GPIO | N | UART | UART Transmit Data 3 |
| PAK23 | AP_UARTTX4 | 3V3 | SD13 | S | GPIO | N | UART | UART Transmit Data 4 |
| PAK24 | AP_UARTTX5 | 3V3 | SD15 | S | GPIO | N | UART | UART Transmit Data 5 |
| PAK25 | AP_GPB0_VID1_1_I2SLRCK1 | 3V3 | VID1_1 | S | GPIO | N | I2S1 | I2S 1 Left Right Clock |
| PAK26 | AP_GPA28_I2SMCLK1 | 3V3 | VICLK1 | S | GPIO | N | I2S1 | I2S 1 Master Clock |
| PAK27 | AP_GPA30_VID1_0_I2SBCLK1 | 3V3 | VID1_0 | S | GPIO | N | I2S1 | I2S 1 Bit Clock |
| PAK28 | AP_SD0_CMD | 3V3 | SDCMD0 | S | GPIO | N | SD/MMC | SD Command |
| PAK29 | AP_SD0_D1 | 3V3 | SDDAT0_1 | S | GPIO | N | SD/MMC | SD Data 1 |
| PAK30 | AP_SD0_CLK | 3V3 | SDCLK0 | S | GPIO | N | SD/MMC | SD Clock |
| PAK31 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PAK32 | AP_GPB13_SD0_BOOT | 3V3 | SD0 | S | GPIO | N | BOOTING | Select Booting Scenario |
| PAK33 | AP_GPC17 | 3V3 | SA17 | S | GPIO | N | GPIO | Generic GPIO |
| PAK34 | AP_GPC0 | 3V3 | SA0 | S | GPIO | N | GPIO | Generic GPIO |
| PAK35 | AP_GPC26 | 3V3 | RDNWR | S | GPIO | PU | GPIO | Generic GPIO |
| PAK36 | AP_GPB8 | 3V3 | VID1_5 | S | GPIO | N | GPIO | Generic GPIO |
| PAK37 | AP_GPB14 | 3V3 | RNB0 | S | GPIO | N | MISC | Miscellaneous |
| PAK38 | AP_GPA20 | 3V3 | DISD19 | S | GPIO | N | GPIO | Generic GPIO |
| PAK39 | AP_GPA18 | 3V3 | DISD17 | S | GPIO | N | GPIO | Generic GPIO |
| PAK40 | AP_GPA21 | 3V3 | DISD20 | S | GPIO | N | GPIO | Generic GPIO |
| PAK41 | AP_GPA10 | 3V3 | DISD9 | S | GPIO | N | GPIO | Generic GPIO |
| PAK42 | AP_GPA6 | 3V3 | DISD5 | S | GPIO | N | GPIO | Generic GPIO |
| PAK43 | BT_PCM_D_IN | 3V3 | - | - | - | - | BT PCM | PCM Data In |
| PAL1 | AP_I2S0_DIN | 3V3 | I2SDIN0 | S | GPIO | N | I2S0 | I2S 0 Data In |
| PAL2 | AP_I2S0_MCLK | 3V3 | I2SMCLK0 | S | GPIO | N | I2S0 | I2S 0 Master Clock |
| PAL3 | AP_GPC12_SPI2_MOSI | 3V3 | SA12 | S | GPIO | N | SPI2 | SPI 2 Transmit Data |
| PAL4 | AP_GPC10_SPI2_CS | 3V3 | SA10 | S | GPIO | PU | SPI2 | SPI 2 Frame |
| PAL5 | AP_SPI0_MOSI | 3V3 | SPITXD0 | S | GPIO | N | SPI0 | SPI 0 Transmit Data |
| PAL6 | AP_SPI0_CS | 3V3 | SPIFRM0 | S | GPIO | N | SPI0 | SPI 0 Frame |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|-------------------------|-------|----------|----------|------|-------|---------|-------------------------|
| PAL7 | AP_GPD1_PWM0 | 3V3 | PWM0 | S | GPIO | N | PWM | PWM 0 |
| PAL8 | AP_GPD7_SDA | 3V3 | SDA2 | S | GPIO | N | I2C | I2C SDA |
| PAL9 | AP_GPD5_SDA1 | 3V3 | SDA1 | S | GPIO | N | I2C | I2C SDA 1 |
| PAL10 | AP_GPD3_SDA0 | 3V3 | SDA0 | S | GPIO | N | I2C | I2C SDA 0 |
| PAL11 | AP_GPA24_HDMI_I2C_SDA | 3V3 | DISD23 | S | GPIO | N | I2C | HDMI I2C SDA |
| PAL12 | ZB_JTDI | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE JTAG TDI |
| PAL13 | ZB_JTDO | 3V3 | - | - | - | - | ZIGBEE | ZIGBEE JTAG TDO |
| PAL14 | ZB_RSTN | 3V3 | SA8 | S | GPIO | N | ZIGBEE | ZIGBEE Reset |
| PAL15 | ZB_PA5 | 3V3 | NSCS1 | S | GPIO | PU | ZIGBEE | ZIGBEE Control |
| PAL16 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAL17 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | POWER | DCDC3, VCC 3V3 Power |
| PAL18 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | POWER | DCDC3, VCC 3V3 Power |
| PAL19 | AP_VDDPWON | 3V3 | VDDPWON | S | O | N | MISC | VDD Power On |
| PAL20 | AP_GPE3 | 3V3 | VID0_7 | S | GPIO | N | MISC | Miscellaneous |
| PAL21 | AP_GPE0 | 3V3 | VID0_4 | S | GPIO | N | MISC | Miscellaneous |
| PAL22 | AP_UARTRX3 | 3V3 | UARTRXD3 | S | GPIO | N | UART | UART Receive Data 3 |
| PAL23 | AP_UARTRX4 | 3V3 | SD12 | S | GPIO | N | UART | UART Receive Data 4 |
| PAL24 | AP_UARTRX5 | 3V3 | SD14 | S | GPIO | N | UART | UART Receive Data 5 |
| PAL25 | AP_GPD31 | 3V3 | VID0_3 | S | GPIO | N | MISC | Miscellaneous |
| PAL26 | AP_GPB9_I2SDIN1 | 3V3 | VID1_6 | S | GPIO | N | I2S1 | I2S 1 Data In |
| PAL27 | AP_GPB6 VID1_4_I2SDOUT1 | 3V3 | VID1_4 | S | GPIO | N | I2S1 | I2S 1 Data Out |
| PAL28 | AP_SD0_D3 | 3V3 | SDDAT0_3 | S | GPIO | N | SD/MMC | SD Data 3 |
| PAL29 | AP_SD0_D2 | 3V3 | SDDAT0_2 | S | GPIO | N | SD/MMC | SD Data 2 |
| PAL30 | AP_SD0_D0 | 3V3 | SDDAT0_0 | S | GPIO | N | SD/MMC | SD Data 0 |
| PAL31 | AP_GPB4 VID1_3_BOOT | 3V3 | VID1_3 | S | GPIO | N | BOOTING | Select Booting Scenario |
| PAL32 | AP_GPB15_SD1_BOOT | 3V3 | SD1 | S | GPIO | N | BOOTING | Select Booting Scenario |
| PAL33 | AP_GPD8 | 3V3 | SD8 | S | GPIO | N | GPIO | Generic GPIO |
| PAL34 | AP_GPE30 | 3V3 | NSOE | S | GPIO | PU | GPIO | Generic GPIO |
| PAL35 | AP_GPC27 | 3V3 | NSDQM | S | GPIO | PU | GPIO | Generic GPIO |
| PAL36 | AP_GPB22 | 3V3 | SD6 | S | GPIO | N | GPIO | Generic GPIO |
| PAL37 | AP_GPB16 | 3V3 | NNFOE0 | S | GPIO | N | MISC | Miscellaneous |
| PAL38 | AP_GPB23 | 3V3 | SD7 | S | GPIO | N | GPIO | Generic GPIO |
| PAL39 | AP_GPA22 | 3V3 | DISD21 | S | GPIO | N | GPIO | Generic GPIO |
| PAL40 | AP_GPA19 | 3V3 | DISD18 | S | GPIO | N | GPIO | Generic GPIO |
| PAL41 | AP_GPA17 | 3V3 | DISD16 | S | GPIO | N | GPIO | Generic GPIO |
| PAL42 | AP_GPA3 | 3V3 | DISD2 | S | GPIO | N | GPIO | Generic GPIO |
| PAL43 | BT_PCM_CLK | 3V3 | - | - | - | - | BT PCM | PCM Clock |

LEFT BALL ARRAY

Table 3. LEFT BALL ARRAY

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|-------------------|---------|------------|----------|------|-------|-----------|-------------------------------|
| PC1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PC2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PD1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PD2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PE1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PE2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PF1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PF2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PG1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PG2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PH1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PH2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PJ1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PJ2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PK1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PK2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PL1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PL2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PM1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PM2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PN1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PN2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PP1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PP2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PR1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PR2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PT1 | VCC1P8_LDO4 | 0.9-3.5 | - | NA | 1V8 | - | POWER | 1V8 LDO, 25mV Step, 300mA Max |
| PT2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PU1 | VCC1P8_LDO4 | 0.9-3.5 | - | NA | 1V8 | - | POWER | 1V8 LDO, 25mV Step, 300mA Max |
| PU2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PV1 | VCC1P8_LDO4 | 0.9-3.5 | - | NA | 1V8 | - | POWER | 1V8 LDO, 25mV Step, 300mA Max |
| PV2 | NO BALL | - | - | - | - | - | NO BALL | NA |
| PW1 | AP_ADC4 | 1V8 | ADC4 | S | IO | N | ADC | ADC Channel 4 |
| PW2 | AP_ADC5 | 1V8 | ADC5 | S | IO | N | ADC | ADC Channel 5 |
| PY1 | AP_ADC0 | 1V8 | ADC0 | S | IO | N | ADC | ADC Channel 0 |
| PY2 | AP_ADC1 | 1V8 | ADC1 | S | IO | N | ADC | ADC Channel 1 |
| PAA1 | AP_ADC2 | 1V8 | ADC2 | S | IO | N | ADC | ADC Channel 2 |
| PAA2 | AP_ADC3 | 1V8 | ADC3 | S | IO | N | ADC | ADC Channel 3 |
| PAB1 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAB2 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAC1 | AP_TCK | 3V3 | TCLK | S | GPIO | PD | JTAG | JTAG TCK |
| PAC2 | AP_TMS | 3V3 | TMS | S | GPIO | PU | JTAG | JTAG TMS |
| PAD1 | AP_TDO | 3V3 | TDO | S | GPIO | N | JTAG | JTAG TDO |
| PAD2 | AP_TDI | 3V3 | TDI | S | GPIO | PU | JTAG | JTAG TDI |
| PAE1 | AP_NTRST | 3V3 | NTRST | S | GPIO | PU | JTAG | JTAG NTRST |
| PAE2 | AP_AGP2_RTC_INT_N | 3V3 | ALIVEGPIO2 | S | IO | N | KEY/ALIVE | RTC Interrupt |
| PAF1 | AP_PWRKEY | 3V3 | ALIVEGPIO0 | S | IO | N | KEY/ALIVE | Power Key part of AliveGPIO |
| PAF2 | AP_AGP1_HOMEKEY | 3V3 | ALIVEGPIO1 | S | IO | N | KEY/ALIVE | Home Key part of AliveGPIO |
| PAG1 | AP_NRESET | 3V3 | NRESET | S | I | N | KEY | Reset |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|------------------|-------|-----------|----------|------|-------|-------|------------------------|
| PAG2 | AP_GPA25_BACKKEY | 3V3 | DISVSYNC | S | GPIO | N | KEY | Back Key |
| PAH1 | AP_GPA26_VOLUP | 3V3 | DISHSYNC | S | GPIO | N | KEY | Volume Up |
| PAH2 | AP_GPA0_MENUKEY | 3V3 | DISCLK | S | GPIO | N | KEY | Menu Key |
| PAJ1 | AP_I2S0_LRCLK | 3V3 | I2SLRCLK0 | S | GPIO | N | I2S0 | I2S 0 Left Right Clock |
| PAJ2 | AP_GPA27_VOLDOWN | 3V3 | DISDE | S | GPIO | N | KEY | Volume Down |

RIGHT BALL ARRAY

Table 4. RIGHT BALL ARRAY

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|----------------|---------|---------|----------|-----|-------|-------|---|
| PC42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PC43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PD42 | VCC5P0_OTGVBUS | - | - | NA | 5V0 | - | POWER | USB2.0 OTG BUS Power |
| PD43 | VCC5P0_OTGVBUS | - | - | NA | 5V0 | - | POWER | USB2.0 OTG BUS Power |
| PE42 | VCC2P8_LDO7 | 0.9-3.5 | - | NA | 2V8 | - | POWER | 2V8 LDO, 25mV Step, 200mA Max |
| PE43 | VCC2P8_LDO7 | 0.9-3.5 | - | NA | 2V8 | - | POWER | 2V8 LDO, 25mV Step, 200mA Max |
| PF42 | VCC2P8_LDO7 | 0.9-3.5 | - | NA | 2V8 | - | POWER | 2V8 LDO, 25mV Step, 200mA Max |
| PF43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PG42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PG43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PH42 | VCC_LDO5 | 0.6-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PH43 | VCC_LDO5 | 0.6-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PJ42 | VCC_LDO5 | 0.6-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PJ43 | VCC_LDO2 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PK42 | VCC_LDO2 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PK43 | VCC_LDO2 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PL42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PL43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PM42 | VCC_LDO1 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PM43 | VCC_LDO1 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PN42 | VCC_LDO1 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PN43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PP42 | VCC1P2_LDO10 | 0.9-3.5 | - | NA | 1V2 | - | POWER | 1V2 LDO, 25mV Step, 200mA Max |
| PP43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PR42 | VCC1P2_LDO10 | 0.9-3.5 | - | NA | 1V2 | - | POWER | 1V2 LDO, 25mV Step, 200mA Max |
| PR43 | VCC1P2_LDO10 | 0.9-3.5 | - | NA | 1V2 | - | POWER | 1V2 LDO, 25mV Step, 200mA Max |
| PT42 | VCC_LDO9 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PT43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PU42 | VCC_LDO9 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PU43 | VCC_LDO9 | 0.9-3.5 | - | NA | | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PV42 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PV43 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Group | Function |
|----------|--------------|---------|---------|----------|----------|-------|--------|---|
| PW42 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PW43 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PY42 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PY43 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PAA42 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PAA43 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PAB42 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PAB43 | VBAT_MAIN | VBAT | - | NA | | - | POWER | Main Power Supply for Module |
| PAC42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAC43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAD42 | VCC3V3_LDO8 | 0.9-3.5 | - | NA | 3V3 | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PAD43 | VCC3V3_LDO8 | 0.9-3.5 | - | NA | 3V3 | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PAE42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAE43 | VCC3V3_LDO8 | 0.9-3.5 | - | NA | 3V3 | - | POWER | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PAF42 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAF43 | GND | 0V0 | GND | NA | 0V0 | - | GND | Ground |
| PAG42 | AP_GPB11 | 3V3 | CLE0 | S | GPI O | N | GPIO | Generic GPIO |
| PAG43 | AP_GPB18 | 3V3 | NNFWE0 | S | GPI O | N | GPIO | Generic GPIO |
| PAH42 | AP_GPC25 | 3V3 | NSWAIT | S | GPI O | PU | GPIO | Generic GPIO |
| PAH43 | AP_GPE31 | 3V3 | NSWE | S | GPI O | PU | GPIO | Generic GPIO |
| PAJ42 | BT_PCM_D_OUT | 3V3 | - | - | - | - | BT PCM | PCM Data Out |
| PAJ43 | BT_PCM_LRCK | 3V3 | - | - | - | - | BT PCM | PCM LR Clock |

ARTIK 710 MODULE FUNCTIONAL INTERFACES

This section shows the functional interfaces that are available at the PADS of the ARTIK 710 Module. The functions provided are related to the development environment used. Depending on your project, you can always choose to reprogram some of the GPIOs that are currently assigned to the pre-defined functional interfaces.

ADC

Table 5. ADC

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------|-------|---------|----------|-----|-------|---------------|
| PW1 | AP_ADC4 | 1V8 | ADC4 | S | IO | N | ADC Channel 4 |
| PW2 | AP_ADC5 | 1V8 | ADC5 | S | IO | N | ADC Channel 5 |
| PY1 | AP_ADC0 | 1V8 | ADC0 | S | IO | N | ADC Channel 0 |
| PY2 | AP_ADC1 | 1V8 | ADC1 | S | IO | N | ADC Channel 1 |
| PAA1 | AP_ADC2 | 1V8 | ADC2 | S | IO | N | ADC Channel 2 |
| PAA2 | AP_ADC3 | 1V8 | ADC3 | S | IO | N | ADC Channel 3 |

BOOTING

Table 6. Booting

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|---------------------|-------|---------|----------|------|-------|-------------------------|
| PAK32 | AP_GPB13_SD0_BOOT | 3V3 | SD0 | S | GPIO | N | Select Booting Scenario |
| PAL31 | AP_GPB4_VID1_3_BOOT | 3V3 | VID1_3 | S | GPIO | N | Select Booting Scenario |
| PAL32 | AP_GPB15_SD1_BOOT | 3V3 | SD1 | S | GPIO | N | Select Booting Scenario |

BLUETOOTH PCM

Table 7. Bluetooth PCM

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|--------------|-------|---------|----------|-----|-------|--------------|
| PAK43 | BT_PCM_D_IN | 3V3 | - | - | - | - | PCM Data In |
| PAL43 | BT_PCM_CLK | 3V3 | - | - | - | - | PCM Clock |
| PAJ42 | BT_PCM_D_OUT | 3V3 | - | - | - | - | PCM Data Out |
| PAJ43 | BT_PCM_LRCK | 3V3 | - | - | - | - | PCM LR Clock |

MIPI CSI

Table 8. MIPI CSI

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------------|-------|---------------|----------|-----|-------|------------------------------|
| PA10 | AP_MIPICSI_DNCLK | 1V8 | MIPICSI_DNCLK | S | IO | N | MIPI CSI Data Negative Clock |
| PA11 | AP_MIPICSI_DN0 | 1V8 | MIPICSI_DN0 | S | IO | N | MIPI CSI Data Negative 0 |
| PA12 | AP_MIPICSI_DN1 | 1V8 | MIPICSI_DN1 | S | IO | N | MIPI CSI Data Negative 1 |
| PA13 | AP_MIPICSI_DN2 | 1V8 | MIPICSI_DN2 | S | IO | N | MIPI CSI Data Negative 2 |
| PA14 | AP_MIPICSI_DN3 | 1V8 | MIPICSI_DN3 | S | IO | N | MIPI CSI Data Negative 3 |
| PB10 | AP_MIPICSI_DPCLK | 1V8 | MIPICSI_DPCLK | S | IO | N | MIPI CSI Data Positive Clock |
| PB11 | AP_MIPICSI_DP0 | 1V8 | MIPICSI_DP0 | S | IO | N | MIPI CSI Data Positive 0 |
| PB12 | AP_MIPICSI_DP1 | 1V8 | MIPICSI_DP1 | S | IO | N | MIPI CSI Data Positive 1 |
| PB13 | AP_MIPICSI_DP2 | 1V8 | MIPICSI_DP2 | S | IO | N | MIPI CSI Data Positive 2 |
| PB14 | AP_MIPICSI_DP3 | 1V8 | MIPICSI_DP3 | S | IO | N | MIPI CSI Data Positive 3 |

MIPI DSI

Table 9. MIPI DSI

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------------|-------|---------------|----------|-----|-------|------------------------------|
| PA16 | AP_MIPIDSI_DNCLK | 1V8 | MIPIDSI_DNCLK | S | IO | N | MIPI DSI Data Negative Clock |
| PA17 | AP_MIPIDSI_DN0 | 1V8 | MIPIDSI_DN0 | S | IO | N | MIPI DSI Data Negative 0 |
| PA18 | AP_MIPIDSI_DN1 | 1V8 | MIPIDSI_DN1 | S | IO | N | MIPI DSI Data Negative 1 |
| PA19 | AP_MIPIDSI_DN2 | 1V8 | MIPIDSI_DN2 | S | IO | N | MIPI DSI Data Negative 2 |
| PA20 | AP_MIPIDSI_DN3 | 1V8 | MIPIDSI_DN3 | S | IO | N | MIPI DSI Data Negative 3 |
| PB16 | AP_MIPIDSI_DPCLK | 1V8 | MIPIDSI_DPCLK | S | IO | N | MIPI DSI Data Positive Clock |
| PB17 | AP_MIPIDSI_DP0 | 1V8 | MIPIDSI_DP0 | S | IO | N | MIPI DSI Data Positive 0 |
| PB18 | AP_MIPIDSI_DP1 | 1V8 | MIPIDSI_DP1 | S | IO | N | MIPI DSI Data Positive 1 |
| PB19 | AP_MIPIDSI_DP2 | 1V8 | MIPIDSI_DP2 | S | IO | N | MIPI DSI Data Positive 2 |
| PB20 | AP_MIPIDSI_DP3 | 1V8 | MIPIDSI_DP3 | S | IO | N | MIPI DSI Data Positive 3 |

GMAC

Table 10. GMAC

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-------------|-------|-------------|----------|------|-------|----------------------|
| PA1 | GMAC_TXEN | 3V3 | GMAC_TXEN | S | GPIO | N | GMAC Transmit Enable |
| PA2 | GMAC_TXD1 | 3V3 | GMAC_TXD1 | S | GPIO | N | GMAC Transmit Data 1 |
| PA3 | GMAC_TXD3 | 3V3 | GMAC_TXD3 | S | GPIO | N | GMAC Transmit Data 3 |
| PA5 | GMAC_GTXCLK | 3V3 | GMAC_GTXCLK | S | GPIO | N | GMAC Transmit Clock |
| PA6 | GMAC_RXDV | 3V3 | GMAC_RXDV | S | GPIO | N | GMAC Receive Enable |
| PA7 | GMAC_RXD2 | 3V3 | GMAC_RXD2 | S | GPIO | N | GMAC Receive Data 2 |
| PA8 | GMAC_RXD0 | 3V3 | GMAC_RXD0 | S | GPIO | N | GMAC Receive Data 0 |
| PB2 | GMAC_TXD0 | 3V3 | GMAC_TXD0 | S | GPIO | N | GMAC Transmit Data 0 |
| PB3 | GMAC_TXD2 | 3V3 | GMAC_TXD2 | S | GPIO | N | GMAC Transmit Data 2 |
| PB4 | GMAC_MDC | 3V3 | GMAC_MDC | S | GPIO | N | GMAC MDC |
| PB5 | GMAC_RXCLK | 3V3 | GMAC_RXCLK | S | GPIO | N | GMAC Receive Clock |
| PB6 | GMAC_RXD3 | 3V3 | GMAC_RXD3 | S | GPIO | N | GMAC Receive Data 3 |
| PB7 | GMAC_RXD1 | 3V3 | GMAC_RXD1 | S | GPIO | N | GMAC Receive Data 1 |
| PB8 | GMAC_MDIO | 3V3 | GMAC_MDIO | S | GPIO | N | GMAC MDIO |

GPIO

Table 11. GPIO

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------|-------|---------|----------|------|-------|--------------|
| PA37 | AP_GPA13 | 3V3 | DISD12 | S | GPIO | N | Generic GPIO |
| PA39 | AP_GPA14 | 3V3 | DISD13 | S | GPIO | N | Generic GPIO |
| PA40 | AP_GPA9 | 3V3 | DISD8 | S | GPIO | N | Generic GPIO |
| PA41 | AP_GPA15 | 3V3 | DISD14 | S | GPIO | N | Generic GPIO |
| PA42 | AP_GPA12 | 3V3 | DISD11 | S | GPIO | N | Generic GPIO |
| PB39 | AP_GPA4 | 3V3 | DISD3 | S | GPIO | N | Generic GPIO |
| PB40 | AP_GPA5 | 3V3 | DISD4 | S | GPIO | N | Generic GPIO |
| PB41 | AP_GPA16 | 3V3 | DISD15 | S | GPIO | N | Generic GPIO |
| PAK33 | AP_GPC17 | 3V3 | SA17 | S | GPIO | N | Generic GPIO |
| PAK34 | AP_GPC0 | 3V3 | SA0 | S | GPIO | N | Generic GPIO |
| PAK35 | AP_GPC26 | 3V3 | RDNWR | S | GPIO | PU | Generic GPIO |
| PAK36 | AP_GPB8 | 3V3 | VID1_5 | S | GPIO | N | Generic GPIO |
| PAK38 | AP_GPA20 | 3V3 | DISD19 | S | GPIO | N | Generic GPIO |
| PAK39 | AP_GPA18 | 3V3 | DISD17 | S | GPIO | N | Generic GPIO |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------|-------|---------|----------|------|-------|--------------|
| PAK40 | AP_GPA21 | 3V3 | DISD20 | S | GPIO | N | Generic GPIO |
| PAK41 | AP_GPA10 | 3V3 | DISD9 | S | GPIO | N | Generic GPIO |
| PAK42 | AP_GPA6 | 3V3 | DISD5 | S | GPIO | N | Generic GPIO |
| PAL33 | AP_GPD8 | 3V3 | SD8 | S | GPIO | N | Generic GPIO |
| PAL34 | AP_GPE30 | 3V3 | NSOE | S | GPIO | PU | Generic GPIO |
| PAL35 | AP_GPC27 | 3V3 | NSDQM | S | GPIO | PU | Generic GPIO |
| PAL36 | AP_GPB22 | 3V3 | SD6 | S | GPIO | N | Generic GPIO |
| PAL38 | AP_GPB23 | 3V3 | SD7 | S | GPIO | N | Generic GPIO |
| PAL39 | AP_GPA22 | 3V3 | DISD21 | S | GPIO | N | Generic GPIO |
| PAL40 | AP_GPA19 | 3V3 | DISD18 | S | GPIO | N | Generic GPIO |
| PAL41 | AP_GPA17 | 3V3 | DISD16 | S | GPIO | N | Generic GPIO |
| PAL42 | AP_GPA3 | 3V3 | DISD2 | S | GPIO | N | Generic GPIO |
| PB42 | AP_GPA11 | 3V3 | DISD10 | S | GPIO | N | Generic GPIO |
| PAG42 | AP_GPB11 | 3V3 | CLE0 | S | GPIO | N | Generic GPIO |
| PAG43 | AP_GPB18 | 3V3 | NNFWE0 | S | GPIO | N | Generic GPIO |
| PAH42 | AP_GPC25 | 3V3 | NSWAIT | S | GPIO | PU | Generic GPIO |
| PAH43 | AP_GPE31 | 3V3 | NSWE | S | GPIO | PU | Generic GPIO |

HDMI

Table 12. HDMI

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|--------------|-------|-------------|----------|------|-------|-----------------------------------|
| PA29 | AP_HDMI_CEC | 3V3 | SA3 | S | GPIO | N | HDMI Consumer Electronics Control |
| PA30 | AP_HDMI_TX2N | 1V8 | HDMI_TXN2 | S | O | N | HDMI Transmit Channel 1 Negative |
| PA31 | AP_HDMI_TX1N | 1V8 | HDMI_TXN1 | S | O | N | HDMI Transmit Channel 0 Negative |
| PA32 | AP_HDMI_TX0N | 1V8 | HDMI_TXN0 | S | O | N | HDMI Transmit Channel 2 Negative |
| PA33 | AP_HDMI_TXCN | 1V8 | HDMI_TXNCLK | S | O | N | HDMI Transmit Negative Clock |
| PB29 | AP_HDMI_HPD | 3V3 | HDMI_HOT5V | S | I | N | HDMI Hot 5V |
| PB30 | AP_HDMI_TX2P | 1V8 | HDMI_TXP2 | S | O | N | HDMI Transmit Channel 1 Positive |
| PB31 | AP_HDMI_TX1P | 1V8 | HDMI_TXP1 | S | O | N | HDMI Transmit Channel 0 Positive |
| PB32 | AP_HDMI_TX0P | 1V8 | HDMI_TXP0 | S | O | N | HDMI Transmit Channel 2 Positive |
| PB33 | AP_HDMI_TXCP | 1V8 | HDMI_TXPCLK | S | O | N | HDMI Transmit Positive Clock |

HSIC

Table 13. HSIC

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|----------------|-------|----------------|----------|-----|-------|-------------|
| PA38 | AP_HSIC_STROBE | 1V2 | USBHSIC_STROBE | S | IO | N | HSIC Strobe |
| PB38 | AP_HSIC_DATA | 1V2 | USBHSIC_DATA | S | IO | N | HSIC Data |

I²C

Table 14. I²C

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------------------|-------|---------|----------|------|-------|--------------|
| PAK8 | AP_GPD6_SCL | 3V3 | SCL2 | S | GPIO | N | I2C SCL |
| PAK9 | AP_GPD4_SCL1 | 3V3 | SCL1 | S | GPIO | N | I2C SCL 1 |
| PAK10 | AP_GPD2_SCL0 | 3V3 | SCL0 | S | GPIO | N | I2C SCL 0 |
| PAK11 | AP_GPA23_HDMI_I2C_SCL | 3V3 | DISD22 | S | GPIO | N | HDMI I2C SCL |
| PAL8 | AP_GPD7_SDA | 3V3 | SDA2 | S | GPIO | N | I2C SDA |
| PAL9 | AP_GPD5_SDA1 | 3V3 | SDA1 | S | GPIO | N | I2C SDA 1 |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------------------|-------|---------|----------|------|-------|--------------|
| PAL10 | AP_GPD3_SDA0 | 3V3 | SDA0 | S | GPIO | N | I2C SDA 0 |
| PAL11 | AP_GPA24_HDMI_I2C_SDA | 3V3 | DISD23 | S | GPIO | N | HDMI I2C SDA |

I²S

Table 15. I²S

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|--------------------------|-------|-----------|----------|------|-------|------------------------|
| PAK1 | AP_I2S0_DOUT | 3V3 | I2SDOUT0 | S | GPIO | N | I2S 0 Data Out |
| PAK2 | AP_I2S0_BCLK | 3V3 | I2SBCLK0 | S | GPIO | N | I2S 0 Bit Clock |
| PAK25 | AP_GPB0_VID1_1_I2SLRCK1 | 3V3 | VID1_1 | S | GPIO | N | I2S 1 Left Right Clock |
| PAK26 | AP_GPA28_I2SMCLK1 | 3V3 | VICLK1 | S | GPIO | N | I2S 1 Master Clock |
| PAK27 | AP_GPA30_VID1_0_I2SBCLK1 | 3V3 | VID1_0 | S | GPIO | N | I2S 1 Bit Clock |
| PAL1 | AP_I2S0_DIN | 3V3 | I2SDIN0 | S | GPIO | N | I2S 0 Data In |
| PAL2 | AP_I2S0_MCLK | 3V3 | I2SMCLK0 | S | GPIO | N | I2S 0 Master Clock |
| PAL26 | AP_GPB9_I2SDIN1 | 3V3 | VID1_6 | S | GPIO | N | I2S 1 Data In |
| PAL27 | AP_GPB6_VID1_4_I2SDOUT1 | 3V3 | VID1_4 | S | GPIO | N | I2S 1 Data Out |
| PAJ1 | AP_I2S0_LRCLK | 3V3 | I2SLRCLK0 | S | GPIO | N | I2S 0 Left Right Clock |

JTAG

Table 16. JTAG

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------|-------|---------|----------|------|-------|------------|
| PAC1 | AP_TCK | 3V3 | TCLK | S | GPIO | PD | JTAG TCK |
| PAC2 | AP_TMS | 3V3 | TMS | S | GPIO | PU | JTAG TMS |
| PAD1 | AP_TDO | 3V3 | TDO | S | GPIO | N | JTAG TDO |
| PAD2 | AP_TDI | 3V3 | TDI | S | GPIO | PU | JTAG TDI |
| PAE1 | AP_NTRST | 3V3 | NTRST | S | GPIO | PU | JTAG NTRST |

KEY

Table 17. Key

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-------------------|-------|------------|----------|------|-------|-----------------------------|
| PAE2 | AP_AGP2_RTC_INT_N | 3V3 | ALIVEGPIO2 | S | IO | N | RTC Interrupt |
| PAF1 | AP_PWRKEY | 3V3 | ALIVEGPIO0 | S | IO | N | Power Key part of AliveGPIO |
| PAF2 | AP_AGP1_HOMEKEY | 3V3 | ALIVEGPIO1 | S | IO | N | Home Key part of AliveGPIO |
| PAG1 | AP_NRESET | 3V3 | NRESET | S | I | N | Reset |
| PAG2 | AP_GPA25_BACKKEY | 3V3 | DISVSYNC | S | GPIO | N | Back Key |
| PAH1 | AP_GPA26_VOLUP | 3V3 | DISHSYNC | S | GPIO | N | Volume Up |
| PAH2 | AP_GPA0_MENUKEY | 3V3 | DISCLK | S | GPIO | N | Menu Key |
| PAJ2 | AP_GPA27_VOLDOWN | 3V3 | DISDE | S | GPIO | N | Volume Down |

LVDS

Table 18. LVDS

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|---------------|-------|------------|----------|-----|-------|----------------------------------|
| PA22 | AP_LVDS_TN0 | 1V8 | LVDS_TN0 | S | IO | N | LVDS Transmit Channel 0 Negative |
| PA23 | AP_LVDS_TN1 | 1V8 | LVDS_TN1 | S | IO | N | LVDS Transmit Channel 1 Negative |
| PA24 | AP_LVDS_TN2 | 1V8 | LVDS_TN2 | S | IO | N | LVDS Transmit Channel 2 Negative |
| PA25 | AP_LVDS_TNCLK | 1V8 | LVDS_TNCLK | S | IO | N | LVDS Transmit Negative Clock |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|---------------|-------|------------|----------|-----|-------|----------------------------------|
| PA26 | AP_LVDS_TN3 | 1V8 | LVDS_TN3 | S | IO | N | LVDS Transmit Channel 3 Negative |
| PA27 | AP_LVDS_TN4 | 1V8 | LVDS_TN4 | S | IO | N | LVDS Transmit Channel 4 Negative |
| PB22 | AP_LVDS_TP0 | 1V8 | LVDS_TP0 | S | IO | N | LVDS Transmit Channel 0 Positive |
| PB23 | AP_LVDS_TP1 | 1V8 | LVDS_TP1 | S | IO | N | LVDS Transmit Channel 1 Positive |
| PB24 | AP_LVDS_TP2 | 1V8 | LVDS_TP2 | S | IO | N | LVDS Transmit Channel 2 Positive |
| PB25 | AP_LVDS_TPCLK | 1V8 | LVDS_TPCLK | S | IO | N | LVDS Transmit Positive Clock |
| PB26 | AP_LVDS_TP3 | 1V8 | LVDS_TP3 | S | IO | N | LVDS Transmit Channel 3 Positive |
| PB27 | AP_LVDS_TP4 | 1V8 | LVDS_TP4 | S | IO | N | LVDS Transmit Channel 4 Positive |

MISCELLANEOUS

Table 19. Miscellaneous

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------|-------|------------|----------|------|-------|---------------|
| PAK19 | AP_NBATTFF | 3V3 | AP_NBATTFF | - | NA | - | Battery |
| PAK20 | AP_GPE2 | 3V3 | VID0_6 | S | GPIO | N | Miscellaneous |
| PAK21 | AP_GPE1 | 3V3 | VID0_5 | S | GPIO | N | Miscellaneous |
| PAK37 | AP_GPB14 | 3V3 | RNB0 | S | GPIO | N | Miscellaneous |
| PAL19 | AP_VDDPWON | 3V3 | VDDPWON | S | O | N | VDD Power On |
| PAL20 | AP_GPE3 | 3V3 | VID0_7 | S | GPIO | N | Miscellaneous |
| PAL21 | AP_GPE0 | 3V3 | VID0_4 | S | GPIO | N | Miscellaneous |
| PAL25 | AP_GPD31 | 3V3 | VID0_3 | S | GPIO | N | Miscellaneous |
| PAL37 | AP_GPB16 | 3V3 | NNFOE0 | S | GPIO | N | Miscellaneous |

POWER

Table 20. Power

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|----------------|---------|---------|----------|-----|-------|---|
| PAK17 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | DCDC3, VCC 3V3 Power |
| PAK18 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | DCDC3, VCC 3V3 Power |
| PAL17 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | DCDC3, VCC 3V3 Power |
| PAL18 | VCC3P3_SYS | 3V3 | - | NA | 3V3 | - | DCDC3, VCC 3V3 Power |
| PD42 | VCC5P0_OTGVBUS | - | - | NA | 5V0 | - | USB2.0 OTG BUS Power |
| PD43 | VCC5P0_OTGVBUS | - | - | NA | 5V0 | - | USB2.0 OTG BUS Power |
| PE42 | VCC2P8 LDO7 | 0.9-3.5 | - | NA | 2V8 | - | 2V8 LDO, 25mV Step, 200mA Max |
| PE43 | VCC2P8 LDO7 | 0.9-3.5 | - | NA | 2V8 | - | 2V8 LDO, 25mV Step, 200mA Max |
| PF42 | VCC2P8 LDO7 | 0.9-3.5 | - | NA | 2V8 | - | 2V8 LDO, 25mV Step, 200mA Max |
| PH42 | VCC LDO5 | 0.6-3.5 | - | NA | | - | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PH43 | VCC LDO5 | 0.6-3.5 | - | NA | | - | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PJ42 | VCC LDO5 | 0.6-3.5 | - | NA | | - | User Controlled LDO, 0.6-3.5V, 25mV Step, 300mA Max |
| PJ43 | VCC LDO2 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PK42 | VCC LDO2 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PK43 | VCC LDO2 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PM42 | VCC LDO1 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PM43 | VCC LDO1 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PN42 | VCC LDO1 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 300mA Max |
| PP42 | VCC1P2 LDO10 | 0.9-3.5 | - | NA | 1V2 | - | 1V2 LDO, 25mV Step, 200mA Max |
| PR42 | VCC1P2 LDO10 | 0.9-3.5 | - | NA | 1V2 | - | 1V2 LDO, 25mV Step, 200mA Max |
| PT1 | VCC1P8 LDO4 | 0.9-3.5 | - | NA | 1V8 | - | 1V8 LDO, 25mV Step, 300mA Max |
| PR43 | VCC1P2 LDO10 | 0.9-3.5 | - | NA | 1V2 | - | 1V2 LDO, 25mV Step, 200mA Max |
| PT42 | VCC LDO9 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PU1 | VCC1P8 LDO4 | 0.9-3.5 | - | NA | 1V8 | - | 1V8 LDO, 25mV Step, 300mA Max |

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-------------|---------|---------|----------|-----|-------|---|
| PU42 | VCC LDO9 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PU43 | VCC LDO9 | 0.9-3.5 | - | NA | | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PV1 | VCC1P8 LDO4 | 0.9-3.5 | - | NA | 1V8 | - | 1V8 LDO, 25mV Step, 300mA Max |
| PV42 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PV43 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PW42 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PW43 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PY42 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PY43 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PAA42 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PAA43 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PAB42 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PAB43 | VBAT_MAIN | VBAT | - | NA | | - | Main Power Supply for Module |
| PAD42 | VCC3V3 LDO8 | 0.9-3.5 | - | NA | 3V3 | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PAD43 | VCC3V3 LDO8 | 0.9-3.5 | - | NA | 3V3 | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |
| PAE43 | VCC3V3 LDO8 | 0.9-3.5 | - | NA | 3V3 | - | User Controlled LDO, 0.9-3.5V, 25mV Step, 200mA Max |

PWM

Table 21. PWM

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|---------------|-------|---------|----------|------|-------|----------|
| PAK7 | AP_GPC14_PWM2 | 3V3 | SA14 | S | GPIO | N | PWM 2 |
| PAL7 | AP_GPD1_PWM0 | 3V3 | PWM0 | S | GPIO | N | PWM 0 |

SD/MMC

Table 22. SD/MMC

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------|-------|----------|----------|------|-------|------------|
| PAK28 | AP_SD0_CMD | 3V3 | SDCMD0 | S | GPIO | N | SD Command |
| PAK29 | AP_SD0_D1 | 3V3 | SDDAT0_1 | S | GPIO | N | SD Data 1 |
| PAK30 | AP_SD0_CLK | 3V3 | SDCLK0 | S | GPIO | N | SD Clock |
| PAL28 | AP_SD0_D3 | 3V3 | SDDAT0_3 | S | GPIO | N | SD Data 3 |
| PAL29 | AP_SD0_D2 | 3V3 | SDDAT0_2 | S | GPIO | N | SD Data 2 |
| PAL30 | AP_SD0_D0 | 3V3 | SDDAT0_0 | S | GPIO | N | SD Data 0 |

SPI

Table 23. SPI

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|--------------------|-------|---------|----------|------|-------|---------------------|
| PAK3 | AP_GPC11_SPI2_MISO | 3V3 | SA11 | S | GPIO | N | SPI 2 Receive Data |
| PAK4 | AP_GPC9_SPI2_CLK | 3V3 | SA9 | S | GPIO | N | SPI 2 Clock |
| PAK5 | AP_SPI0_MISO | 3V3 | SPIRXD0 | S | GPIO | N | SPI 0 Receive Data |
| PAK6 | AP_SPI0_CLK | 3V3 | SPICLK0 | S | GPIO | N | SPI 0 Clock |
| PAL3 | AP_GPC12_SPI2_MOSI | 3V3 | SA12 | S | GPIO | N | SPI 2 Transmit Data |
| PAL4 | AP_GPC10_SPI2_CS | 3V3 | SA10 | S | GPIO | PU | SPI 2 Frame |
| PAL5 | AP_SPI0_MOSI | 3V3 | SPITXD0 | S | GPIO | N | SPI 0 Transmit Data |
| PAL6 | AP_SPI0_CS | 3V3 | SPIFRM0 | S | GPIO | N | SPI 0 Frame |

UART

Table 24. UART

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------|-------|----------|----------|------|-------|----------------------|
| PAK22 | AP_UARTTX3 | 3V3 | UARTTXD3 | S | GPIO | N | UART Transmit Data 3 |
| PAK23 | AP_UARTTX4 | 3V3 | SD13 | S | GPIO | N | UART Transmit Data 4 |
| PAK24 | AP_UARTTX5 | 3V3 | SD15 | S | GPIO | N | UART Transmit Data 5 |
| PAL22 | AP_UARTRX3 | 3V3 | UARTRXD3 | S | GPIO | N | UART Receive Data 3 |
| PAL23 | AP_UARTRX4 | 3V3 | SD12 | S | GPIO | N | UART Receive Data 4 |
| PAL24 | AP_UARTRX5 | 3V3 | SD14 | S | GPIO | N | UART Receive Data 5 |

USB HOST/USB OTG

Table 25. USB Host/USB OTG

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|------------|-------|---------------|----------|-----|-------|---------------------|
| PA35 | AP_OTG_DM | 3V3 | USB2.0OTG_DM | S | IO | N | USB OTG Data Minus |
| PA36 | AP_USBH_DM | 3V3 | USB2.0HOST_DM | S | IO | N | USB HOST Data Plus |
| PB35 | AP_OTG_DP | 3V3 | USB2.0OTG_DP | S | IO | N | USB OTG Data Plus |
| PB36 | AP_USBH_DP | 3V3 | USB2.0HOST_DP | S | IO | N | USB HOST Data Minus |
| PB37 | AP_OTG_ID | - | USB2.0OTG_ID | S | IO | N | USB HOST ID |

ZIGBEE

Table 26. ZigBee

| BALL LOC | BALL Name | Power | Default | I/O Type | I/O | PU/PD | Function |
|----------|-----------|-------|---------|----------|------|-------|-----------------|
| PAK12 | ZB_JTMS | 3V3 | - | - | - | - | ZIGBEE JTAG TMS |
| PAK13 | ZB_JTCK | 3V3 | - | - | - | - | ZIGBEE JTAG TCK |
| PAK14 | ZB_PC0 | 3V3 | - | - | - | - | ZIGBEE Control |
| PAK15 | ZB_PA4 | 3V3 | - | - | - | - | ZIGBEE Control |
| PAL12 | ZB_JTDI | 3V3 | - | - | - | - | ZIGBEE JTAG TDI |
| PAL13 | ZB_JTDO | 3V3 | - | - | - | - | ZIGBEE JTAG TDO |
| PAL14 | ZB_RSTn | 3V3 | SA8 | S | GPIO | N | ZIGBEE Reset |
| PAL15 | ZB_PA5 | 3V3 | NSCS1 | S | GPIO | PU | ZIGBEE Control |

ARTIK 710 MODULE GPIO ALTERNATE FUNCTIONS

A number of the GPIOs can be programmed to have alternate functions beyond their default behavior using the GPIO API provided in the SW development environment. [Table 27](#), [Table 28](#), [Table 29](#) and

[Table 30](#) provide the alternate functions of all the GPIOs that are available on the PADS of the ARTIK 710 Module that can be user programmed.

Table 27. GPIO Alternate Functions TOP PART

| GPIO Alternate Functions TOP PART | | | | | | | | |
|-----------------------------------|-------------|------------------|------|------------|-------------|------------|------------|-------|
| BALL LOC | Name | Default Function | I/O | Function 0 | Function 1 | Function 2 | Function 3 | Group |
| PA1 | GMAC_TXEN | GMAC_TXEN | GPIO | GPIOE11 | GMAC_TXEN | - | - | GMAC |
| PA2 | GMAC_TXD1 | GMAC_TXD1 | GPIO | GPIOE8 | GMAC_TXD1 | - | - | GMAC |
| PA3 | GMAC_TXD3 | GMAC_TXD3 | GPIO | GPIOE10 | GMAC_TXD3 | - | - | GMAC |
| PA5 | GMAC_GTXCLK | GMAC_GTXCLK | GPIO | GPIOE24 | GMAC_GTXCLK | - | - | GMAC |
| PA6 | GMAC_RXDV | GMAC_RXDV | GPIO | GPIOE19 | GMAC_RXDV | SPITXD1 | - | GMAC |
| PA7 | GMAC_RXD2 | GMAC_RXD2 | GPIO | GPIOE16 | GMAC_RXD2 | - | - | GMAC |
| PA8 | GMAC_RXD0 | GMAC_RXD0 | GPIO | GPIOE14 | GMAC_RXD0 | SPICLK1 | - | GMAC |
| PA29 | AP_HDMI_CEC | SA3 | GPIO | SA3 | GPIOC3 | HDMI_CEC | SDnRST0 | HDMI |
| PA37 | AP_GPA13 | DISD12 | GPIO | GPIOA13 | DISD12 | - | - | GPIO |
| PA39 | AP_GPA14 | DISD13 | GPIO | GPIOA14 | DISD13 | - | - | GPIO |
| PA40 | AP_GPA9 | DISD8 | GPIO | GPIOA9 | DISD8 | - | - | GPIO |
| PA41 | AP_GPA15 | DISD14 | GPIO | GPIOA15 | DISD14 | - | - | GPIO |
| PA42 | AP_GPA12 | DISD11 | GPIO | GPIOA12 | DISD11 | - | - | GPIO |
| PB2 | GMAC_TXD0 | GMAC_TXD0 | GPIO | GPIOE7 | GMAC_TXD0 | VIVSYNC1 | - | GMAC |
| PB3 | GMAC_TXD2 | GMAC_TXD2 | GPIO | GPIOE9 | GMAC_TXD2 | - | - | GMAC |
| PB4 | GMAC_MDC | GMAC_MDC | GPIO | GPIOE20 | GMAC_MDC | - | - | GMAC |
| PB5 | GMAC_RXCLK | GMAC_RXCLK | GPIO | GPIOE18 | GMAC_RXCLK | SPIRXD1 | - | GMAC |
| PB6 | GMAC_RXD3 | GMAC_RXD3 | GPIO | GPIOE17 | GMAC_RXD3 | - | - | GMAC |
| PB7 | GMAC_RXD1 | GMAC_RXD1 | GPIO | GPIOE15 | GMAC_RXD1 | SPIFRM1 | - | GMAC |
| PB8 | GMAC_MDIO | GMAC_MDIO | GPIO | GPIOE21 | GMAC_MDIO | - | - | GMAC |
| PB39 | AP_GPA4 | DISD3 | GPIO | GPIOA4 | DISD3 | - | - | GPIO |
| PB40 | AP_GPA5 | DISD4 | GPIO | GPIOA5 | DISD4 | - | - | GPIO |
| PB41 | AP_GPA16 | DISD15 | GPIO | GPIOA16 | DISD15 | - | - | GPIO |
| PB42 | AP_GPA11 | DISD10 | GPIO | GPIOA11 | DISD10 | - | - | GPIO |

Table 28. GPIO Alternate Functions BOTTOM PART

| GPIO Alternate Functions BOTTOM PART | | | | | | | | |
|--------------------------------------|--------------------------|------------------|------|------------|------------|------------|-------------------|---------|
| BALL LOC | Name | Default Function | I/O | Function 0 | Function 1 | Function 2 | Function 3 | Group |
| PAK1 | AP_I2S0_DOUT | I2SDOUT0 | GPIO | GPIOD9 | I2SDOUT0 | AC97_DOUT | - | I2S0 |
| PAK2 | AP_I2S0_BCLK | I2SBCLK0 | GPIO | GPIOD10 | I2SBCLK0 | AC97_BCLK | - | I2S0 |
| PAK3 | AP_GPC11_SPI2_MISO | SA11 | GPIO | SA11 | GPIOC11 | SPIRXD2 | USB2.0OTG_DrvVBUS | SPI2 |
| PAK4 | AP_GPC9_SPI2_CLK | SA9 | GPIO | SA9 | GPIOC9 | SPICLK2 | PDMStrobe | SPI2 |
| PAK5 | AP_SPI0_MISO | SPIRXD0 | GPIO | GPIOD0 | SPIRXD0 | PWM3 | - | SPI0 |
| PAK6 | AP_SPI0_CLK | SPICLK0 | GPIO | GPIOC29 | SPICLK0 | - | - | SPI0 |
| PAK7 | AP_GPC14_PWM2 | SA14 | GPIO | SA14 | GPIOC14 | PWM2 | VICLK2 | PWM |
| PAK8 | AP_GPD6_SCL | SCL2 | GPIO | GPIOD6 | SCL2 | - | - | I2C |
| PAK9 | AP_GPD4_SCL1 | SCL1 | GPIO | GPIOD4 | SCL1 | - | - | I2C |
| PAK10 | AP_GPD2_SCL0 | SCL0 | GPIO | GPIOD2 | SCL0 | ISO7816 | - | I2C |
| PAK11 | AP_GPA23_HDMI_I2C_SCL | DISD22 | GPIO | GPIOA23 | DISD22 | - | - | I2C |
| PAK20 | AP_GPE2 | VID0_6 | GPIO | GPIOE2 | VID0_6 | TSIDATA1_6 | - | MISC |
| PAK21 | AP_GPE1 | VID0_5 | GPIO | GPIOE1 | VID0_5 | TSIDATA1_5 | - | MISC |
| PAK22 | AP_UARTTX3 | UARTTXD3 | GPIO | GPIOD21 | UARTTXD3 | - | SDnCD1 | UART |
| PAK23 | AP_UARTTX4 | SD13 | GPIO | SD13 | GPIOB29 | TSIDATA0_5 | UARTTXD4 | UART |
| PAK24 | AP_UARTTX5 | SD15 | GPIO | SD15 | GPIOB31 | TSIDATA0_7 | UARTTXD5 | UART |
| PAK25 | AP_GPB0_VID1_1_I2SLRCK1 | VID1_1 | GPIO | GPIOB0 | VID1_1 | SDEX1 | I2SLRCLK1 | I2S1 |
| PAK26 | AP_GPA28_I2SMCLK1 | VICLK1 | GPIO | GPIOA28 | VICLK1 | I2SMCLK2 | I2SMCLK1 | I2S1 |
| PAK27 | AP_GPA30_VID1_0_I2SBCLK1 | VID1_0 | GPIO | GPIOA30 | VID1_0 | SDEX0 | I2SBCLK1 | I2S1 |
| PAK28 | AP_SD0_CMD | SDCMD0 | GPIO | GPIOA31 | SDCMD0 | - | - | SD/MMC |
| PAK29 | AP_SD0_D1 | SDDAT0_1 | GPIO | GPIOB3 | SDDAT0_1 | - | - | SD/MMC |
| PAK30 | AP_SD0_CLK | SDCLK0 | GPIO | GPIOA29 | SDCLK0 | - | - | SD/MMC |
| PAK32 | AP_GPB13_SD0_BOOT | SD0 | GPIO | SD0 | GPIOB13 | - | - | BOOTING |
| PAK33 | AP_GPC17 | SA17 | GPIO | SA17 | GPIOC17 | TSIDP0 | VID2_0 | GPIO |
| PAK34 | AP_GPC0 | SA0 | GPIO | SA0 | GPIOC0 | TSERR0 | - | GPIO |
| PAK35 | AP_GPC26 | RDNWR | GPIO | RDNWR | GPIOC26 | PDMDATA0 | - | GPIO |
| PAK36 | AP_GPB8 | VID1_5 | GPIO | GPIOB8 | VID1_5 | SDEX5 | I2SDOUT2 | GPIO |
| PAK37 | AP_GPB14 | RNB0 | GPIO | RnB0 | RnB1 | GPIOB14 | - | MISC |
| PAK38 | AP_GPA20 | DISD19 | GPIO | GPIOA20 | DISD19 | - | - | GPIO |
| PAK39 | AP_GPA18 | DISD17 | GPIO | GPIOA18 | DISD17 | - | - | GPIO |
| PAK40 | AP_GPA21 | DISD20 | GPIO | GPIOA21 | DISD20 | - | - | GPIO |
| PAK41 | AP_GPA10 | DISD9 | GPIO | GPIOA10 | DISD9 | - | - | GPIO |
| PAK42 | AP_GPA6 | DISD5 | GPIO | GPIOA6 | DISD5 | - | - | GPIO |
| PAL1 | AP_I2S0_DIN | I2SDIN0 | GPIO | GPIOD11 | I2SDIN0 | AC97_DIN | - | I2S0 |
| PAL2 | AP_I2S0_MCLK | I2SMCLK0 | GPIO | GPIOD13 | I2SMCLK0 | AC97_nRST | - | I2S0 |
| PAL3 | AP_GPC12_SPI2_MOSI | SA12 | GPIO | SA12 | GPIOC12 | SPITXD2 | SDnRST2 | SPI2 |
| PAL4 | AP_GPC10_SPI2_CS | SA10 | GPIO | SA10 | GPIOC10 | SPIFRM2 | - | SPI2 |
| PAL5 | AP_SPI0_MOSI | SPITXD0 | GPIO | GPIOC31 | SPITXD0 | - | - | SPI0 |
| PAL6 | AP_SPI0_CS | SPIFRM0 | GPIO | GPIOC30 | SPIFRM0 | - | - | SPI0 |
| PAL7 | AP_GPD1_PWM0 | PWM0 | GPIO | GPIOD1 | PWM0 | SA25 | - | PWM |
| PAL8 | AP_GPD7_SDA | SDA2 | GPIO | GPIOD7 | SDA2 | - | - | I2C |
| PAL9 | AP_GPD5_SDA1 | SDA1 | GPIO | GPIOD5 | SDA1 | - | - | I2C |
| PAL10 | AP_GPD3_SDA0 | SDA0 | GPIO | GPIOD3 | SDA0 | ISO7816 | - | I2C |
| PAL11 | AP_GPA24_HDMI_I2C_SDA | DISD23 | GPIO | GPIOA24 | DISD23 | - | - | I2C |
| PAL14 | ZB_RSTN | SA8 | GPIO | SA8 | GPIOC8 | UARTnDTR1 | SDnINT1 | ZIGBEE |
| PAL15 | ZB_PA5 | NSCS1 | GPIO | GPIOC28 | NSCS1 | UARTnRI1 | - | ZIGBEE |
| PAL20 | AP_GPE3 | VID0_7 | GPIO | GPIOE3 | VID0_7 | TSIDATA1_7 | - | MISC |

| GPIO Alternate Functions BOTTOM PART | | | | | | | | |
|--------------------------------------|-----------------------------|------------------|------|------------|------------|------------|------------|---------|
| BALL LOC | Name | Default Function | I/O | Function 0 | Function 1 | Function 2 | Function 3 | Group |
| PAL21 | AP_GPE0 | VID0_4 | GPIO | GPIOE0 | VID0_4 | TSIDATA1_4 | - | MISC |
| PAL22 | AP_UARTRX3 | UARTRXD3 | GPIO | GIOD17 | UARTRXD3 | - | - | UART |
| PAL23 | AP_UARTRX4 | SD12 | GPIO | SD12 | GPIOB28 | TSIDATA0_4 | UARTRXD4 | UART |
| PAL24 | AP_UARTRX5 | SD14 | GPIO | SD14 | GPIOB30 | TSIDATA0_6 | UARTRXD5 | UART |
| PAL25 | AP_GPD31 | VID0_3 | GPIO | GIOD31 | VID0_3 | TSIDATA1_3 | - | MISC |
| PAL26 | AP_GPB9_I2SDIN1 | VID1_6 | GPIO | GPIOB9 | VID1_6 | SDEX6 | I2SDIN1 | I2S1 |
| PAL27 | AP_GPB6 VID1_4_I2SDOUT 1 | VID1_4 | GPIO | GPIOB6 | VID1_4 | SDEX4 | I2SDOUT1 | I2S1 |
| PAL28 | AP_SD0_D3 | SDDAT0_3 | GPIO | GPIOB7 | SDDAT0_3 | - | - | SD/MMC |
| PAL29 | AP_SD0_D2 | SDDAT0_2 | GPIO | GPIOB5 | SDDAT0_2 | - | - | SD/MMC |
| PAL30 | AP_SD0_D0 | SDDAT0_0 | GPIO | GPIOB1 | SDDAT0_0 | - | - | SD/MMC |
| PAL31 | AP_GPB4 VID1_3_BOOT | VID1_3 | GPIO | GPIOB4 | VID1_3 | SDEX3 | I2SLRCLK2 | BOOTING |
| PAL32 | AP_GPB15_SD1_BOOT | SD1 | GPIO | SD1 | GPIOB15 | - | - | BOOTING |
| PAL33 | AP_GPD8 | SD8 | GPIO | SD8 | GPIOB24 | TSIDATA0_0 | - | GPIO |
| PAL34 | AP_GPE30 | NSOE | GPIO | NSOE | GPIOE30 | - | - | GPIO |
| PAL35 | AP_GPC27 | NSDQM | GPIO | NSDQM | GPIOC27 | PDMDATA1 | - | GPIO |
| PAL36 | AP_GPB22 | SD6 | GPIO | SD6 | GPIOB22 | - | - | GPIO |
| PAL37 | AP_GPB16 | NNFOE0 | GPIO | NNFOE0 | NNFOE1 | GPIOB16 | - | MISC |
| PAL38 | AP_GPB23 | SD7 | GPIO | SD7 | GPIOB23 | - | - | GPIO |
| PAL39 | AP_GPA22 | DISD21 | GPIO | GPIOA22 | DISD21 | - | - | GPIO |
| PAL40 | AP_GPA19 | DISD18 | GPIO | GPIOA19 | DISD18 | - | - | GPIO |
| PAL41 | AP_GPA17 | DISD16 | GPIO | GPIOA17 | DISD16 | - | - | GPIO |
| PAL42 | AP_GPA3 | DISD2 | GPIO | GPIOA3 | DISD2 | - | - | GPIO |

Table 29. GPIO Alternate Functions LEFT PART

| GPIO Alternate Functions LEFT PART | | | | | | | | |
|------------------------------------|------------------|------------------|------|------------|------------|------------|------------|-------|
| BALL LOC | Name | Default Function | I/O | Function 0 | Function 1 | Function 2 | Function 3 | Group |
| PAC1 | AP_TCK | TCLK | GPIO | TCLK | GPIOE28 | - | - | JTAG |
| PAC2 | AP_TMS | TMS | GPIO | TMS | GPIOE26 | - | - | JTAG |
| PAD1 | AP_TDO | TDO | GPIO | TDO | GPIOE29 | - | - | JTAG |
| PAD2 | AP_TDI | TDI | GPIO | TDI | GPIOE27 | - | - | JTAG |
| PAE1 | AP_NTRST | NTRST | GPIO | NTRST | GPIOE25 | - | - | JTAG |
| PAG2 | AP_GPA25_BACKKEY | DISVSYNC | GPIO | GPIOA25 | DISVSYNC | - | - | KEY |
| PAH1 | AP_GPA26_VOLUP | DISHSYNC | GPIO | GPIOA26 | DISHSYNC | - | - | KEY |
| PAH2 | AP_GPA0_MENUKEY | DISCLK | GPIO | GPIOA0 | DISCLK | - | - | KEY |
| PAJ1 | AP_I2S0_LRCLK | I2SLRCLK0 | GPIO | GPIOD12 | I2SLRCLK0 | AC97_SYNC | - | I2S0 |
| PAJ2 | AP_GPA27_VOLDOWN | DISDE | GPIO | GPIOA27 | DISDE | - | - | KEY |

Table 30. GPIO Alternate Functions RIGHT PART

| GPIO Alternate Functions RIGHT PART | | | | | | | | |
|-------------------------------------|----------|------------------|------|------------|------------|------------|------------|-------|
| BALL LOC | Name | Default Function | I/O | Function 0 | Function 1 | Function 2 | Function 3 | Group |
| PAG42 | AP_GPB11 | CLE0 | GPIO | CLE0 | CLE1 | GPIOB11 | - | GPIO |
| PAG43 | AP_GPB18 | NNFWE0 | GPIO | NNFWE0 | nNFWE1 | GPIOB18 | - | GPIO |
| PAH42 | AP_GPC25 | NSWAIT | GPIO | NSWAIT | GPIOC25 | SPDIFTX | - | GPIO |
| PAH43 | AP_GPE31 | NSWE | GPIO | NSWE | GPIOE31 | - | - | GPIO |

ARTIK 710 MODULE BOOTING SEQUENCE

The ARTIK 710 Module supports a variety of booting scenarios as depicted in [Table 31](#). [Table 32](#) describes the values of the PAD signals needed to initiate the various booting scenarios. When nothing is done, default booting will take place.

(AP_GPB13_SD0_BOOT is High, AP_GPB15_SD1_BOOT is Low and AP_GPB4_VID1_3_BOOT is High) In this case, the ARTIK 710 Module will try to boot from eMMC, if this fails, it will continue to initiate a boot from SD0 and if this fails, it will continue booting from the USB device. The other booting scenarios execute in a similar manner. Changing the PAD signals according to the values in [Table 32](#) will allow for different booting options to be executed. By default the ARTIK 710 Module will boot in a non-secure way.

Table 31. Booting Scenarios

| Booting Scenario | Primary Booting Device | Secondary Booting Device | Tertiary Booting Device |
|------------------|------------------------|--------------------------|-------------------------|
| 1 | Boot from eMMC | Boot from SD0 | Boot from USB device |
| 2 | - | Boot from SD0 | Boot from USB device |
| 3 | - | - | Boot from USB device |

Table 32. Booting Options

| Signal Name | Booting Scenario 1 (default) | Booting Scenario 2 | Booting Scenario 3 |
|---------------------|------------------------------|--------------------|--------------------|
| AP_GPB13_SD0_BOOT | High | High | Low |
| AP_GPB15_SD1_BOOT | Low | Low | High |
| AP_GPB4_VID1_3_BOOT | High | Low | X |

ARTIK 710 MODULE POWER STATES

Figure 6 shows the Power Management state diagram. In this diagram the entry and WAKEUP conditions for each power down mode are given.

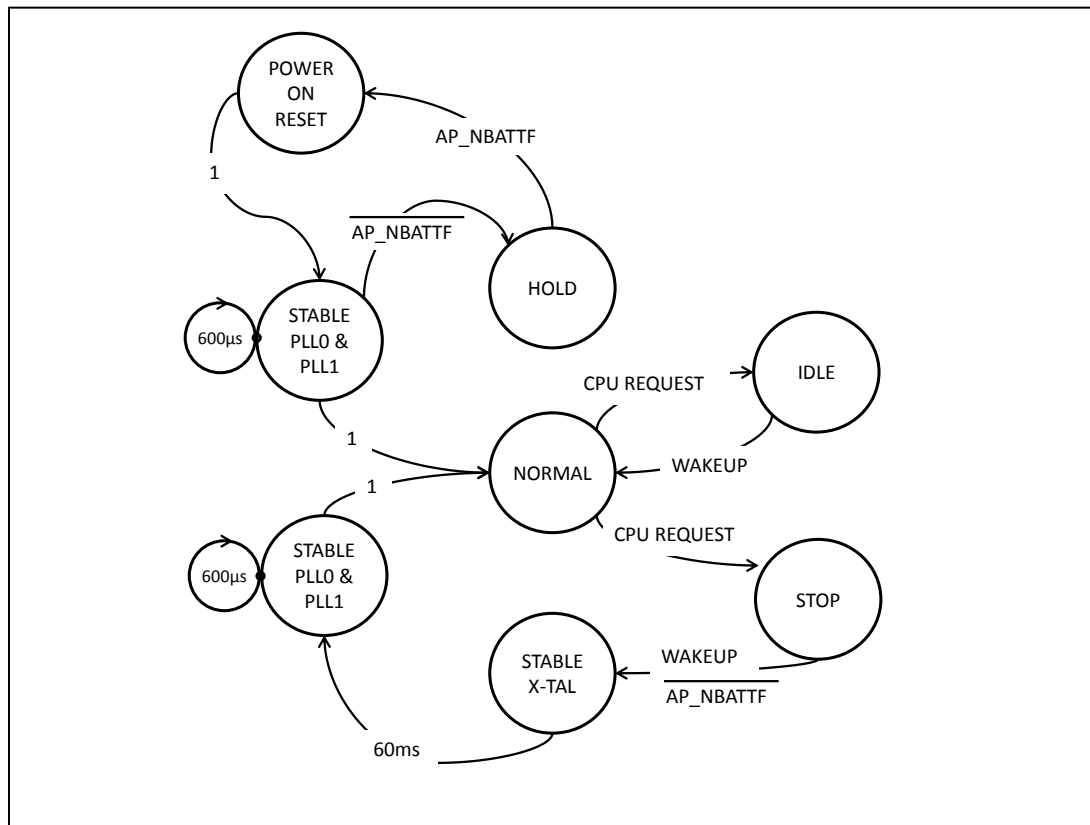


Figure 6. ARTIK 710 Module Power Management State Diagram

The following Modes of operation can be distinguished:

- NORMAL Mode
 - Everything is running, this is the normal mode of operation when applications are executed on the ARM cores
- IDLE Mode
 - CPU clocks are turned off
 - IDLE state can be initiated by CPU using Software API
 - The following WAKEUP sources can be used to return to NORMAL Mode:
- GPIO Interrupt, RTC Interrupt, AliveGPIO Interrupt (see BOT:[AP_AGP2_RTC_INT_N, AP_PWRKEY, AP_AGP1_HOMEKEY]), External IRQ
- STOP Mode
 - PLLs are turned off, DRAM goes into self-refresh
 - STOP state can be initiated by CPU using Software API
 - Certain WAKEUP sources or the ARTIK 710 Module AP_NBATTF signal can be used to transition to NORMAL Mode
 - The following WAKEUP sources can be used to return to NORMAL Mode:
 - RTC Interrupt, AliveGPIO Interrupt

For more information on how to access discussed WAKEUP mechanisms like AliveGPIO interrupts, GPIO Interrupts, RTC Interrupts and External Interrupts, please refer to the Software User Guide.

ARTIK 710 MODULE ANTENNA CONNECTIONS

Two antennas are required to use the full set of radio communication links on the ARTIK 710 Module. One supports the combination of Wi-Fi and BT, and the other is dedicated to 802.15.4 for ZigBee or Thread.

Caution: Do not apply power (enable) the radio chips before connecting antennas or damage to the chip may result.

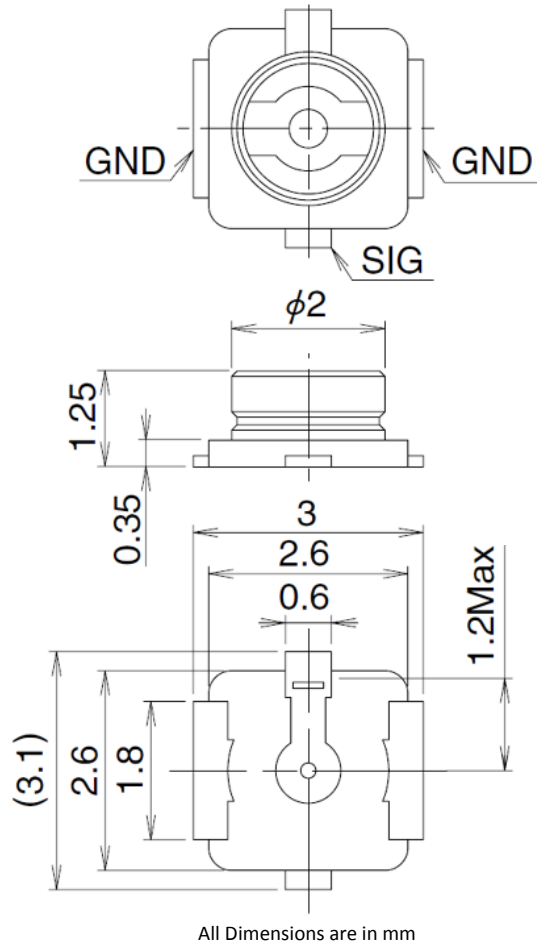


Figure 7. RF Connector for BT/Wi-Fi and ZigBee/Thread

The U.FL-R-SMT Hirose connector is used for both the BT/Wi-Fi and the 802.15.4 for ZigBee or Thread antenna connectors on the ARTIK 710 Module.

The mechanical size of the connector (receptacle) is described in [Figure 7](#). For suggestions on mating plug and more details on the connector, please contact Hirose Electric Co., LTD.

ARTIK 710 MODULE ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 33. Absolute Maximum Ratings

| Absolute Maximum Ratings | | | | | |
|--------------------------|--|--------------------------|------|-----|-------|
| Parameter | Symbol | Condition | Min | Max | Units |
| Main battery supply | VBAT_MAIN | - | -0.3 | 6.0 | |
| DC input/output voltage | PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,14,15,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,42,43] PAH:[1,2,42,43] PAJ:[1,2] | 3.3V Buffer | -0.5 | 3.8 | V |
| | PAK:[43] PAL:[43] PAJ:[42,43] | 3.3V Input/output buffer | -0.5 | 3.8 | |
| | PAK:[12,13,14,15] PAL:[12,13,14,15] | 3.3V Input/output buffer | -0.3 | 3.6 | |
| | PAF:[1] | - | -0.3 | 3.8 | |
| | PAL:[19] | - | -0.3 | 6.3 | |
| DC Input output current | PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,14,15,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,42,43] PAH:[1,2,42,43] PAJ:[1,2] | - | -20 | 20 | mA |
| Storage Temperature | T _A | Commercial | -20 | 85 | °C |
| | T _A | Industrial | TBD | TBD | °C |

RECOMMENDED OPERATING CONDITIONS

The recommended operation of the ARTIK 710 Module is based on the operating conditions listed in [Table 34](#).

Table 34. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------|--|-----|-----|-----|-------|
| Main Battery Supply | VBAT_MAIN PV:[42,43],PW:[42,43],PY:[42,43],PAA:[42,43],PAB:[42,43] | 3.7 | 4.2 | 5.0 | V |
| Operating Temperature | Commercial | 0 | - | 70 | °C |
| | Industrial | TBD | - | TBD | °C |

DC MODULE USE CASE CHARACTERISTICS

POWER SUPPLY REQUIREMENTS

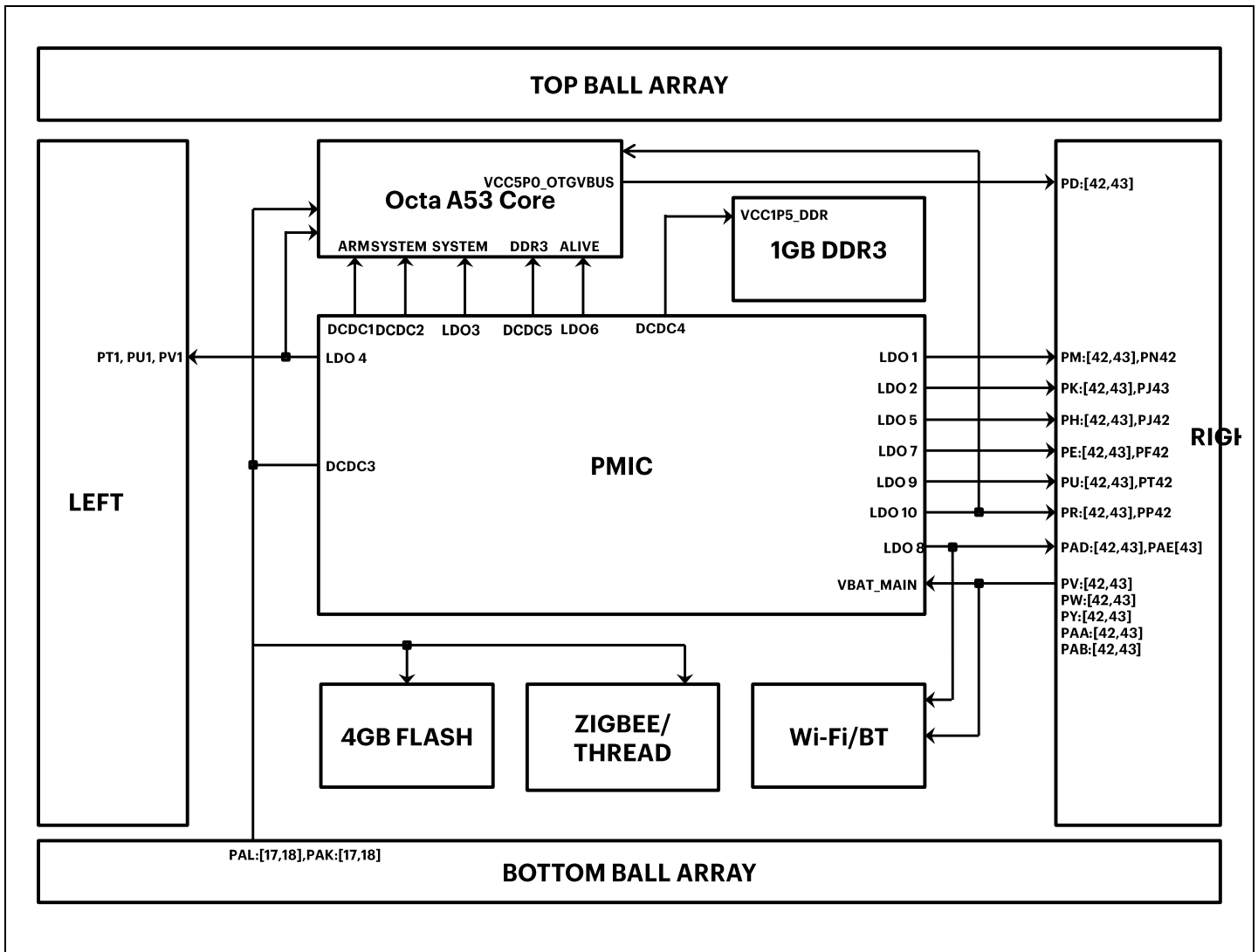


Figure 8. ARTIK 710 Module Power Distribution

The power management of the ARTIK 710 Module as described in [Figure 8](#) is controlled by the PMIC. This PMIC contains 5 high efficiency DC-DC converters and 10 LDO regulators. See [Table 35](#) and [Table 36](#) for details on voltage and amperage ranges and how they are used in the ARTIK 710 Module.

Table 35. DC-DC Converter Description

| Buck | Powers | Header | Max Current [mA] | Range [V] | Default [V] |
|-------|--------------------------------|-------------------------|------------------|-----------|-------------|
| DCDC1 | ARM | - | 4000 | 0.60-3.50 | 1.30 |
| DCDC2 | ARM SoC | - | 4000 | 0.60-3.50 | 1.20 |
| DCDC3 | FLASH, ZIGBEE, GPIO of ARM SoC | PAL:[17,18],PAK:[17,18] | 1000 | 0.60-3.50 | 3.30 |
| DCDC4 | DDR3 Memory | - | 2000 | 0.60-3.50 | 1.50 |
| DCDC5 | DDR3 Memory of ARM SoC | - | 2000 | 0.60-3.50 | 1.50 |

Table 36. PMIC LDOs

| LDO | Powers | Header | Current [mA] | Range [V] | Step [mV] | Default [V] |
|-------|-------------------------------------|---------------------|--------------|-----------|-----------|-------------|
| LDO1 | User Controlled | PM:[42,43],PN42 | 300 | 0.90-3.50 | 25 | - |
| LDO2 | User Controlled | PK:[42,43],PJ43 | 300 | 0.90-3.50 | 25 | - |
| LDO3 | Powers SYSTEM of ARM SoC | - | 300 | 0.90-3.50 | 25 | 1.80 |
| LDO4 | Powers ADC, USB of ARM SoC | PT1, PU1, PV1 | 300 | 0.90-3.50 | 25 | 1.80 |
| LDO5 | User Controlled | PH:[42,43],PJ42 | 300 | 0.60-3.50 | 25 | - |
| LDO6 | Powers 3.3V Alive Signal of ARM SoC | - | 300 | 0.60-3.50 | 25 | 3.30 |
| LDO7 | User Available | PE:[42,43],PF42 | 200 | 0.90-3.50 | 25 | 2.80 |
| LDO8 | User Controlled | PAD:[42,43],PAE[43] | 200 | 0.90-3.50 | 25 | - |
| LDO9 | User Controlled | PU:[42,43],PT42 | 200 | 0.90-3.50 | 25 | - |
| LDO10 | User Available | PR:[42,43],PP42 | 200 | 0.90-3.50 | 25 | 1.20 |

Table 37. AC/DC Characteristics LDO1, LDO2, LDO4

| PM:[42,43], PN42, PK:[42,43], PJ43, PT1, PU1, PV1 | | | | | | |
|---|----------------------------|--|-------|------|------|---------------|
| Operating Conditions $V_{IN}=3.6V$, $C_{OUT}=4.7\mu F$, $T_A=25^\circ C$ unless otherwise specified | | | | | | |
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| V_{IN} | Input Voltage Range | - | 3.70 | 4.20 | 5.00 | V |
| V_{OUT} | Output Voltage Range | $50\mu A < I_{OUT} < I_{OUTMAX}$ | 0.90 | - | 3.50 | V |
| | Voltage Setting Step Width | - | - | 25 | - | mV |
| V_{ACCU} | Output Voltage Accuracy | $V_{OUT} = \text{All Output Range}, I_{OUT}=1mA$ | -1.50 | - | 1.50 | % |
| I_{OUTMAX} | Output Current | - | - | - | 300 | mA |
| I_{LIM} | Limit Current | - | 350 | - | - | mA |
| V_{DIFF} | Dropout Voltage | $V_{OUT} \text{ Setting}=V_{IN}, I_{OUT}=I_{OUTMAX}$ | - | - | 0.20 | V |
| V_{LINE} | Line Regulation | $2.7 < V_{IN} < 5.5V, I_{OUT}=1mA$ | - | - | 0.20 | %/V |
| V_{LOAD} | Load Regulation | $100\mu A < I_{OUT} < I_{OUTMAX}$ | - | - | 30 | mV |
| V_{TR} | Transient Response | $I_{OUT}=100\mu A > I_{OUTMAX}/2$ | - | 50 | - | mV |
| RR | Ripple Rejection | $F=217 \sim 1kHz, I_{OUT}=I_{OUTMAX}/2, V_{DIFF} > 0.6V$ | - | 70 | - | dB |
| O_{NOISE} | Output Noise | $I_{OUT}=I_{OUTMAX}/2, BW=10Hz-100kHz$ | - | 20 | - | μV_{rms} |
| I_{SS} | Supply Current | $I_{OUT}=0mA$ | - | 100 | - | μA |
| I_{OFF} | Standby Current | $I_{OUT}=0mA$ | - | - | 1 | μA |
| T_R | Rising Time | $V_{OUT} \times 0.9, I_{OUT}=0mA$ | - | - | 500 | μs |
| T_F | Falling Time | $V_{OUT} \times 0.1, I_{OUT}=0mA$ | - | - | 1 | ms |
| C_{OUT} | Output Capacitor | - | - | 4.7 | - | μF |

Table 38. AC/DC Characteristics LDO1, LDO2, LDO4 Eco Mode

| PM:[42,43], PN42, PK:[42,43], PJ43, PT1, PU1, PV1 | | | | | | |
|---|----------------------------|--|-------|------|------|---------|
| Operating Conditions $V_{IN}=3.6V$, $C_{OUT}=4.7\mu F$, $T_A=25^\circ C$ unless otherwise specified | | | | | | |
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| V_{IN} | Input Voltage Range | - | 3.70 | 4.20 | 5.00 | V |
| V_{OUT} | Output Voltage Range | $50\mu A < I_{OUT} < I_{OUTMAX}$ | 0.90 | - | 3.50 | V |
| | Voltage Setting Step Width | - | - | 25 | - | mV |
| V_{ACCU} | Output Voltage Accuracy | $V_{OUT} = \text{All Output Range}, I_{OUT}=1mA$ | -1.50 | - | 1.50 | % |
| I_{OUTMAX} | Output Current | Eco Mode | - | - | 10 | mA |
| I_{SS} | Supply Current | - | - | 1 | 1.5 | μA |

Table 39. AC/DC Characteristics LDO5

| PH:[42,43], PJ42 | | | | | | |
|---|----------------------------|--|-------|------|------|---------------|
| Operating Conditions $V_{IN}=3.6V$, $C_{OUT}=1\mu F$, $T_A=25^\circ C$ unless otherwise specified | | | | | | |
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| V_{IN} | Input Voltage Range | - | 3.70 | 4.20 | 5.00 | V |
| V_{OUT} | Output Voltage Range | $50\mu A < I_{OUT} < I_{OUTMAX}$ | 0.60 | - | 3.50 | V |
| | Voltage Setting Step Width | - | - | 25 | - | mV |
| V_{ACCU} | Output Voltage Accuracy | $V_{OUT} = \text{All Output Range}, I_{OUT}=1mA$ | -1.50 | - | 1.50 | % |
| I_{OUTMAX} | Output Current | - | - | - | 300 | mA |
| I_{LIM} | Limit Current | - | 350 | - | - | mA |
| V_{DIFF} | Dropout Voltage | $V_{OUT} \text{ Setting}=V_{IN}, I_{OUT}=I_{OUTMAX}$ | - | - | 0.30 | V |
| V_{LINE} | Line Regulation | $2.7 < V_{IN} < 5.5V, I_{OUT}=1mA$ | - | - | 0.20 | %/V |
| V_{LOAD} | Load Regulation | $100\mu A < I_{OUT} < I_{OUTMAX}$ | - | - | 30 | mV |
| V_{TR} | Transient Response | $I_{OUT}=100\mu A < I_{OUTMAX}/2$ | - | 40 | - | mV |
| RR | Ripple Rejection | $F=217 \sim 1kHz, I_{OUT}=I_{OUTMAX}/2, V_{DIFF} > 0.6V$ | - | 70 | - | dB |
| O_{NOISE} | Output Noise | $I_{OUT}=I_{OUTMAX}/2, BW=10Hz-100kHz$ | - | 100 | - | μV_{rms} |
| I_{SS} | Supply Current | $I_{OUT}=0mA$ | - | 20 | - | μA |
| I_{OFF} | Standby Current | $I_{OUT}=0mA$ | - | - | 1 | μA |
| T_R | Rising Time | $V_{OUT} \times 0.9, I_{OUT}=0mA$ | - | - | 500 | μs |
| T_F | Falling Time | $V_{OUT} \times 0.1, I_{OUT}=0mA$ | - | - | 500 | μs |
| C_{OUT} | Output Capacitor | - | - | 1.0 | - | μF |

Table 40. AC/DC Characteristics LDO5 Eco Mode

| PH:[42,43], PJ42 | | | | | | |
|---|----------------------------|--|-------|------|------|---------|
| Operating Conditions $V_{IN}=3.6V$, $C_{OUT}=1\mu F$, $T_A=25^\circ C$ unless otherwise specified | | | | | | |
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| V_{IN} | Input Voltage Range | - | 3.70 | 4.20 | 5.00 | V |
| V_{OUT} | Output Voltage Range | $50\mu A < I_{OUT} < I_{OUTMAX}$ | 0.60 | - | 3.50 | V |
| | Voltage Setting Step Width | - | - | 25 | - | mV |
| V_{ACCU} | Output Voltage Accuracy | $V_{OUT} = \text{All Output Range}, I_{OUT}=1mA$ | -1.50 | - | 1.50 | % |
| I_{OUTMAX} | Output Current | $V_{IN} > 2.7V$ | - | - | 10 | mA |
| | | $1.7 \leq V_{IN} < 2.7V$ | - | - | 5 | mA |
| I_{SS} | Supply Current | $I_{OUT}=0mA$ | - | 1 | 1.5 | μA |

Table 41. AC/DC Characteristics LDO7, LDO8, LDO9, LDO10

| PE:[42,43], PF42, PAD:[42,43], PAE[43], PU:[42,43], PT42, PR:[42,43], PP42 Operating Conditions $V_{IN}=3.6V$, $C_{OUT}=1\mu F$, $T_A=25^\circ C$ unless otherwise specified | | | | | | |
|---|----------------------------|--|-------|------|------|---------------|
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| V_{IN} | Input Voltage Range | - | 3.70 | 4.20 | 5.00 | V |
| V_{OUT} | Output Voltage Range | $50\mu A < I_{OUT} < I_{OUTMAX}$ | 0.60 | - | 3.50 | V |
| | Voltage Setting Step Width | - | - | 25 | - | mV |
| V_{ACCU} | Output Voltage Accuracy | $V_{OUT} = \text{All Output Range}, I_{OUT}=1mA$ | -1.50 | - | 1.50 | % |
| I_{OUTMAX} | Output Current | - | - | - | 200 | mA |
| I_{LIM} | Limit Current | - | 250 | - | - | mA |
| V_{DIFF} | Dropout Voltage | $V_{OUT} \text{ Setting} = V_{IN}, I_{OUT} = I_{OUTMAX}$ | - | - | 0.40 | V |
| V_{LINE} | Line Regulation | $2.7 < V_{IN} < 5.5V, I_{OUT}=1mA$ | - | - | 0.20 | %/V |
| V_{LOAD} | Load Regulation | $100\mu A < I_{OUT} < I_{OUTMAX}$ | - | - | 20 | mV |
| V_{TR} | Transient Response | $I_{OUT}=100\mu A < I_{OUTMAX}/2$ | - | 30 | - | mV |
| RR | Ripple Rejection | $F=217 \sim 1kHz, I_{OUT}=I_{OUTMAX}/2, V_{DIFF} > 0.6V$ | - | 70 | - | dB |
| O_{NOISE} | Output Noise | $I_{OUT}=I_{OUTMAX}/2, BW=10Hz-100kHz, V_{OUT}=1.2V$ | - | 50 | - | μV_{rms} |
| I_{SS} | Supply Current | $I_{OUT}=0mA$ | - | 20 | - | μA |
| I_{OFF} | Standby Current | $I_{OUT}=0mA$ | - | - | 1 | μA |
| T_R | Rising Time | $V_{OUT} \times 0.9, I_{OUT}=0mA$ | - | - | 500 | μs |
| T_F | Falling Time | $V_{OUT} \times 0.1, I_{OUT}=0mA$ | - | - | 500 | μs |
| C_{OUT} | Output Capacitor | - | - | 1.0 | - | μF |

ESD RATINGS

Table 42. ESD Ratings

| Symbol | Min. | Max. | Units |
|---|------|------|-------|
| ESD stress voltage Human Body Model | - | TBD | kV |
| ESD stress voltage Charged Device Model | - | TBD | V |

Table 43. Shock and Vibration Ratings

| Shock and Vibration | | Range |
|---------------------|---------------|-------|
| Shock | Operating | TBD |
| | Non Operating | TBD |
| Vibration | Operating | TBD |
| | Non Operating | TBD |

DC ELECTRICAL CHARACTERISTICS

The DC characteristics for the GPIO pins of the ARTIK 710 Module are listed in [Table 44](#). Use the parameters from [Table 44](#) to determine maximum DC loading and to determine maximum transition times for a given load.

Table 44. I/O DC Electrical Characteristics GPIO

V_{DD} = 3.3V, V_{ext} = 3.0 to 3.6 V, T_j = -40 to 125 °C (Junction Temperature), 3.30V Tolerant

| GPIO BALL Coordinates | Parameter | Condition | Min | Typ | Max | Units | | |
|--|-----------------------------|---|---|------|------|-------|------|-------------------------------------|
| PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,42,43] PAH:[1,2,42,43] PAJ:[1,2] | V _{TOL} | Tolerant external voltage | V _{DD} Power Off & On | | - | - | 3.60 | V |
| | V _{IH} | High Level Input Voltage | | 2.31 | - | 3.60 | V | |
| | | CMOS Interface | - | | | | | |
| | V _{IL} | Low Level Input Voltage | | -0.3 | - | 0.70 | V | |
| | | CMOS Interface | V _{DD} = 3.3V ± 10 % | | | | | |
| | ΔV | Hysteresis Voltage | | 0.15 | - | | V | |
| | I _{IH} | High Level Input Current | | -3 | - | 3 | μA | |
| | | Input Buffer | V _{IN} = V _{DD} | | | | | V _{DD} Power On |
| | | | | | | | | V _{DD} Power Off & SNS = 0 |
| | Input Buffer with pull-down | V _{IN} = V _{DD} | V _{DD} = 3.3V ± 10 % | 15 | 40 | 80 | | |
| | I _{IL} | Low Level Input Current | | -3 | - | 3 | μA | |
| | | Input Buffer | V _{IN} = V _{SS} | | | | | V _{DD} Power On & Off |
| | | | | | | | | V _{DD} = 3.3V ± 10 % |
| | Input Buffer with pull-up | V _{IN} = V _{SS} | V _{DD} = 3.3V ± 10 % | -15 | -40 | -110 | | |
| | V _{OH} | Output High Voltage | I _{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA | 2.64 | - | 3.30 | V | |
| V _{OL} | Output Low Voltage | I _{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA | 0 | - | 0.66 | V | | |
| I _{OZ} | Output Hi-Z current | - | -5 | - | 5 | μA | | |
| C _{IN} | Input capacitance | Any input and bi-directional buffers | - | - | 5 | pF | | |
| C _{OUT} | Output capacitance | Any output buffer | - | - | 5 | pF | | |

Table 45. I/O DC Electrical Characteristics GPIO

| ZIGBEE/THREAD BALL Coordinates | Parameter | Test Condition | Min | Typ | Max | Units |
|--|---|---|------|-----|------|-------|
| PAK:[12,13,14,15] PAL:[12,13,14,15] | Low Schmitt switching threshold | V _{SWIL} Schmitt input threshold going from high to low | 1.39 | - | 1.65 | V |
| | High Schmitt switching threshold | V _{SWIH} Schmitt input threshold going from low to high | 2.05 | - | 2.64 | V |
| | Input current for logic 0 | I _{IL} | - | - | -0.5 | μA |
| | Input current for logic 1 | I _{IH} | - | - | +0.5 | μA |
| | Input pull-up resistor value | R _{IPU} | 24 | 29 | 34 | kΩ |
| | Input pull-down resistor value | R _{IPD} | 24 | 29 | 34 | kΩ |
| | Output voltage for logic 0 | V _{OL} (I _{OL} = 4mA for standard pads, 8mA for high current pads) | 0 | - | 0.60 | V |
| | Output voltage for logic 1 | V _{OH} (I _{OH} = 4mA for standard pads, 8mA for high current pads) | 2.71 | - | 3.30 | V |
| | Output source current (standard current pad) | I _{OHS} | - | - | 4 | mA |
| | Output sink current (standard current pad) | I _{OLS} | - | - | 4 | mA |
| | Output source current high current pad: BOT:[66] | I _{OHH} | - | - | 8 | mA |

| ZIGBEE/THREAD BALL Coordinates | Parameter | Test Condition | Min | Typ | Max | Units |
|--------------------------------|--|-------------------|-----|-----|-----|-------|
| | Output sink current high current pad: BOT:[66] | I_{OLH} | - | - | 8 | mA |
| | Total output current (for I/O Pads) | $I_{OH} + I_{OL}$ | - | - | 40 | mA |

Table 46. I/O DC Electrical Characteristics PMIC

| PMIC BALL Coordinates | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|-----------------------|--------------------------|----------|----------------|------|-----|------|-------|
| PAF:[1] | Low level input voltage | V_{IL} | - | - | - | 0.40 | V |
| | High level input voltage | V_{IH} | - | 2.31 | - | 3.30 | V |
| PAL:[19] | Low level input voltage | V_{IL} | - | - | - | 0.40 | V |
| | High level input voltage | V_{IH} | - | 1.40 | - | 3.30 | V |

Table 47. I/O DC Electrical Characteristics GPIO

| BALL Coordinates | Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------|--------------------------|----------|-----------|-----|-----|-----|------|
| PAK:[43] PAL:[43] | High level input voltage | V_{IH} | - | 2.0 | - | - | V |
| | Low level input voltage | V_{IL} | - | - | - | 0.8 | |
| PAJ:[42,43] | Output High voltage | V_{OH} | at 2mA | 2.9 | - | - | V |
| | Output Low voltage | V_{OL} | at 2mA | - | - | 0.4 | |

Table 48. GPIO Pull-up Resistor Current

| BALL Coordinates | Condition | Pull Up | Min | Typ | Max | Unit |
|--|--|---------|-----|-----|-----|------|
| PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,42,43] PAH:[1,2,42,43] PAJ:[1,2] | Every GPIO has a 100kΩ internal pull-up resistor | Enable | 10 | 33 | 72 | μA |
| | | Disable | - | - | 0.1 | μA |

*Based on 100kΩ internal pull-up resistor

Table 49. Power on Reset Timing Specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------|---|------|------|------|------|
| t_{RESW} | Reset assert time after clock stabilization | TBD | - | - | ns |

AC ELECTRICAL CHARACTERISTICS

AC characteristics covered in this section are preliminary and are likely to change.

SDMMC AC ELECTRICAL CHARACTERISTICS

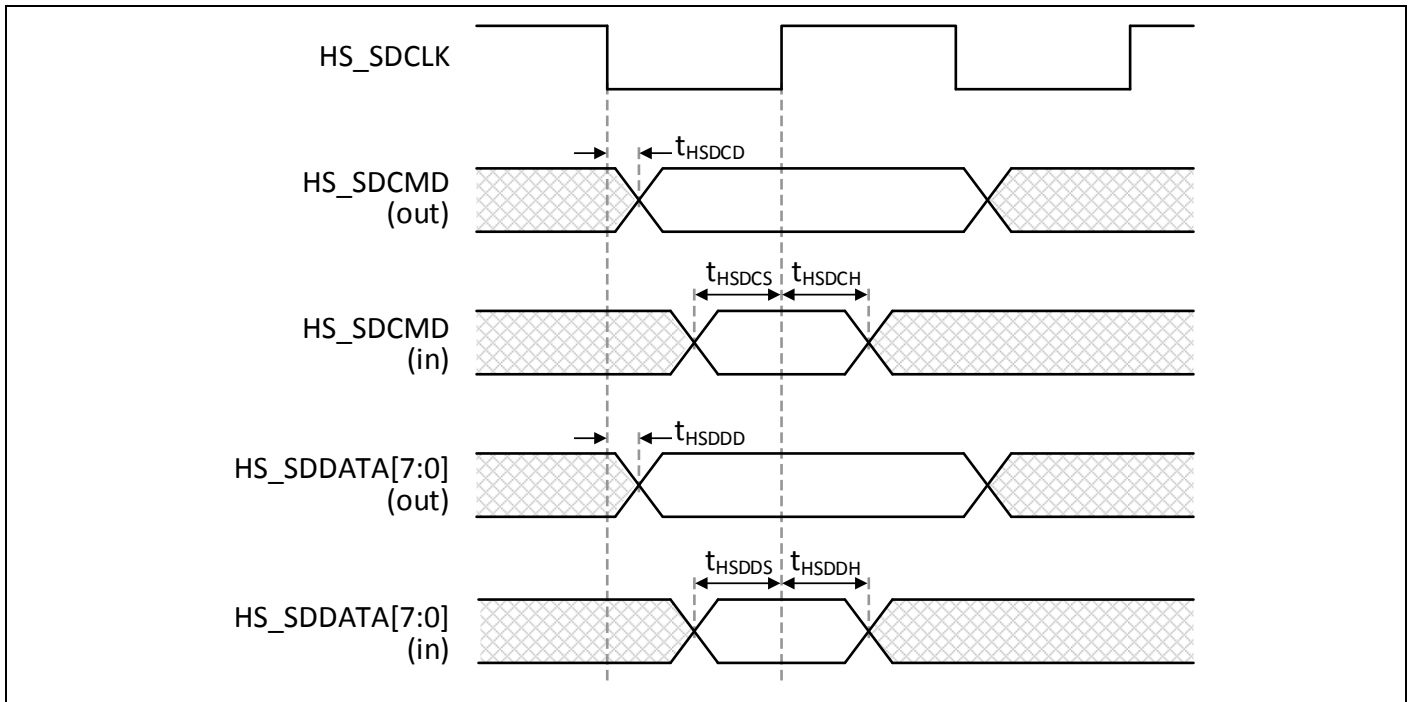


Figure 9. High Speed SDMMC Interface Timing

Table 50. High Speed SDMMC Interface Transmit/Receive Timing Constants

(V_{DDINT} = 1.0V ± 5%, T_A = -25 to 85°C, V_{DDmmc} = 3.3V ± 5%, 2.5V ± 5%, 1.8V ± 5%)

| BOT:[59,60,61,62,63,64] | | | | | |
|-------------------------|------------------------------|-----|-----|-----|------|
| Symbol | Parameter | Min | Typ | Max | Unit |
| t _{SDCD} | SD command output delay time | - | - | 4.0 | ns |
| t _{SDCS} | SD command input setup time | 4.0 | - | - | |
| t _{SDCH} | SD command input hold time | 0 | - | - | |
| t _{SDDD} | SD data output delay time | - | - | 4.0 | |
| t _{SDDS} | SD data input setup time | 4.0 | - | - | |
| t _{SDDH} | SD data input hold time | 0 | - | - | |

SPI AC ELECTRICAL CHARACTERISTICS

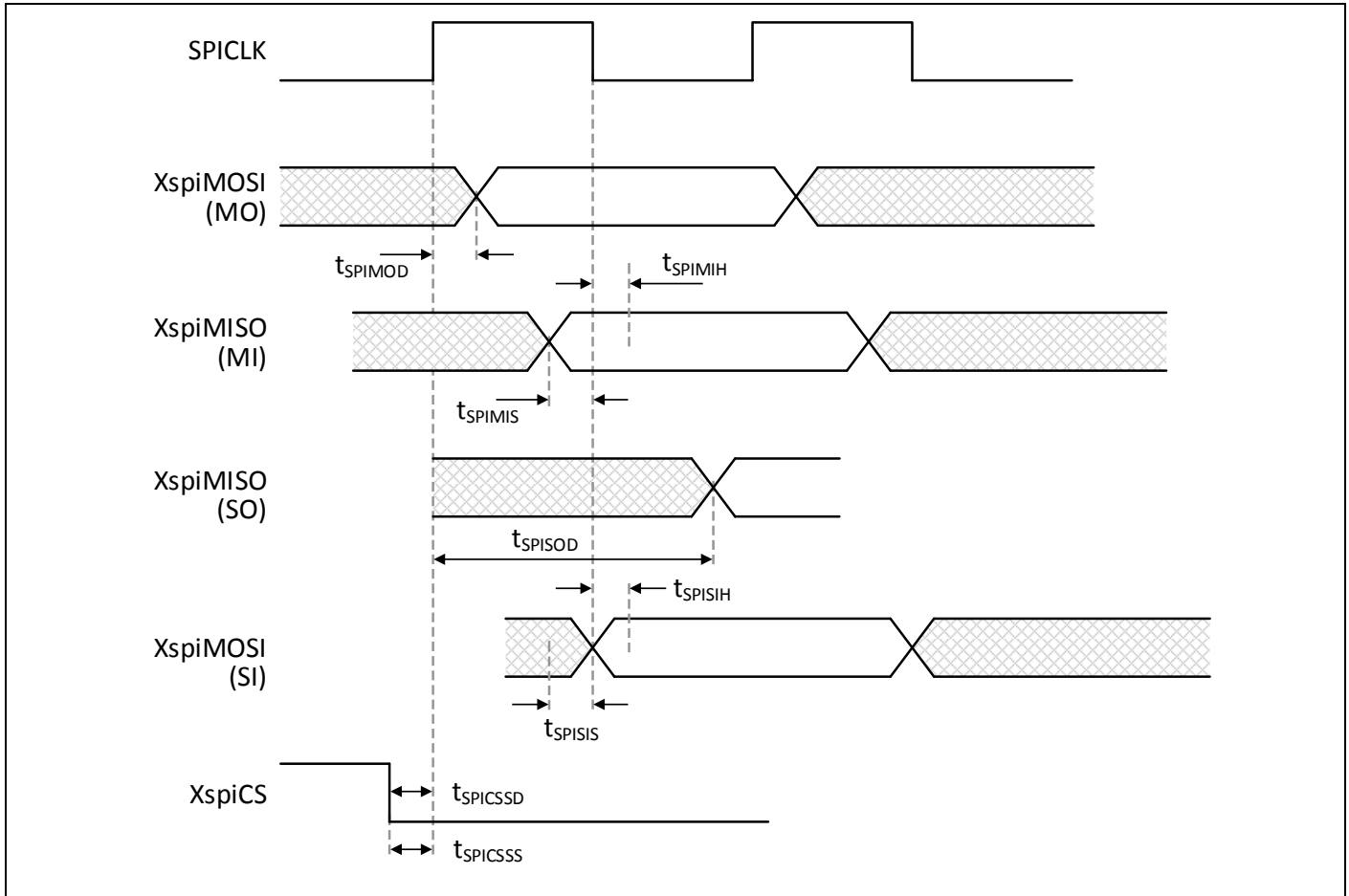


Figure 10. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A))

Table 51. SPI Interface Transmit/ Receive Timing Constants with 15pF Load

(V_{DDINT} = 1.0 V ± 5 %, T_A = -25 to 85 °C, V_{DDext} = 1.8 V ± 10 %, load = 15 pF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | | |
|--|--|----------------------------------|-----------------------------------|---------------------|------|----|----|
| Ch 0 | SPI MOSI Master Output Delay time | t _{SPIMOD} | - | - | 5 | ns | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | t _{SPIMIS} | 12 | - | - | | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) | | 7 | - | - | | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) | | 2 | - | - | | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) | | -3 | - | - | | |
| | SPI MISO Master Input Hold time | | t _{SPIMIHI} | 5 | - | | - |
| | Ch 0 | SPI MOSI Slave Input Setup time | t _{SPISIS} | 2 | - | - | ns |
| | | SPI MOSI Slave Input Hold time | t _{SPISIH} | 5 | - | - | |
| | | SPI MISO Slave Output Delay time | t _{SPISOD} | - | - | 17 | |
| | | SPI nSS Master Output Delay time | t _{SPICSSD} | 7 | - | - | |
| | | SPI nSS Slave Input Setup time | t _{SPICSSS} | 5 | - | - | |
| | | Ch 1 | SPI MOSI Master Output Delay time | t _{SPIMOD} | - | - | |
| SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | t _{SPIMIS} | | 13 | - | - | | |
| SPI MISO Master Input Setup time (FB_CLK_SEL = 01) | | | 8 | - | - | | |
| SPI MISO Master Input Setup time (FB_CLK_SEL = 10) | | | 3 | - | - | | |
| SPI MISO Master Input Setup time (FB_CLK_SEL = 11) | | | -2 | - | - | | |
| SPI MISO Master Input Hold time | | | t _{SPIMIHI} | 5 | - | - | |
| Ch 1 | SPI MOSI Slave Input Setup time | | t _{SPISIS} | 3 | - | - | ns |
| | SPI MOSI Slave Input Hold time | | t _{SPISIH} | 5 | - | - | |
| | SPI MISO Slave Output Delay time | | t _{SPISOD} | - | - | 18 | |
| | SPI nSS Master Output Delay time | | t _{SPICSSD} | 7 | - | - | |
| | SPI nSS Slave Input Setup time | | t _{SPICSSS} | 5 | - | - | |

Note: SPICLKout = 50 MHz

- t_{SPIMIS,CH0} = 12 - (cycle period/4) x FB_CLK_SEL
- t_{SPIMIS,CH1} = 13 - (cycle period/4) x FB_CLK_SEL

Table 52. SPI Interface Transmit/ Receive Timing Constants with 30pF Load

(VDDINT = 1.0 V ± 5 %, TA = -25 to 85 °C, VDDext = 3.3 V ± 10 %, load = 30 pF)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|-----------|--|----------------------|----------------------|------|------|------|
| Ch 0 | SPI MOSI Master Output Delay time | t _{SPIMOD} | - | - | 6 | ns |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | t _{SPIMIS} | 13 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) | | 8 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) | | 3 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) | | -2 | - | - | |
| | SPI MISO Master Input Hold time | | t _{SPIMIHI} | 5 | - | |
| | SPI MOSI Slave Input Setup time | t _{SPISIS} | 4 | - | - | ns |
| | SPI MOSI Slave Input Hold time | t _{SPISIH} | 5 | - | - | |
| | SPI MISO Slave Output Delay time | t _{SPISOD} | - | - | 18 | |
| | SPI nSS Master Output Delay time | t _{SPICSSD} | 8 | - | - | |
| | SPI nSS Slave Input Setup time | t _{SPICSSS} | 6 | - | - | |
| Ch 1 | SPI MOSI Master Output Delay time | t _{SPIMOD} | - | - | 5 | ns |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | t _{SPIMIS} | 14 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) | | 9 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) | | 4 | - | - | |
| | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) | | -1 | - | - | |
| | SPI MISO Master Input Hold time | t _{SPIMIHI} | 5 | - | - | |
| | SPI MOSI Slave Input Setup time | t _{SPISIS} | 4 | - | - | ns |
| | SPI MOSI Slave Input Hold time | t _{SPISIH} | 5 | - | - | |
| | SPI MISO Slave Output Delay time | t _{SPISOD} | - | - | 19 | |
| | SPI nSS Master Output Delay time | t _{SPICSSD} | 8 | - | - | |
| | SPI nSS Slave Input Setup time | t _{SPICSSS} | 6 | - | - | |

Note: SPICLKout = 50 MHz

- t_{SPIMIS,CH0} = 12 - (cycle period/4) x FB_CLK_SEL
- t_{SPIMIS,CH1} = 13 - (cycle period/4) x FB_CLK_SEL

I²C AC ELECTRICAL CHARACTERISTICS

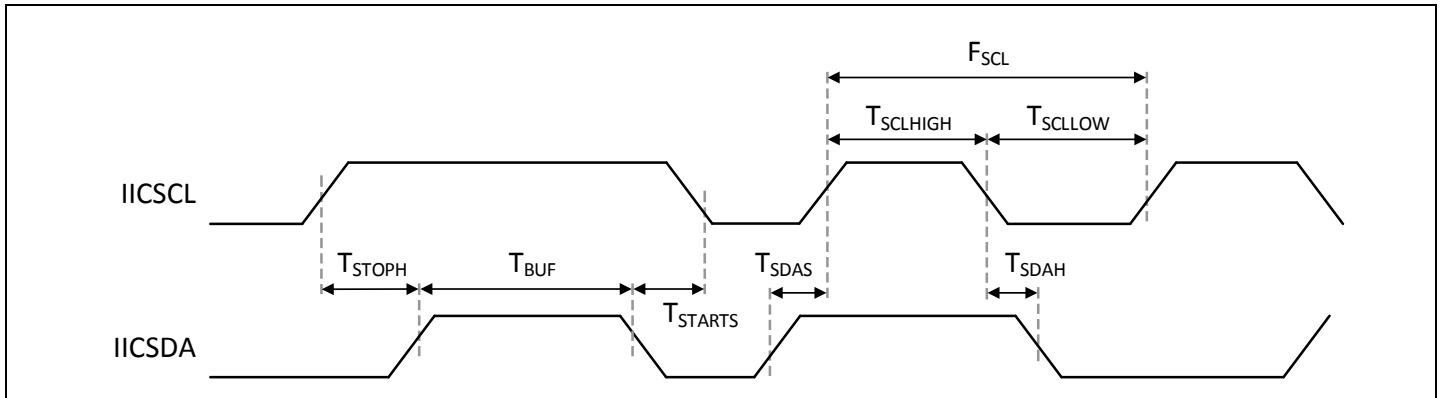


Figure 11. I²C Interface Timing

Table 53. I²C BUS Controller Module Signal Timing

(VDDINT, VDDarm = 1.1 V ± 5 %, T_A = -25 to 85 °C, VDDext = 3.3 V ± 10 %)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|----------------------|----------------------|------|----------------------|------|
| SCL clock frequency | F _{SCL} | - | - | std. 100 fast 400 | kHz |
| SCL high level pulse width | T _{SCLHIGH} | std. 4.0 fast 0.6 | - | - | μs |
| SCL low level pulse width | T _{SCLLOW} | std. 4.7 fast 1.3 | - | - | |
| Bus free time between STOP and START | T _{BUF} | std. 4.7 fast 1.3 | - | - | |
| START hold time | T _{STARTS} | std. 4.0 fast 0.6 | - | - | |
| SDA hold time | T _{SDAH} | std. 0 fast 0 | - | std. fast 0.9 | |
| SDA setup time | T _{SDAS} | std. 250 fast 100 | - | - | ns |
| STOP setup time | T _{STOPH} | std. 4.0 fast 0.6 | - | - | μs |

Note: std. refers to Standard Mode and fast refers to Fast Mode.

1. The I²C data hold time (t_{SDAH}) is minimum 0ns.
(I²C data hold time is minimum 0ns for standard/fast bus mode I²C specification v2.1)
Check whether the data hold time of your I²C device is 0 ns or not.
2. The I²C controller supports I²C bus device only (standard/fast bus mode), and does not support C bus device.

RF ELECTRICAL CHARACTERISTICS

All performance numbers related to 802.11, 802.15.1 and 802.15.4 mentioned in this section are preliminary and likely to change once module characterization has taken place.

Wi-Fi WLAN 2.4GHZ RECEIVER RF SPECIFICATIONS

Table 54. Wi-Fi WLAN 2.4GHz Receiver RF Specifications

| Parameter | Conditions | Min | Typ. | Max | Unit |
|--|--|------|------|------|------|
| Frequency Range | - | 2400 | - | 2500 | MHz |
| Minimum receiver sensitivity in 802.11b mode | | | | | |
| 1Mbps | PER < 8%, Packet size = 1024 bytes | - | - | -92 | dBm |
| 2Mbps | | - | - | -80 | dBm |
| 5.5Mbps | | - | - | -76 | dBm |
| 11Mbps | | - | - | -83 | dBm |
| Minimum receiver sensitivity in 802.11g mode | | | | | |
| 6Mbps | PER < 10%, Packet size= 1024 bytes | - | - | -82 | dBm |
| 9Mbps | | - | - | -81 | dBm |
| 12Mbps | | - | - | -79 | dBm |
| 18Mbps | | - | - | -77 | dBm |
| 24Mbps | | - | - | -74 | dBm |
| 36Mbps | | - | - | -70 | dBm |
| 48Mbps | | - | - | -66 | dBm |
| 54Mbps | | - | - | -65 | dBm |
| Minimum receiver sensitivity in 802.11n mode | | | | | |
| MCS 0 | PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC | - | - | -82 | dBm |
| MCS 1 | | - | - | -79 | dBm |
| MCS 2 | | - | - | -77 | dBm |
| MCS 3 | | - | - | -74 | dBm |
| MCS 4 | | - | - | -70 | dBm |
| MCS 5 | | - | - | -68 | dBm |
| MCS 6 | | - | - | -65 | dBm |
| MCS 7 | | - | - | -64 | dBm |
| Maximum input level | | | | | |
| Maximum input signal level in 802.11b mode | PER < 8% | -10 | - | - | dBm |
| Maximum input signal level in 802.11g mode | PER < 10% | -20 | - | - | dBm |
| Maximum input signal level in 802.11n mode | PER < 10% | -20 | - | - | dBm |

Wi-Fi WLAN 2.4GHz TRANSMITTER RF SPECIFICATIONS

Table 55. Wi-Fi WLAN 2.4GHz Transmitter RF Specifications

| Parameter | Conditions | Min | Typ. | Max | Unit |
|--|------------------------------|-----|------|-----|------|
| Linear output power | | | | | |
| Maximum output power in 802.11b mode | As specified in IEEE802.11 | - | 16 | - | dBm |
| Maximum output power in 802.11g mode | | - | 12.5 | - | dBm |
| Maximum output power in 802.11n mode | | - | 13 | - | dBm |
| Transmit spectrum mask | | | | | |
| Margin to 802.11b spectrum mask | Maximum output power | 0 | - | - | dB |
| Margin to 802.11g spectrum mask | | 0 | - | - | dB |
| Margin to 802.11n spectrum mask | | 0 | - | - | dB |
| Transmit modulation accuracy in 802.11b mode | | | | | |
| 1Mbps | As specified in IEEE 802.11b | - | - | 35 | % |
| 2Mbps | | - | - | 35 | % |
| 5.5Mbps | | - | - | 35 | % |
| 11Mbps | | - | - | 35 | % |
| Transmit modulation accuracy in 802.11g mode | | | | | |
| 6Mbps | Mandatory | - | - | -5 | dB |
| 9Mbps | Optional | - | - | -8 | dB |
| 12Mbps | Mandatory | - | - | -10 | dB |
| 18Mbps | Optional | - | - | -13 | dB |
| 24Mbps | Mandatory | - | - | -16 | dB |
| 36Mbps | Optional | - | - | -19 | dB |
| 48Mbps | Optional | - | - | -22 | dB |
| 54Mbps | Optional | - | - | -25 | dB |
| Transmit modulation accuracy in 802.11n mode | | | | | |
| MCS7 | As specified in IEEE 802.11n | - | - | -27 | dB |
| Transmit power-on and power-down ramp time in 802.11b mode | | | | | |
| Transmit power-on ramp time from 10% to 90% output power | - | - | - | 2 | μs |
| Transmit power-down ramp time from 90% to 10% output power | - | - | - | 2 | μs |

Wi-Fi WLAN 5GHz RECEIVER RF SPECIFICATIONS

Table 56. Wi-Fi WLAN 5GHz Receiver RF Specifications

| Parameter | Conditions | Min | Typ. | Max | Unit |
|--|------------|------|------|------|------|
| Frequency Range | - | 4900 | - | 5845 | MHz |
| Minimum receiver sensitivity in 802.11a mode | | | | | |
| 6Mbps | PER < 10% | - | - | -82 | dBm |
| 12Mbps | | - | - | -79 | dBm |
| 24Mbps | | - | - | -74 | dBm |
| 36Mbps | | - | - | -70 | dBm |
| 48Mbps | | - | - | -66 | dBm |
| 54Mbps | | - | - | -65 | dBm |
| Minimum receiver sensitivity in 802.11n (HT-20) mode | | | | | |
| MCS 0 | - | - | - | -82 | dBm |
| MCS 1 | - | - | - | -79 | dBm |
| MCS 2 | - | - | - | -77 | dBm |
| MCS 3 | - | - | - | -74 | dBm |
| MCS 4 | - | - | - | -70 | dBm |

| Parameter | Conditions | Min | Typ. | Max | Unit |
|--|------------|------|------|------|------|
| Frequency Range | - | 4900 | - | 5845 | MHz |
| MCS 5 | | - | - | -66 | dBm |
| MCS 6 | | - | - | -65 | dBm |
| MCS 7 | | - | - | -64 | dBm |
| Minimum receiver sensitivity in 802.11n (HT-40) mode | | | | | |
| MCS 0 | PER<10 | - | - | -79 | dBm |
| MCS 1 | | - | - | -76 | dBm |
| MCS 2 | | - | - | -74 | dBm |
| MCS 3 | | - | - | -71 | dBm |
| MCS 4 | | - | - | -67 | dBm |
| MCS 5 | | - | - | -63 | dBm |
| MCS 6 | | - | - | -62 | dBm |
| MCS 7 | | - | - | -61 | dBm |
| Minimum receiver sensitivity in 802.11ac (VHT-20) mode | | | | | |
| MCS 0 | PER<10 | - | - | -82 | dBm |
| MCS 1 | | - | - | -79 | dBm |
| MCS 2 | | - | - | -77 | dBm |
| MCS 3 | | - | - | -74 | dBm |
| MCS 4 | | - | - | -70 | dBm |
| MCS 5 | | - | - | -66 | dBm |
| MCS 6 | | - | - | -65 | dBm |
| MCS 7 | | - | - | -64 | dBm |
| MCS 8 | | - | - | -59 | dBm |
| Minimum receiver sensitivity in 802.11ac (VHT-40) mode | | | | | |
| MCS 0 | PER<10 | - | - | -79 | dBm |
| MCS 1 | | - | - | -76 | dBm |
| MCS 2 | | - | - | -74 | dBm |
| MCS 3 | | - | - | -71 | dBm |
| MCS 4 | | - | - | -67 | dBm |
| MCS 5 | | - | - | -63 | dBm |
| MCS 6 | | - | - | -62 | dBm |
| MCS 7 | | - | - | -61 | dBm |
| MCS 8 | | - | - | -56 | dBm |
| MCS 9 | | - | - | -54 | dBm |
| Minimum receiver sensitivity in 802.11ac (VHT-80) mode | | | | | |
| MCS 0 | PER<10 | - | - | -76 | dBm |
| MCS 1 | | - | - | -73 | dBm |
| MCS 2 | | - | - | -71 | dBm |
| MCS 3 | | - | - | -68 | dBm |
| MCS 4 | | - | - | -64 | dBm |
| MCS 5 | | - | - | -60 | dBm |
| MCS 6 | | - | - | -59 | dBm |
| MCS 7 | | - | - | -58 | dBm |
| MCS 8 | | - | - | -53 | dBm |
| MCS 9 | | - | - | -51 | dBm |
| Maximum input level | | | | | |
| Maximum input signal level in 802.11a mode | PER < 10% | -30 | - | - | dBm |
| Maximum input signal level in 802.11n mode | PER < 10% | -30 | - | - | dBm |
| Maximum input signal level in 802.11ac mode | PER < 10% | -30 | - | - | dBm |

Wi-Fi WLAN 5GHz TRANSMITTER RF SPECIFICATIONS

Table 57. Wi-Fi WLAN 5GHz Transmitter RF Specifications

| Parameter | Conditions | Min | Typ. | Max | Unit |
|--|------------------------------|------|------|------|------|
| Frequency Range | - | 4900 | | 5845 | MHz |
| Linear output power | | | | | |
| Maximum output power in 802.11a mode | 54M, UNII-2e | - | 12.5 | - | dBm |
| Maximum output power in 802.11n mode | HT20, MCS7, UNII-2e | - | 12 | - | dBm |
| | HT40, MCS7, UNII-2e | - | 11 | - | dBm |
| Maximum output power in 802.11ac mode | VHT20, MCS8, UNII-2e | - | 12 | - | dBm |
| | VHT40, MCS9, UNII-2e | - | 11 | - | dBm |
| | VHT80, MCS9, UNII-2e | - | 8 | - | dBm |
| Transmit spectrum mask | | | | | |
| Margin to 802.11a spectrum mask | Maximum output power | 0 | - | - | dBr |
| Margin to 802.11n spectrum mask | | 0 | - | - | dBr |
| Margin to 802.11ac spectrum mask | | 0 | - | - | dBr |
| Transmit constellation error in 802.11a mode | | | | | |
| 54Mbps | As specified in IEEE 802.11n | - | - | -25 | dB |
| Transmit constellation error in 802.11n (HT-20, HT-40) mode | | | | | |
| MCS 7 | As specified in IEEE 802.11n | - | - | -27 | dB |
| Transmit constellation error in 802.11ac (VHT-20) mode | | | | | |
| MCS 8 | As specified in IEEE 802.11n | - | - | -30 | dB |
| Transmit constellation error in 802.11ac (VHT-40, VHT-80) mode | | | | | |
| MCS 9 | As specified in IEEE 802.11n | - | - | -32 | dB |

BLUETOOTH RF SPECIFICATIONS

Table 58. Bluetooth Receiver RF Specifications

| Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|----------------------------------|------|-----|------|------|
| Frequency Range | - | 2402 | - | 2480 | MHz |
| Sensitivity (BER) | GPSK, BER \leq 0.1% | - | - | -80 | dBm |
| | $\pi/4$ -DQPSK, BER \leq 0.01% | - | - | -80 | dBm |
| | BER \leq 0.01%, 8DPSK | - | - | -80 | dBm |
| Maximum Input Level | GPSK, BER \leq 0.1% | -20 | - | - | dBm |
| | $\pi/4$ -DQPSK, BER \leq 0.1% | -20 | - | - | dBm |
| | BER \leq 0.1%, 8 DPSK | -20 | - | - | dBm |
| BDR | | | | | |
| Intermodulation Performance | - | - | - | 0.1 | % |
| Rx C/I Performance | 1DH1 | - | - | 0.1 | % |
| | 1DH3 | - | - | 0.1 | % |
| | 1DH5 | - | - | 0.1 | % |
| EDR | | | | | |
| Rx C/I Performance | 2DH1 | - | - | 0.1 | % |
| | 2DH3 | - | - | 0.1 | % |
| | 2DH5 | - | - | 0.1 | % |
| | 3DH1 | - | - | 0.1 | % |
| | 3DH3 | - | - | 0.1 | % |
| | 3DH5 | - | - | 0.1 | % |
| Rx BER Floor Performance | BER \leq 0.001% | - | - | -70 | dBm |

Table 59. Bluetooth Transmitter RF Specifications

| Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|------------|------|-----|------|------|
| Frequency Range | - | 2402 | - | 2480 | MHz |
| Output Power (Average) | | | | | |
| BDR (QPSK) | 2440 MHz | - | 7 | - | dBm |
| EDR ($\pi/4$ -DQPSK) | 2440 MHz | - | 3 | - | dBm |
| EDR (8DPSK) | 2440 MHz | - | 3 | - | dBm |

Table 60. BLE RF Specifications

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------|------|-----|------|------|
| Frequency Range | - | 2402 | - | 2480 | MHz |
| Rx Receiver Sensitivity PER | @ -70dBm | - | - | 30.8 | % |
| Rx C/I and Receiver Selectivity Performance PER | - | - | - | 30.8 | % |
| Tx Power | - | - | 7 | - | dBm |

802.15.4 RF RECEIVE SPECIFICATIONS

Receive measurements were collected with the 802.15.4 SoC Ceramic Balun Reference Design (Version A0) at 2440MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25°C). The Min and Max numbers were measured over process corners at room temperature.

Table 61. 802.15.4 RF Receive Specifications

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|--|------|------|------|------|
| Frequency range | | 2400 | - | 2500 | MHz |
| Sensitivity (boost mode) | 1% PER, 20 byte packet defined by IEEE 802.15.4-2003; | - | -102 | -96 | dBm |
| Sensitivity | 1% PER, 20 byte packet defined by IEEE 802.15.4-2003; | - | -100 | -94 | dBm |
| High-side adjacent channel rejection | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 35 | - | dB |
| Low-side adjacent channel rejection | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 35 | - | dB |
| 2nd high-side adjacent channel rejection | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 46 | - | dB |
| 2nd low-side adjacent channel rejection | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 46 | - | dB |
| High-side adjacent channel rejection | Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 39 | - | dB |
| Low-side adjacent channel rejection | Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 47 | - | dB |
| 2nd high-side adjacent channel rejection | Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 49 | - | dB |
| 2nd low-side adjacent channel rejection | Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 49 | - | dB |
| High-side adjacent channel rejection | CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 44 | - | dB |
| Low-side adjacent channel rejection | CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 47 | - | dB |
| 2nd high-side adjacent channel rejection | CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 59 | - | dB |
| 2nd low-side adjacent channel rejection | CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 59 | - | dB |
| Channel rejection for all other channels | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 40 | - | dB |
| 802.11g rejection centered at +12 MHz or -13 MHz | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | 36 | - | dB |
| Maximum input signal level for correct operation | | 0 | - | - | dBm |
| Co-channel rejection | IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm | - | -6 | - | dBc |
| Relative frequency error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003) | | -120 | - | +120 | ppm |
| Relative timing error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003) | | -120 | - | +120 | ppm |
| Linear RSSI range | As defined by IEEE 802.15.4-2003 | 40 | - | - | dB |
| RSSI Range | | -90 | - | -40 | dB |

802.15.4 RF TRANSMIT SPECIFICATIONS

Transmit measurements were collected with the Silicon Labs 802.15.4 SoC ceramic balun reference design (Version A0) at 2440MHz. The typical number indicates one standard deviation below the mean, measured at room temperature of 25°C. The Min and Max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3n3 inductor in parallel with a 100:50Ω balun to the RF pins.

Table 62. ZigBee/Thread RF Transmit Specifications

| Parameter | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|--|-----|-----|-----|------|
| Maximum output power | At highest normal mode power setting (+3) | -3 | 6.5 | - | dBm |
| Minimum output power | At lowest power setting | - | -55 | - | dBm |
| Error vector magnitude (Offset-EVM) | As defined by IEEE 802.15.4-2003, which sets a 35% maximum | - | - | 10 | % |
| Carrier frequency error | - | -40 | - | +40 | ppm |
| PSD mask relative | 3.5 MHz away (Normal) | -20 | - | - | dBm |
| PSD mask absolute | 100 KHz BW | -30 | - | - | dBm |

Table 63. ZigBee/Thread RF Receive Specifications

| Parameter | Test Condition | Min | Typ | Max | Unit |
|--|---|------|-----|--------|------|
| Operating Frequency Range | | 2400 | - | 2483.5 | MHz |
| Receiver Sensitivity PER | @[-95dBm] | - | - | 1 | % |
| Receiver Sensitivity Search | @PER 1% | - | - | -95 | dBm |
| Receiver Interference Rejection PER | @[-2 Channel, Alternate Channel, 30dB] | - | - | 1 | % |
| Receiver Interference Rejection PER | @[-1 Channel, Adjacent Channel, 0dB] | - | - | 1 | % |
| Receiver Interference Rejection PER | @ [+1 Channel, Adjacent Channel, 0dB] | - | - | 1 | % |
| Receiver Interference Rejection PER | @ [+2 Channel, Alternate Channel, 30dB] | - | - | 1 | % |
| Error Vector Magnitude - RMS (EVM) | @ [Target Power] | - | - | 30 | % |
| Error Vector Magnitude - Offset (EVM) | @ [Target Power] | - | - | 10 | % |
| Receiver Maximum Input Level of Desired Signal | @ [-20dBm Input] | - | - | 1 | % |

ARTIK 710 MODULE MECHANICAL SPECIFICATIONS

The ARTIK 710 Module supports PAD Balls and two RF connectors on a 49mm x 36mm footprint. Refer to section [ARTIK 710 Module Antenna Connections](#) for RF connector details. [Figure 12](#) and [Figure 13](#) show the mechanical dimensions of the ARTIK 710 Module and the Bottom and Top View respectively.

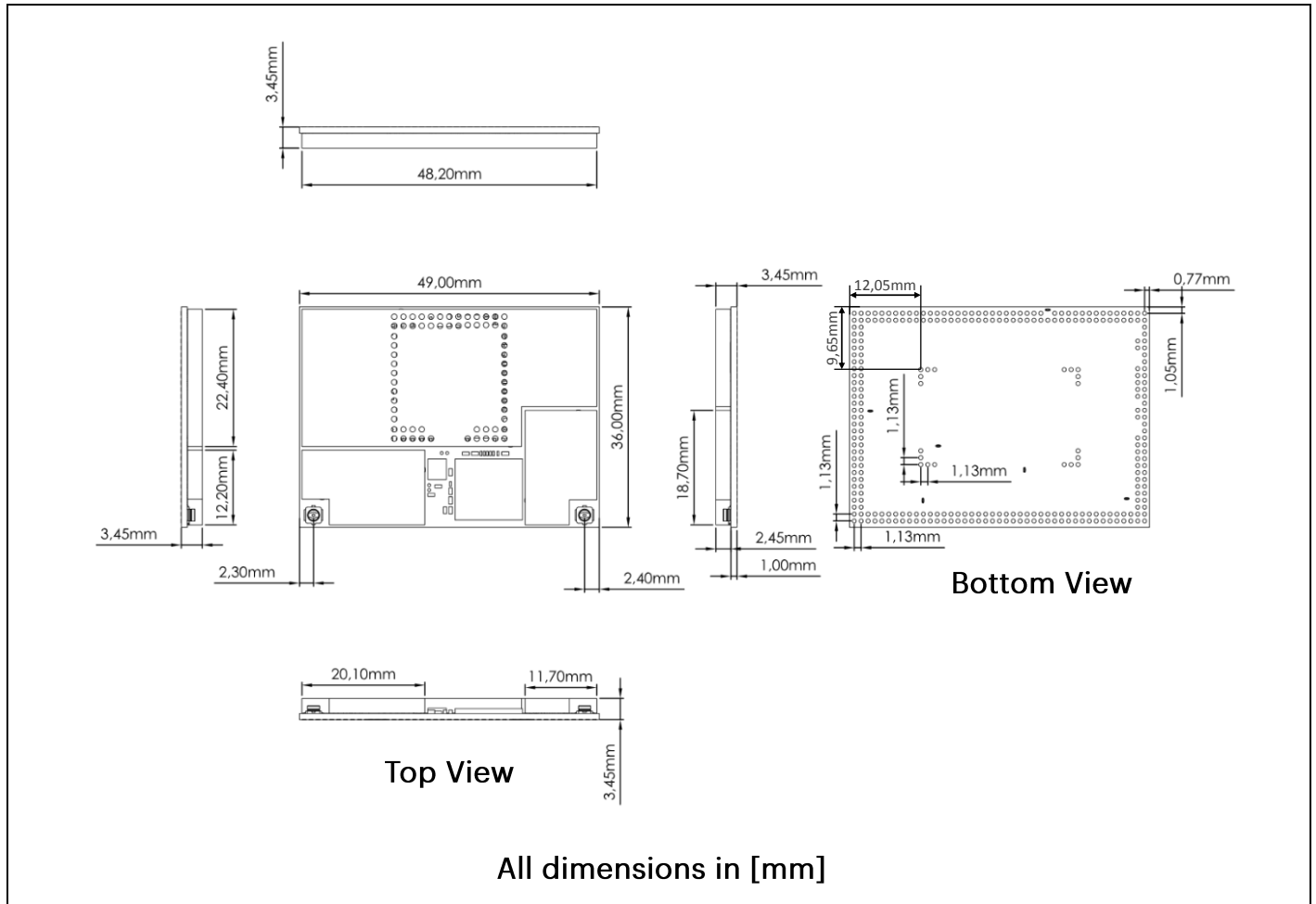


Figure 12. ARTIK 710 Module Mechanical Dimensions

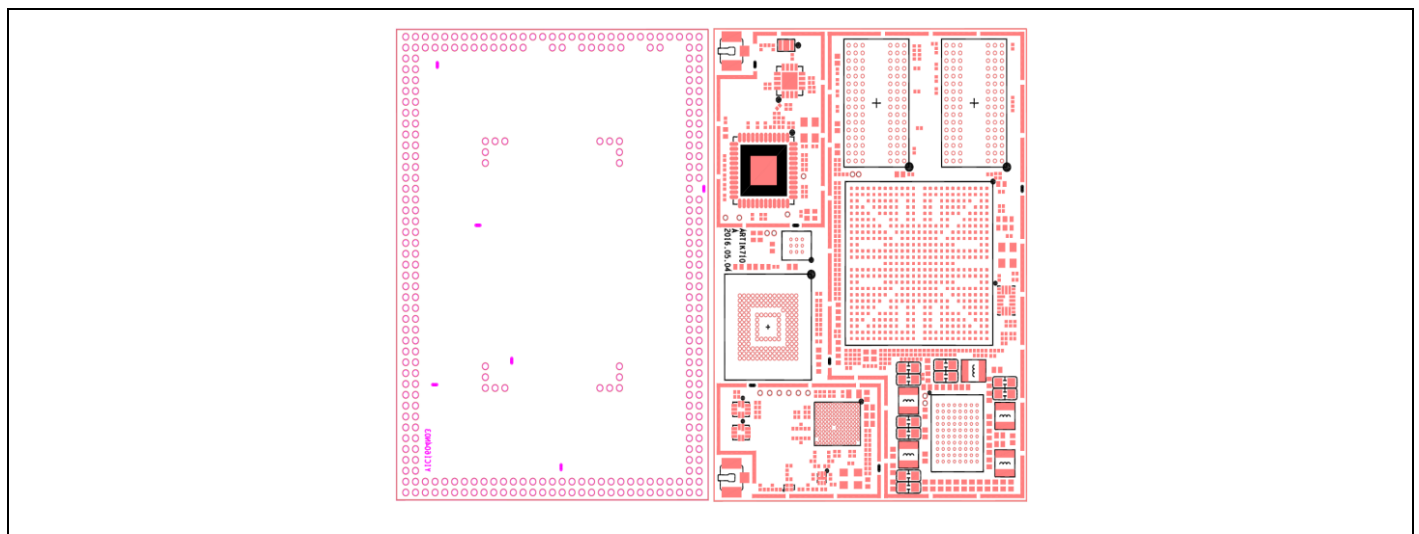


Figure 13. Mechanical Bottom View and Top View

All outer pin locations can be extracted from the mechanical dimensions provided in *Figure 12*. The inner pin locations on the PAD, positioned in an L-shaped form, as depicted in *Figure 14*, are located in *Table 64*. The locations given in the table are the absolute coordinates measured from the edge of the ARTIK 530 Module.

Table 64. L-Shaped Ball Locations

| Ball Name | Ball Number | Netlist Name | X-Location ↑ [mm] | Y-Location → [mm] |
|-----------|-------------|--------------|----------------------|----------------------|
| TP | 282 | GND | 26.35 | 12.05 |
| TP | 283 | GND | 26.35 | 13.18 |
| TP | 284 | GND | 26.35 | 14.31 |
| TP | 285 | GND | 26.35 | 35.49 |
| TP | 286 | GND | 26.35 | 36.62 |
| TP | 287 | GND | 26.35 | 37.75 |
| TP | 288 | GND | 25.22 | 37.75 |
| TP | 289 | GND | 24.09 | 37.75 |
| TP | 290 | GND | 13.11 | 37.75 |
| TP | 291 | GND | 11.98 | 37.75 |
| TP | 292 | GND | 10.85 | 37.75 |
| TP | 293 | GND | 10.85 | 36.62 |
| TP | 294 | GND | 10.85 | 35.49 |
| TP | 295 | GND | 10.85 | 14.31 |
| TP | 296 | GND | 10.85 | 13.18 |
| TP | 297 | GND | 10.85 | 12.05 |
| TP | 298 | GND | 11.98 | 12.05 |
| TP | 299 | GND | 13.11 | 12.05 |
| TP | 300 | GND | 24.09 | 12.05 |
| TP | 301 | GND | 25.22 | 12.05 |

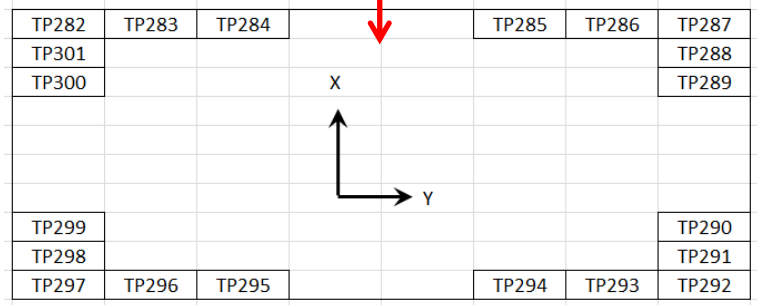
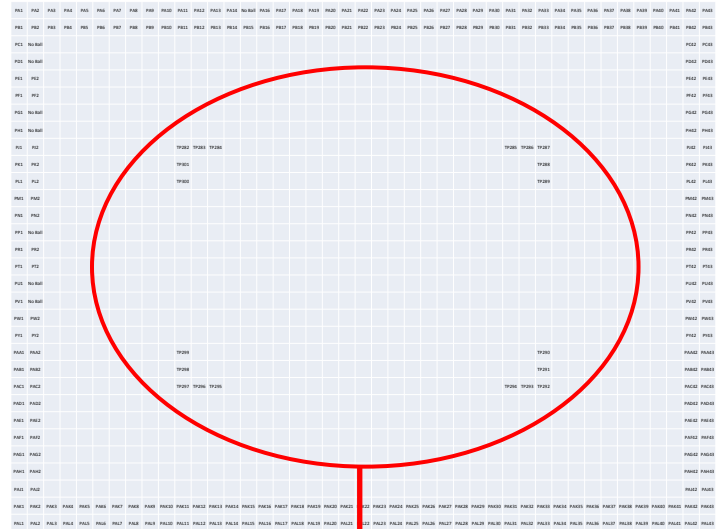


Figure 14. L-Shaped PAD Pins

ORDERING INFORMATION

| Type | Order Number | Description |
|---------------------------|---------------|--|
| ARTIK 710 Module | SIP007AFS001 | 1x ARTIK 710 Module |
| ARTIK 710 Development Kit | SIP-KITNXE001 | 1x ARTIK 710 Module 1x ARTIK 710 Interposer Board 1x Platform Board 1x Interface Board 2x Antennas (1x ZigBee, 1x Wi-Fi) |

For volume ordering of evaluation kits, please contact a sales representative in your area or email sales@artik.io.

LEGAL INFORMATION

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH THE SAMSUNG ARTIK™ DEVELOPMENT KIT AND ALL RELATED PRODUCTS, UPDATES, AND DOCUMENTATION (HEREINAFTER “SAMSUNG PRODUCTS”). NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. THE LICENSE AND OTHER TERMS AND CONDITIONS RELATED TO YOUR USE OF THE SAMSUNG PRODUCTS ARE GOVERNED EXCLUSIVELY BY THE SAMSUNG ARTIK™ DEVELOPER LICENSE AGREEMENT THAT YOU AGREED TO WHEN YOU REGISTERED AS A DEVELOPER TO RECEIVE THE SAMSUNG PRODUCTS. EXCEPT AS PROVIDED IN THE SAMSUNG ARTIK™ DEVELOPER LICENSE AGREEMENT, SAMSUNG ELECTRONICS CO., LTD. AND ITS AFFILIATES (COLLECTIVELY, “SAMSUNG”) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION CONSEQUENTIAL OR INCIDENTAL DAMAGES, AND SAMSUNG DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, ARISING OUT OF OR RELATED TO YOUR SALE, APPLICATION AND/OR USE OF SAMSUNG PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATED TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT.

SAMSUNG RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION, DOCUMENTATION AND SPECIFICATIONS WITHOUT NOTICE. THIS INCLUDES MAKING CHANGES TO THIS DOCUMENTATION AT ANY TIME WITHOUT PRIOR NOTICE. THIS DOCUMENTATION IS PROVIDED FOR REFERENCE PURPOSES ONLY, AND ALL INFORMATION DISCUSSED HEREIN IS PROVIDED ON AN “AS IS” BASIS, WITHOUT WARRANTIES OF ANY KIND. SAMSUNG ASSUMES NO RESPONSIBILITY FOR POSSIBLE ERRORS OR OMISSIONS, OR FOR ANY CONSEQUENCES FROM THE USE OF THE DOCUMENTATION CONTAINED HEREIN.

Samsung Products are not intended for use in medical, life support, critical care, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

This document and all information discussed herein remain the sole and exclusive property of Samsung. All brand names, trademarks and registered trademarks belong to their respective owners. For updates or additional information about Samsung ARTIK™, contact the Samsung ARTIK™ team via the Samsung ARTIK™ website at www.artik.io.

Copyright © 2016 Samsung Electronics Co., Ltd.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of Samsung Electronics.