National Semiconductor

DM74ALS240A/DM74ALS241A/74ALS240A-1/ DM64ALS240A Octal TRI-STATE® Bus Driver

General Description

These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers. The 'ALS240A control inputs symmetrically enable the respective outputs when set logic low, while the 'ALS241A has complementary enable gating. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

The 'ALS240-1 version features the same performance as the standard version with the addition of increased current drive capability to meet the current requirements of various bus architectures. For all ALS-1 products, the recommended maximum I_{OL} is increased to 48 mA.

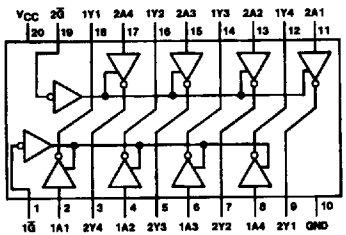
The DM64ALS240A version features the same performance as the standard version DM74ALS240A with a guarantee over an extended temperature range (−40°C to +85°C).

Features

- Maximum I_{OL} increased to 48 mA for 'ALS240A-1 product
- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current: 74ALS = 24 mA
- DM64ALS240A guarantee over extended temperature −40°C to +85°C

Connection Diagrams

Dual-In-Line Package



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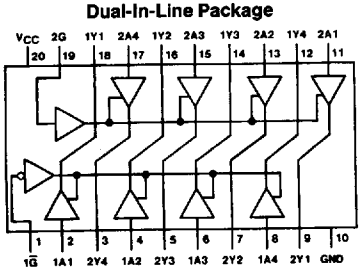
Top View

Order Number DM64ALS240AWM, DM64ALS240AN, DM74ALS240AWM, DM74ALS240AN, DM74ALS240ASJ, 74ALS240A-1N or 74ALS240A-1WM
See NS Package Number M20B, M20D or N20A

Dual-In-Line Package



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Top View

Order Number DM74ALS241AWM or DM74ALS241AN
See NS Package Number M20B or N20A

Function Tables

'ALS240A, 'ALS240A-1

Input		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

'ALS241A

Input		Output
2G	2A	Y
H	L	L
H	H	H
L	X	Z

'ALS241A

Input		Output
$1\overline{G}$	1A	Y
L	L	L
L	H	H
H	X	Z

H = High Level Logic State
L = Low Level Logic State
X = Don't Care (Either Low or High Level Logic State)
Z = High Impedance (Off) State

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Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM74ALS	0°C to +70°C
DM64ALS	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Typical θ_{JA}

N Package	60.5°C/W
M Package	79.8°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74ALS240A, 240A-1, 241A, DM64ALS240A			Units
			Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current	'ALS240A, 'ALS241A			24	mA
		'ALS240A-1			48	
T_A	Operating Free Air Temperature		0		70	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM74ALS240A, 240A-1, 241A, DM64ALS240A			Units
				Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			V
			I_{OH} = Max	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS240A, ALS240A-1 Outputs High			4	10	mA
		Outputs Low			13	23	mA
		Outputs TRI-STATE			14	25	mA
		V_{CC} = 5.5V, ALS241A Outputs High			9	15	mA
		Outputs Low			15	26	mA
		Outputs TRI-STATE			17	30	mA

'ALS240A and 240A-1 Switching Characteristics

over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM64ALS240A, DM74ALS240A, 74ALS240A-1		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$	Y	3	13	ns
t_{PZL}	Output Enable Time to Low Level Output				3	18	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$	Y	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	12	ns

'ALS241A Switching Characteristics

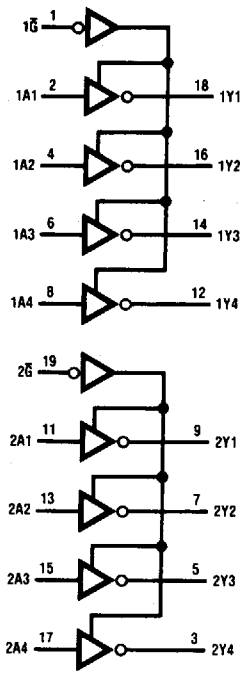
over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74ALS241A		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				3	10	ns
t_{PZH}	Output Enable Time to High Level Output		$1\overline{G}$	Y	3	21	ns
t_{PZL}	Output Enable Time to High Level Output				3	21	ns
t_{PHZ}	Output Disable Time to High Level Output		$1\overline{G}$	Y	2	10	ns
t_{PLZ}	Output Disable Time to Low Level Output				3	15	ns
t_{PZH}	Output Enable Time to High Level Output		2G	Y	7	21	ns
t_{PZL}	Output Enable Time to Low Level Output				7	21	ns
t_{PHZ}	Output Disable Time from High Level Output		2G	Y	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	15	ns

Note 1: See Section 5 for test waveforms and output load.

Logic Diagrams

ALS240A, ALS240A-1



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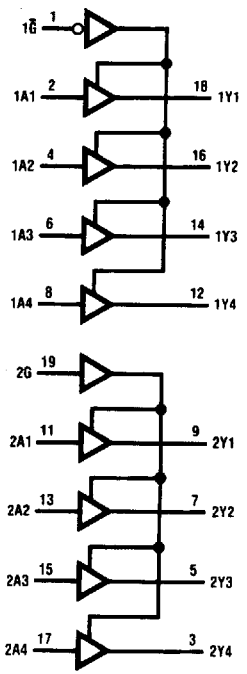
ALS241A



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