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SOLUTIONS

MAMWLExx

Low Power Radio Module with M4/M0+ Core.

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Index:

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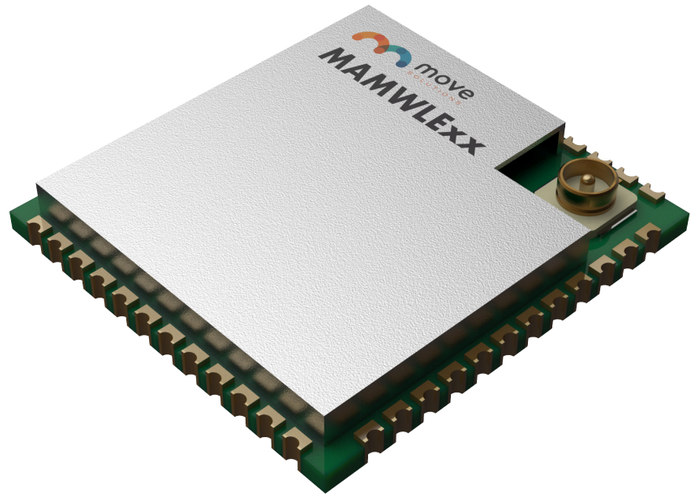
Low Power Radio Module with M4/M0+ Core.



1. FEATURES:

CORE: STM32WL

- Multiprotocol LPWAN 32-bit Arm®Cortex®-M4 MCUs, LoRa®, (G)FSK, (G)MSK, BPSK
- 128KB -256KB Flash, 48KB - 64KB SRAM
- Rich peripherals: ADC, DAC, DMA, Comparators, Timers, independent watchdog & many others
- Ultra-low power features

INTERFACES: 2xSPI, 3xI2C, 2xUSART, 1x LPUART, 1xJTAG, 1xSWDIO

SIZE: 16.5mm X 15.5mm X 2mm

CLOCK: 32MHz TCXO, 32.768KHz XTAL

TX POWER: low power path (up to +14 dBm) high power path (up to +22 dBm).

RF OUTPUT: Two assembly variants:

- 50 Ohm u.FL connector
- 50 Ohm pin

2. GENERAL DESCRIPTION:

MAMWLExx is a new low power radio module with a high-performance processing unit for the most complex task and high demanding applications.
The module comes with a great size of RAM and FLASH Memory which can be used for important computing calculations and to embed the biggest software applications. It even comes with a 64-bit unique identifier (DevEUI) in it, necessary to be compliant with LoRaWAN standard. Since the module is based on STM SoC, it can be programmed using ST environment itself, like STM32 Cubelde and STMCubeMX.

MAMWLExx module is designed to be easily integrated into any PCB offering two assembly variants. One with a U.FL coaxial connector on the top of the package that can be directly plugged into the antenna through a pigtail, saving space on the mainboard. The other variants, that outputs the RF signal on a 50 Ohm pin, fits you if you wish to create your own antenna design.
The module uses a high-performance ARM Cortex M4 32 Bits RISC core operating at 48 Mhz. The MAMWLExx has different types of low-power operation states, perfect for different applications especially the ones that need power saving.

MAMWLExx implements multiples radio modulations: LoRa, (G)FSK, (G)MSK, and BPSK with different options (Bandwidth, SF, Powers, CR) to meet different needs of communication. The module includes a 32MHz TCXO to drive the RF subsystem, and it is capable to output up to +22dbm. MAMWLExx comes with a rich pin-out to meet different needs. Pin-out is designed to use different peripherals at the same time using different protocols like I2C, SPI, LPUART, USART. The module has 12 multiplexed pins for a 12 bit (up to 16 bits) SAR ADC with DMA support, 12 bits DAC, 2 ultra-low-power comparator, multiple timers, and independent watchdog, JTAG and SWDIO debug capabilities. MAMWLExx has up to 32 I/O, most of them 5V-tolerant. The module implements a hardware encryption/decryption accelerator for different types of standards as AES (both 128 - 256 bits) and PKA for RSA, Diffie-Hellmann, or ECC (Elliptic Curve Cryptography) over GF(p) (Galois fields).

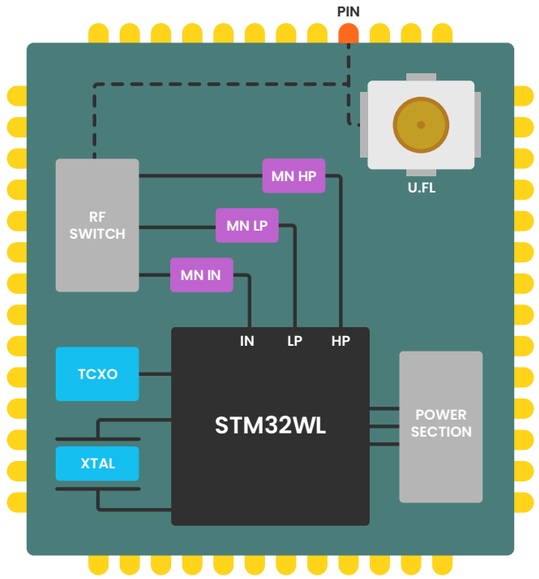
Applications:

- Smart meters,
- Supply chain,
- Building automation,
- Agricultural automation,
- Drone Control,
- GPS RTK,
- Smart cities,
- Retail Store sensors,
- Assets Tracking,
- Street Lights,
- Parking Sensors,
- Environmental Sensors,
- Healthcare Sensors,
- Remote control applications.

3. PART NUMBER:

RF Output	Part number
u.FL connector	MAMWLE-00
Pin 44	MAMWLE-01

4. BLOCK DIAGRAM:

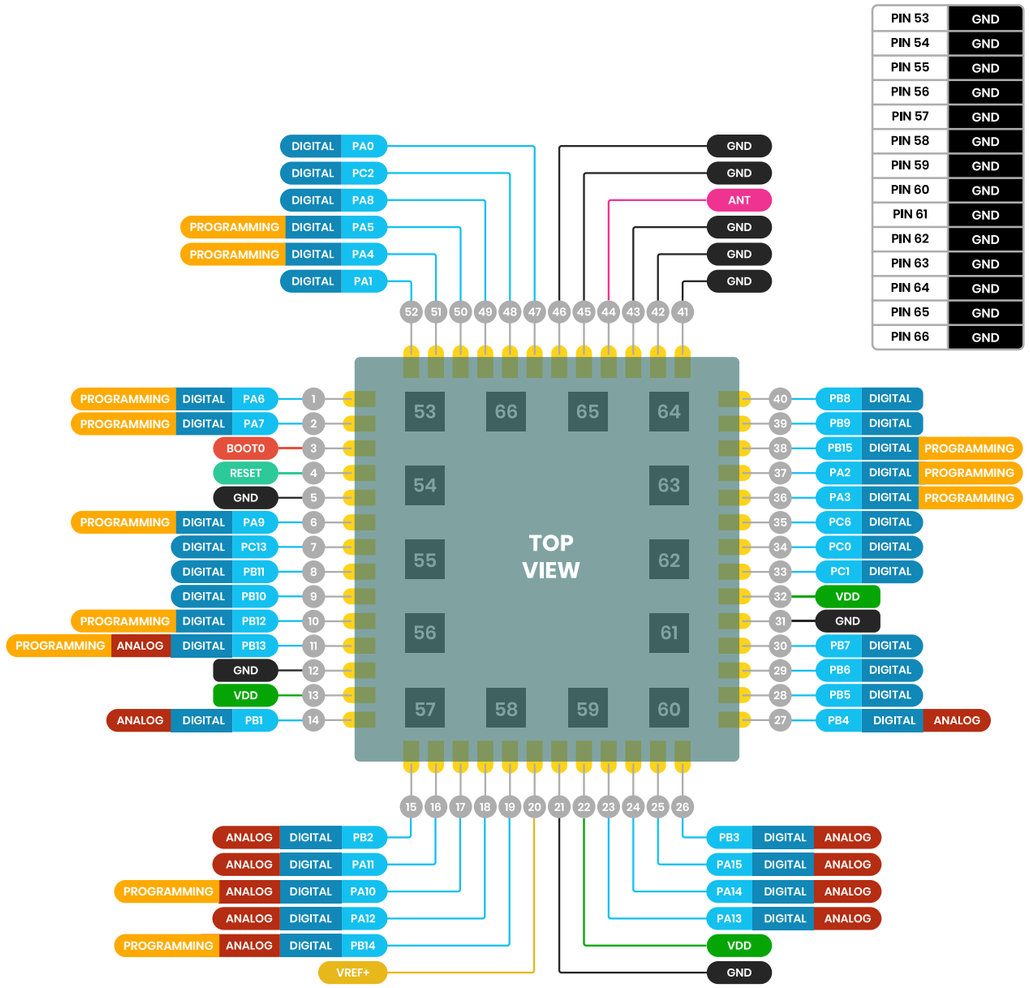


MN HP	Matching Network High Power Tx Path
MN LP	Matching Network Low Power Tx path
MN IN	Matching Network Rx path

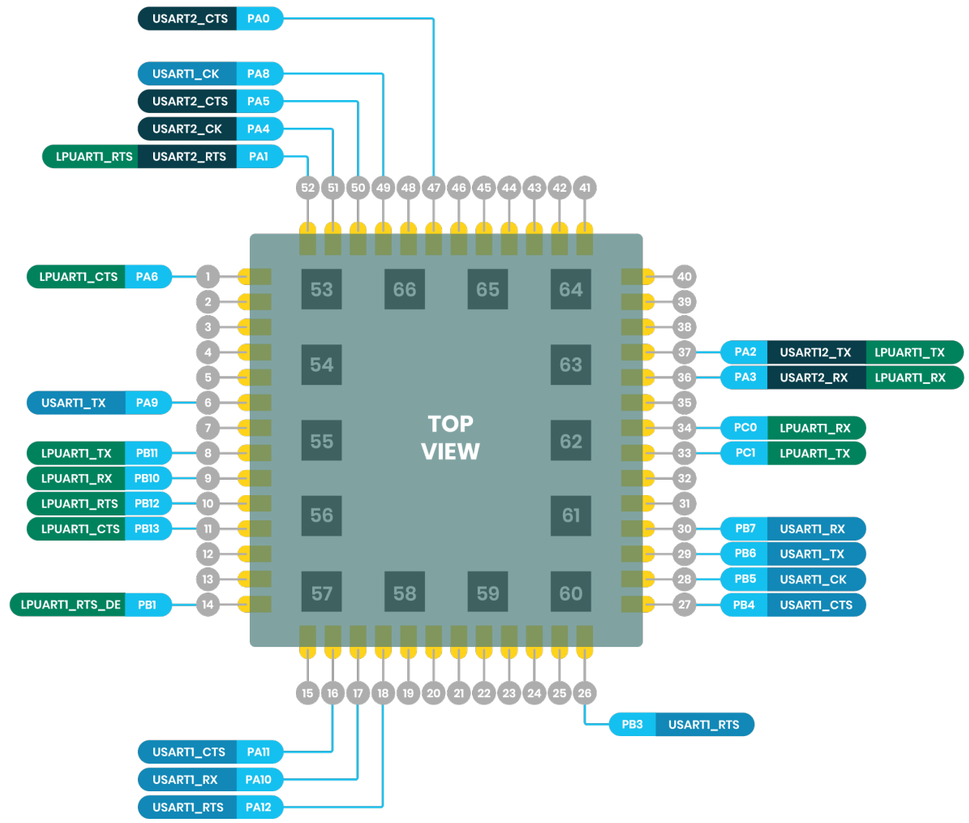
5. PIN - OUT

Main System Peripherals and GPIO

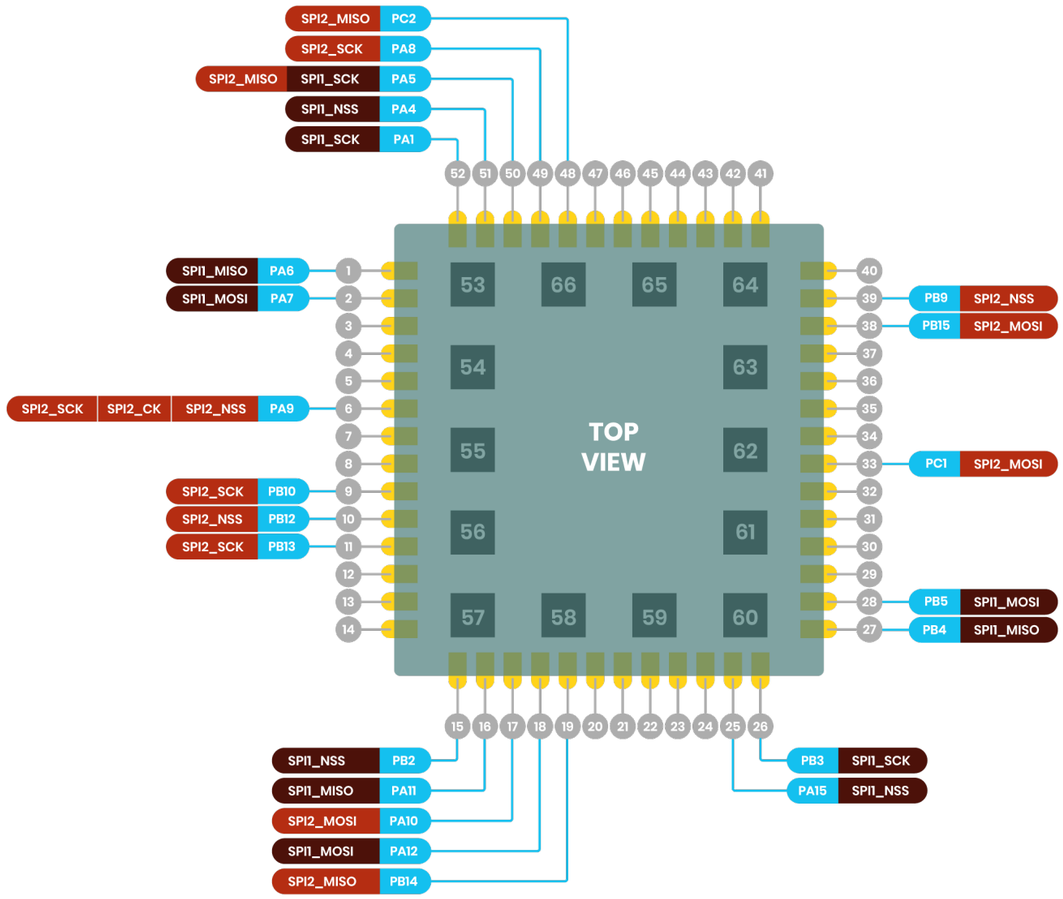
The size of MAMWLExx is about of 16,5 mm X 15,5 mm LGA and comes with a 66 pin out to bring all the functionality and rich peripherals of the STM32WLEx.
It has multiples interfaces availables:



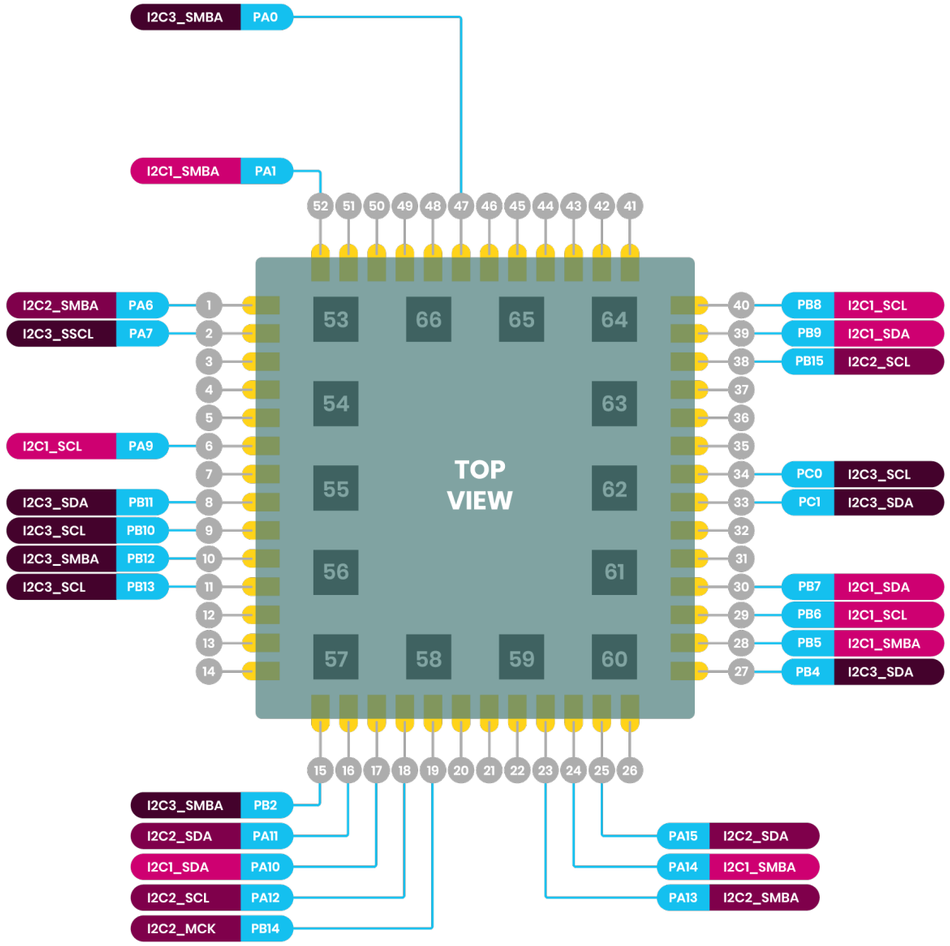
Pin-out: USART1/USART2



Pin-out: SPI1/SPI2



Pin-out: I2C1/I2C2/I2C3



Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2 TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	-	USART1/ USART2
Port A	PA0	-	TIM2_CH1	-	-	I2C3_SMBA	I2S_CKIN	-	USART2_CTS
	PA1	-	TIM2_CH2	-	LPTIM3_OUT	I2C1_SMBA	SPI1_SCK	-	USART2_RTS
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	I2S2_MCK	-	USART2_RX
	PA4	RTC_OUT2	LPTIM1_OUT	-	-	-	SPI1_NSS	-	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	SPI2_MISO	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI1_MISO	-	-
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	SPI2_SCK/ I2S2_Ck	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_NSS/ I2S2_WS	I2C1_SCL	SPI2_SCK/ I2S2_Ck	-	USART1_TX
	PA10	TIM1_CH3	TIM1_CH3	-	-	I2C1_SDA	SPI2_MOSI/ I2S2_SD	-	USART1_RX
	PA11	TIM1_CH4	TIM1_CH4	TIM1_BKIN2	LPTIM3_ETR	I2C2_SDA	SPI1_MISO	-	USART1_CTS

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	-	-	-	COMP1/ COMP2/ TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port A	PA0	-	-	-	-	COMP1_OUT	-	TIM2_ETR	CM4_EVENTOUT
	PA1	LPUART1_RTS	-	-	-	-	-	-	CM4_EVENTOUT
	PA2	LPUART1_TX	-	-	-	COMP2_OUT	-	-	CM4_EVENTOUT
	PA3	LPUART1_RX	-	-	-	-	-	-	CM4_EVENTOUT
	PA4	-	-	-	-	-	-	LPTIM2_OUT	CM4_EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	CM4_EVENTOUT
	PA6	LPUART1_CTS	-	-	-	TIM1_BKIN	-	TIM16_CH1	CM4_EVENTOUT
	PA7	-	-	-	-	COMP2_OUT	-	TIM17_CH1	CM4_EVENTOUT
	PA8	-	-	-	-	-	-	LPTIM2_OUT	CM4_EVENTOUT
	PA9	-	-	-	-	-	-	-	CM4_EVENTOUT
	PA10	-	-	-	-	-	-	TIM17_BKIN	CM4_EVENTOUT
	PA11	-	-	-	-	TIM1_BKIN2	-	-	CM4_EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_ AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2 TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	-	USART1/ USART2
Port A (continued)	PA12	-	TIM1_ ETR	-	LPTIM3_ IN	I2C2_ SCL	SPI1_ MOSI	-	USART1_ RST
	PA13	JTMS-SWDIO	-	-	-	I2C2_ SMBA	-	-	-
	PA14	JTCK-SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-	I2C1_ SDA	SPI1_ NSS	-	-
Port B	PB0	VDD_TCXO[1]							
	PB1	-	-	-	-	-	-	-	-
	PB2	-	LPTIM1_ OUT	-	-	I2C3_ SMBA	SPI1_ NSS	-	-
	PB3	JTDO-TRACE SWO	TIM2_ CH2	-	-	-	SPI1_ SCK	-	USART1_ RTS
	PB4	NJTRST	-	-	-	I2C3_ SDA	SPI1_ MISO	-	USART1_ CTS
	PB5	-	LPTIM1_ IN1	-	-	I2C1_ SMBA	SPI1_ MOSI	-	USART1_ CK
	PB6	-	TIM1_ ETR	-	-	I2C1_ SCL	-	-	USART1_ TX
	PB7	-	TIM1_ IN2	-	TIM1_ BKIN	I2C1_ SDA	-	-	USART1_ RX
	PB8	-	TIM1_ CH2N	-	-	I2C1_ SCL	-	-	-
	PB9	-	TIM2_ CH3N	-	-	I2C1_ SDA	-	-	-

1. Internally connected. Not available as output Pin.

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	-	-	-	COMP1/ COMP2/ TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port A (continued)	PA12	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA13	IR_ OUT	-	-	-	-	-	-	CM4_ EVENTOUT
	PA14	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA15	-	-	-	-	-	-	-	CM4_ EVENTOUT
Port B	PB0	VDD_TCXO[1]							
	PB1	LPUART_1 RTS_DE	-	-	-	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PB2	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PB3	-	-	-	-	-	-	-	CM4_ EVENTOUT
	P4	-	-	-	-	-	-	TIM17_ BKIN	CM4_ EVENTOUT
	PB5	-	-	-	-	-	-	TIM16_ BKIN	CM4_ EVENTOUT
	PB6	-	-	-	-	-	-	TIM16_ CH1N	CM4_ EVENTOUT
	PB7	-	-	-	-	-	-	TIM17_ CH1N	CM4_ EVENTOUT
	PB8	-	-	-	-	-	-	TIM16_ CH1	CM4_ EVENTOUT
	PB9	IR_ OUT	-	-	-	-	-	TIM17_ CH1	CM4_ EVENTOUT

1. Internally connected. Not available as output Pin.

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2 TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	-	USART1/ USART2
Port B (continued)	PB10	-	TIM2_ CH3	-	-	I2C1_ SCL	-	-	-
	PB11	-	TIM2_ CH4	-	-	I2C3_ SDA	-	-	-
	PA12	-	TIM1_ BKIN	-	TIM1_ BKIN	I2C1_ SMBA	SPI2_ NSS/ I2S2_WS	-	-
	PA13	-	TIM2_ CH1N	-	-	I2C1_ SCL	SPI2_ SCK/ I2S2_CK	-	-
	PB14	-	TIM2_ CH2N	-	I2S2_ MCK	I2C1_ SDA	SPI2_ MISO	-	-
	PB15	-	TIM2_ CH2N	-	-	I2C2_ SCL	SPI2_ MOSI/ I2S2_SD	-	-

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF5
		LPUART1	-	-	-	COMP1/ COMP2/ TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port B (continued)	PB10	LPUART1_ RX	-	-	-	COMP1_ OUT	-	-	CM4_ EVENTOUT
	PB11	LPUART1_ TX	-	-	-	COMP2_ OUT	-	-	CM4_ EVENTOUT
	PA12	LPUART1_ RTS	-	-	-	-	-	-	CM4_ EVENTOUT
	PA13	LPUART1_ CTS	-	-	-	-	-	-	CM4_ EVENTOUT
	PB14	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PB15	-	-	-	-	-	-	-	CM4_ EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2 TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	-	USART1/ USART2
Port C	PC0	-	LPTIM1_ IN1	-	-	I2C3_ SCL	SPI1_ MOSI	-	-
	PC1	-	LPTIM1_ OUT	-	SPI2_ MOSI/ I2S2_SD	I2C3_ SDA	-	-	-
	PC2	-	LPTIM1_ IN2	-	-	-	-	-	-
	PC3	FECNTRL3[1]							
	PC4	FECNTRL1[1]							
	PC5	FECNTRL2[1]							
	PC6	-	-	-	-	I2S2_ MCK	SPI1_ NSS	-	-
	PC13	RTC_ OUT1, RTC_ TS	-	-	-	-	SPI1_ SCK	-	-
	PH3	-	-	-	-	-	-	-	-

1. Internally connected. Not available as output Pin.

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	-	-	-	COMP1/ COMP2/ TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_ RX	-	-	-	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PC1	LPUART_ TX	-	-	-	-	-	-	CM4_ EVENTOUT
	PC2	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC3	FECNTRL3[1]							
	PC4	FECNTRL1[1]							
	PC5	FECNTRL2[1]							
	PC6	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC13	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PH3	-	-	-	-	-	-	-	CM4_ EVENTOUT

1. Internally connected. Not available as output Pin.

Interface	Quantity
I2C	3
SPI	2
U(S)ART	2
LPUART	1

With a number of 36 I/O that includes:

Task	Quantity (Pin out)
Digital Pin	up to 36 pins
ADC	12 pins
VREF+	1 pin
Comparators	2 pins
DAC	1 pin

GPIO can have different operations states for output and input operation as:

1) Output States: Push-Pull or Open drain + pull-up/down
2) Input States: Floating, pull-up/down, analog

Most of pins are 5V tolerant.

The module has also different system peripheral to achieve great performances such as:

System Peripheral
2x DMA controllers
Timers and Low Power Timer
RTC with 32-bit sub-second-wakeup counter
Independent watchdog, Window watchdog
Hardware Encryption/Decryption accelerator

6. MAX RATING AND EXTERNAL CHARACTERISTICS

Operating Characteristics

Parameter	Minimum	Typical	Maximum	
Temperature	-40		+85	°C
Supply Voltage (VDD)	3,0	3,3	3,6	V
Supply Voltage (VREF+)	2,0	-	VDD	V
Frequency Band	868		915	Mhz
TCXO		32		Mhz
XTAL		32,768		Khz
Power consumption[1-2] (shutdown mode)		31	150	nA
Power consumption[1-2] (standby mode)		0,255	0,710	uA
Power consuption[1-2] (Stop 2)		0,885	2,60	uA
Power consuption[1-2] (Stop 1)		4,20	20	uA
Power consuption[1-2] (Stop 0)		400	570	uA
Power consumption[1-2] (Sleep mode 48 Mhz)		1,70	2,10	mA
Power consumption[1-2] (Run mode 48 Mhz)		5,55	7,40	mA

1. The effettive power consumption depends on: temperature; supply voltage; clock settings.
2. Given consuptions are for VDD = 3V; T = +25°C.

Absolute Characteristics

Parameter	Minimum	Typical	Maximum	
Temperature	-40		+85	°C
Supply Voltage (VDD)	-0,3		3,6	V
Supply Voltage (VREF+)	-0,3		3,6	V

RF Characteristics

Parameter	Minimum	Typical	Maximum	
Output RF level (Low PA)			+14	dBm
Output RF level (High PA)			+22	dBm
Power consumption (PA=+10dBm)[1]	15		20	mA
Power consumption (PA=+14dBm)[1]			26	mA
Power consumption (PA=+20dBm)[1]	87		106	mA
Power consumption (PA=+22dBm)[1]			120	mA
Sensitivity (868Mhz, BW=125Khz SF=12)		-135,4		dBm
Sensitivity (868Mhz, BW=125Khz SF=7)		-124,2		dBm
Sensitivity (868Mhz, BW=500Khz SF=12)		-129,6		dBm
Sensitivity (868Mhz, BW=500Khz SF=7)		-116,2		dBm
Sensitivity (915Mhz, BW=125Khz SF=12)		-135,6		dBm
Sensitivity (915Mhz, BW=125Khz SF=7)		-122,4		dBm
Sensitivity (915Mhz, BW=500Khz SF=12)		-127,9		dBm
Sensitivity (915Mhz, BW=500Khz SF=7)		-115,1		dBm

1. VDD = 3,3 V

Radio

The Sub-Ghz Radio is a low power radio with a high quality matching filter for operate in the band of 868 Mhz and 915 Mhz. It can use different modulation techniques such as:

Modulation	Mode
LoRa	TX/RX
(G)FSK	TX/RX
(G)MSK	TX/RX
(D)BPSK	Only TX

The radio is compliant for LoRaWAN specification and for different radio regulations ETSI EN 300 220, EN 300 113, EN 301 166, FCC CFR 47 part 15, 24, 90, 101 and the ARIB STD-T30, T-67, T-108.

The Sub-Ghz Radio is equipped with two high performance power amplifier to transmit up to +22dBm and power can be programmed with a step of 1 dB within 32 steps. A high quality TCXO 32 Mhz guarantees great stability during transmission.
LoRa modulation can operate with different bandwidth:

0	1	2	3	4	5	6	7	8	9	Code
7,81	10,42	15,63	20,83	31,25	41,67	62,5	125	250	500	BW[KHZ]

And with different Spreading Factors (from 5 to 12).
It can be set in multiple differents mode of operations for LoRa Packet (Explicit/Implicit Header Mode) choosing also different coding rates:

0	1	2	3	4	CR Settings
4/4	4/5	4/6	4/7	4/8	Coding Rate

The radio is completely programmable to achieve the best performances needs for different kind of application.
MAMWLExx comes with two different option:

1) 50 Ohm u.FL connector
2) 50 Ohm RF pin

The u.FL connector is already applied on the top of the module with a high performance Pi Filter, so there is no need to design any RF circuit to implement the module. To give the best flexibility to the designer MAMWLExx implements a 50 Ohm pin antenna to enhance a complete custom antenna design.
The module can implement Over-The-Air Firmware updates.

7. HOW TO PROGRAM & DEBUG THE MAMWLEXX

HOW TO DEVELOP WITH MAMWLEXX

The MAMWLExx is compatible with all the software development environment that works for the STM32 microcontroller series (e.g. STM32CubeIDE, Keil uVision, IAR Embedded).
The RF switch that selects the Tx/Rx path of the module is controlled by the STM32WL by three GPIOs. Those GPIOs (PC3, PC4, PC5) aren't output in the MAMWLExx footprint, but must be driven in the firmware to use the RF part as desired (see tab). Same thing applies to pin PB0 of the STM32WL that is connected (internally to the module) at the TCXO alimentation. TCXO must be ON when using the RF part and can be OFF the rest of the time reducing the overall consumption.
This choice of control pins for the RF switch and the TCXO is the same as ST Microelectronics. In this way the user can run without further modification the code examples that comes within the firmware packages released by ST for the STM32WL series.
Those example in the firmware packages are also the best way to start a new project with the MAMWLExx.

RF front-end configuration	PC4	PC5	PC3
TX high output power	Low	High	High
TX low output power	High	High	High
RX	High	Low	High
Power-down	Low	Low	Low

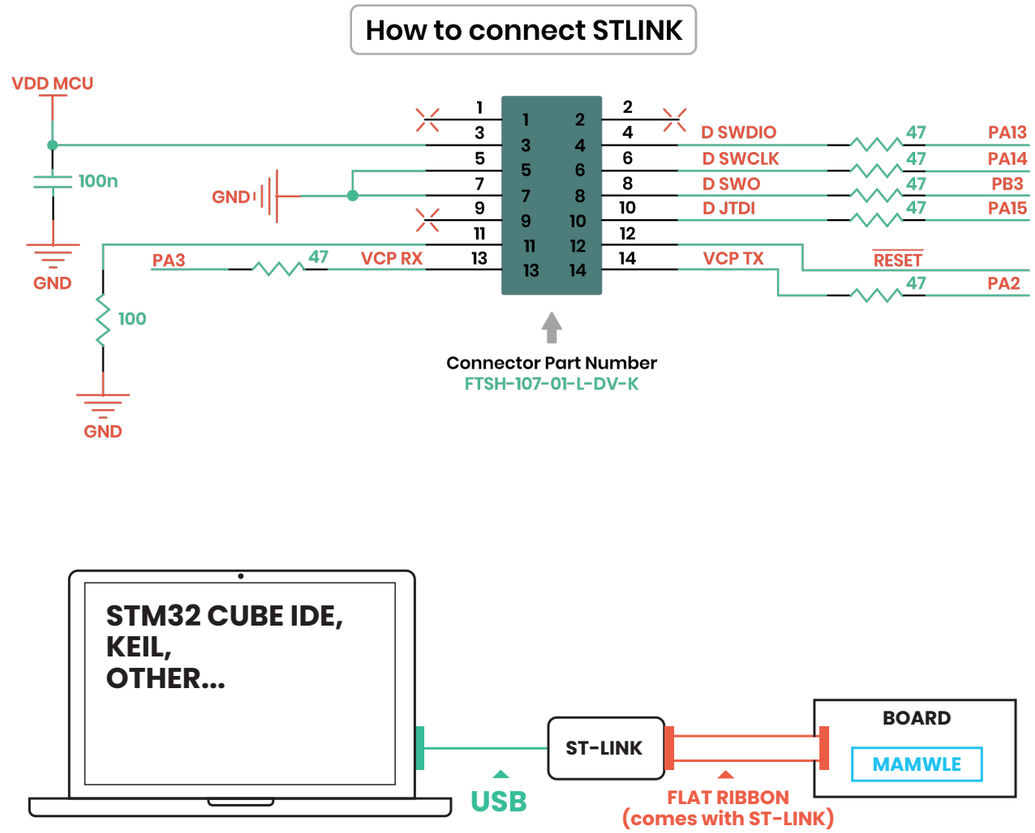
HOW TO PROGRAM & DEBUG

There are many way to program and debug the MAMWLExx. The MAMWLExx comes with an internal bootloader that support boot from SPI and USART, in addition the module can also be programmed and debugged via the JTAG/SWD interface.
The best way to access those interfaces for programming is through the ST-LINK V3 debugger/programmer for STM32 micro series. The ST-link act like a bridge between the board and the PC. It communicates with the PC via a microB-USB cable and has many headers for connecting with various subsets of the SPI/USART/JTAG/SWD intefaces of the module. If you would like to program using SPI or USART see **AN2606** from ST first because there are some details that you must pay attention of. For example if you would like to

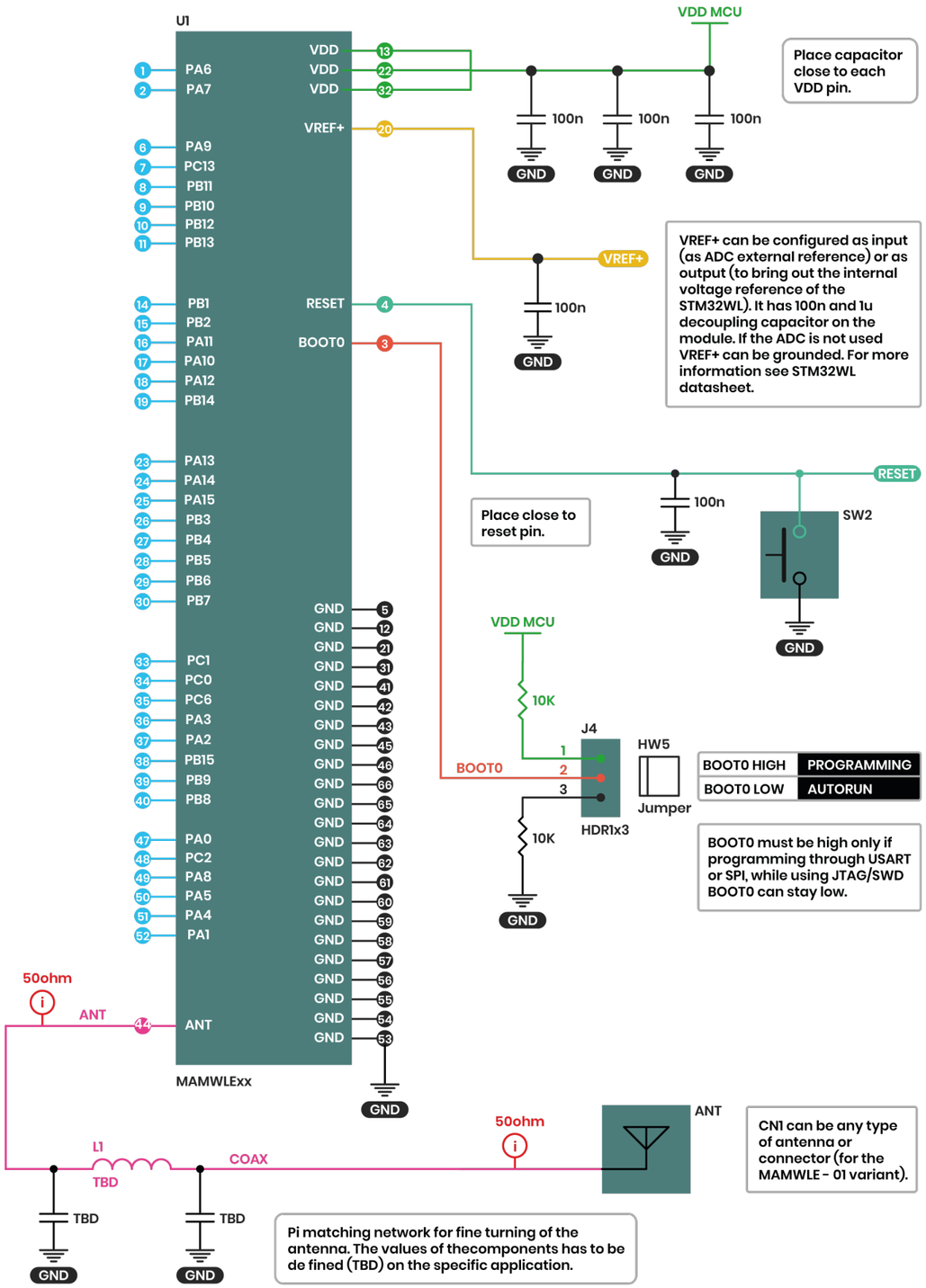
boot from USART1 only pin PA9, PA10 (and not on all pins that support USART1) are fine.
Among all the possible ST-link V3 headers, below we indicate an easy way of connection that suits either programming and debugging. For further information on other ST-link possibility please see the **UM2448** user manual from ST.

USING HEADER CN1 OF ST-LINK:

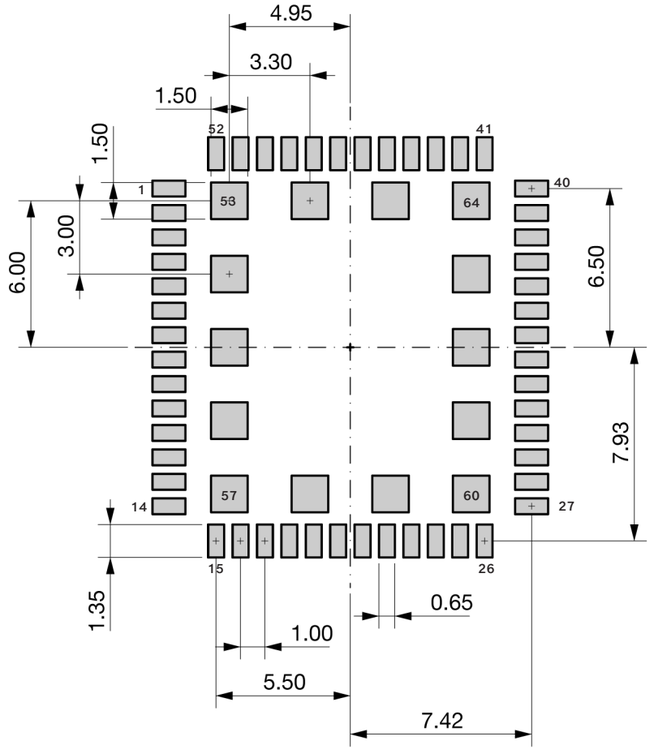
CN1 support the SWD/JTAG interface for programming and debugging the application and provides a virtual com port (COM or VCP) that make simple printing string in a serial terminal. To be able to connect the board to CN1, the board should have a twin header of CN1 connected to the module like shown in the figure. While programming through CN1 is not necessary to connect BOOT0 to VCC.



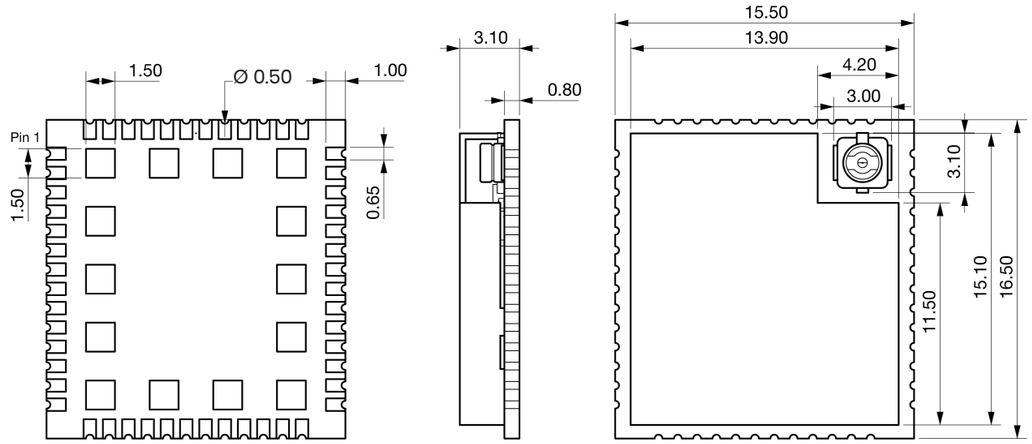
8. REFERENCE SCHEMATIC



9. RECOMMENDED FOOTPRINT



SIZE AND DIMENSIONS



Botton view Right view Top view

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