



In collaboration with



ENA303 ARTIC R2 User Datasheet

For use with Argos 2/3/4

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Contact: info@kineis.com

Table of Contents

Revision historyiv

Referencesiv

Glossaryv

1. Device Information7

 1.1 Pad Assignments 7

 1.2 Pin Descriptions 8

 1.3 Package dimensions 9

 1.4 Storage..... 10

 1.5 Soldering 10

 1.6 Typical usage 11

2. Electrical Characteristics..... 12

 2.1 Absolute Maximum Ratings..... 12

 2.2 Electrical Characteristics 12

 2.3 SPI Interface 14

 2.4 ARTIC Memories 17

 2.5 Boot configuration 18

 2.6 Bias 18

 2.7 Reset 18

 2.8 GPIO 18

 2.9 Flash interface..... 18

 2.10 TCXO interface 18

3. Operating the device 19

 3.1 Start-up sequence..... 19

 3.2 Firmware status – interrupt flags 21

 3.3 MCU commands 22

 3.4 Memory locations 27

 3.5 Transmission..... 28

 3.6 Reception 32

 3.7 CRC Check 35

 3.8 Firmware version..... 35

 3.9 TCXO control feature 36

 3.10 GPIO 36

 3.11 Power consumption..... 37

 3.12 Timing transmission and receiving 38

 3.13 Packet timing..... 38

3.14	Examples	40
4.	Layout considerations	42
4.1	PCB buildup	42
4.2	TCXO	42
4.3	Receiver	42

Preliminary

Revision history

V	Date	Sections concerned	Info
1v0	2016-10-25	all	first version
1v1	2017-03-02	1.3	Added Package dimensions
1v2	2017-08-02	3.1,3.5,3.6,3.11	Startup time, Transmit frequency, Satellite detection flag, current consumption.
1v3	2017-12-01	1	Added storage and soldering information
1v4	2018-03-16	1.3,4	Added typical usage, layout guidelines
1v5	2018-04-24	1	Added build of material
1v6	2018-06-04	3.5.3,	Transmission bands
1v7	2019-10-15	1.4	Storage conditions adapted
1v8	2019-10-23	3.9	TCXO control feature extended
1v9	2019-12-20	1.6	Added Reference to ARTIC_evaluation_board
1v10	2020-01-16	3.12, 3.13	Added transmission, receiving and packet timing

References

AD1 Platform Transmitter Terminal (PTT-A2), Platform Message Transceiver (PMT-A2) - Physical Layer System Requirements. - 19/01/2016. - Vol. v5.0.

AD2 Platform Transmitter Terminal (PTT-A3, including PTT-ZE), Platform Message Transceiver (PMT-A3) - Physical Layer System Requirements. - 19/01/2016. - Vol. v5.0.

AD3 Platform Transmitter Terminal (PTT-HD A3), Platform Message Transceiver (PMT-HD A3) - Physical Layer System Requirements. - 19/01/2016. - Vol. v5.0.

AD4 Very Low Data Rate Platform Transmitter Terminal for ARGOSs 4 (PTT-VLD-A4) - Physical Layer System Requirements. - 19/01/2016. - Vol. v2.0.

AD5 High Data Rate Platform Transmitter Terminal For ARGOS 4 (PTT/PMT-HD-A4) - Physical Layer System Requirements. - 19/01/2016. - Vol. v2.0.

AD6 Receiver Terminal for ARGOS 3 – Physical Layer System Requirements. - 19/01/2016. - Vol. v3.0.

AD7 Receiver Terminal for ARGOS 4 – Physical Layer System Requirements. - 19/01/2016. - Vol. v1.6.

AD8 Services and Message Formats, General Specifications. - 21/03/2019. - Vol. v1.6.

AD9 Certification of PTT and PMT. - 28/08/2006. - Vol. v2.0.

AnSem ARTIC_evaluation_board_1v4, [Report]. - 20/12/2019.

Glossary

ACK	Acknowledge
ADC	Analog-to-Digital Converter
ARGOS	Advanced Research and Global Observation Satellite
ASCII	American Standard Code for Information Interchange
bps	Bits per second
BPSK	Binary Phase-Shift Keying
C/S @	Spacecraft address
CNES	Centre National d'Etudes Spatiales
COSPAS-SARSAT	Cosmitscheskaja Sistema Poiska Awarinitsch Sudow - Search And Rescue Satellite Aided Tracking
CRC	Cyclic Redundancy Check
DSP	Digital Signal Processor
DSSS	Direct Sequence Spread Spectrum
FCS	Frame Check Sequence
GMSK	Gaussian Minimum Shift Keying
GND	Ground connection
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPS	Global Positional System
HAD	High Definition Audio
HD	High data rate
INT1, INT2	Interrupt lines
LSB	Least Significant Bit
LSBit	Least Significant Byte
LUT	LookUp Table
MCU	Microcontroller Unit
MISO	Master In Slave Out (Serial Peripheral Interface)
MOSI	Master Out Slave In (Serial Peripheral Interface)
MSB	Most Significant Byte
MSBit	Most Significant Bit
MSL	Moisture Sensitivity Level
NACK	Negative Acknowledge
NMEA	National Marine Electronics Association
OQPSK	Offset Quadrature Phase Shift Keying
OTP	One Time Programmable memory
PA	Power Amplifier
PCB	Printed Circuit Board
PMT	Platform Message Transceiver
PTT	Platform Transmitter Terminal
QFN	Quad Flat No-leads package
QPSK	Quadrature Phase-Shift Keying
RS-232	Recommended Standard 232 in telecommunications
RX	Receiver
RXIN	Receiver input signal
SCLK	Serial Clock
SPI	Serial Peripheral Interface
SSB	Single Side Band
SSN	Slave Select Not
TCXO	Temperature Compensated Xtal Oscillator
TTL	Transistor-Transistor Logic
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
VLD	Very low datarate

General description

The ARTIC is an integrated low power small size ARGOS 2/3/4 single chip radio. ARTIC implements a message based wireless interface. For satellite uplink communication, ARTIC will encode, modulate and transmit provided user messages. For downlink communication, ARTIC will lock to the downstream, demodulate and decode and extract the satellite messages.

The ARTIC can transmit signals in frequency bands around 400MHz and receive signals in the bands around 466MHz, in accordance with the ARGOS satellite system specifications.

The ARTIC is compliant and certified for all ARGOS 2 and ARGOS 3 TX standards. It contains a RF transceiver, a frequency synthesiser and a digital baseband modem. The ARTIC contains an on-chip power amplifier delivering 1mW [0dBm] output power, that serves as an output for connecting an external high efficient PA. The (de)modulation algorithms run on an on-chip DSP. This software approach allows for retargeting the ARTIC for other applications. The DSP program can be retained on an external flash or the MCU.

Internal power management is autonomously handled by ARTIC in order to optimize its current consumption.

The ARTIC can communicate with an external micro-controller using a standard SPI interface.

The ARTIC chip is a QFN48, 7mm x 7mm, 0.5mm pitch.

Features

- Serial interface (SPI) for communication with MCU
- Programmable DSP core on board to ensure flexibility
- RX frequency : 466MHz - TX frequency: 400MHz
- Fractional N frequency synthesis
- Supported TX standards:
 - BPSK: PTT-A2 (ARGOS 2), PTT-VLD (ARGOS 4), COSPAS-SARSAT 1e Gen¹.
 - QPSK: PTT-A3, PTT-ZE (ARGOS 3).
 - GMSK: PTT-HD (ARGOS3), PTT-MD (ARGOS4), PTT-HD (ARGOS4)
- Supported RX standards:
 - QPSK: PMT-A3 (ARGOS 3)
 - DSSS OQPSK: PMT-A4 (ARGOS 4)
- Dedicated flash Interface to retain Firmware.
- Support COSPAS-SARSAT standard
- Operates on external 26MHz reference clock
- Dual supply, 1.8V and 3.3V
- Integrated PA (0dBm) to combine with external PA

Applications

- Pop up tags for animal tracking
- Buoys and floats, Maritime security
- Satellite-based vessel monitoring system (VMS)
- Tracking of adventurers and yacht racing
- Search and rescue (COSPAS-SARSAT)

Functional Block Diagram

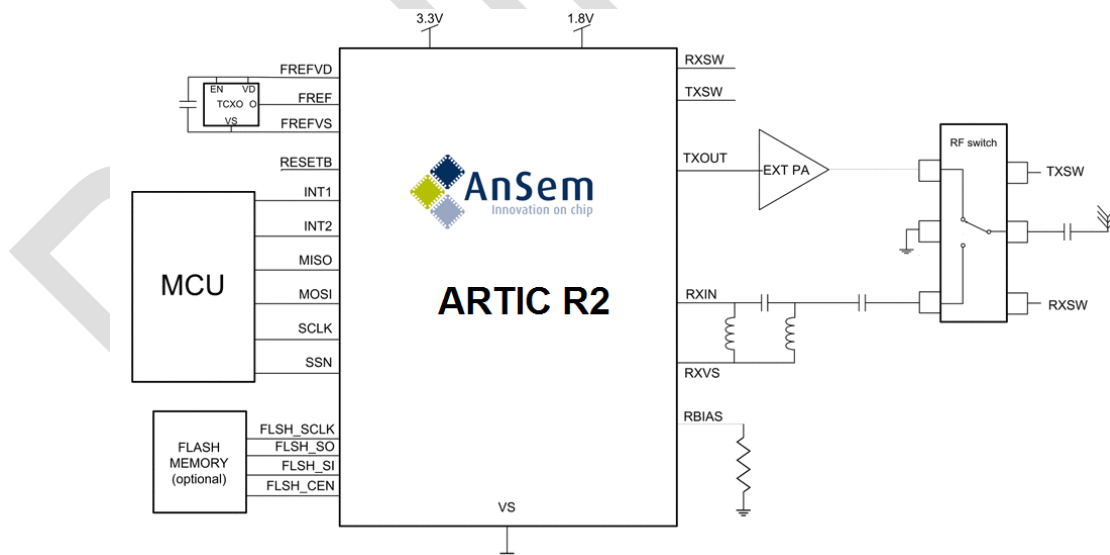


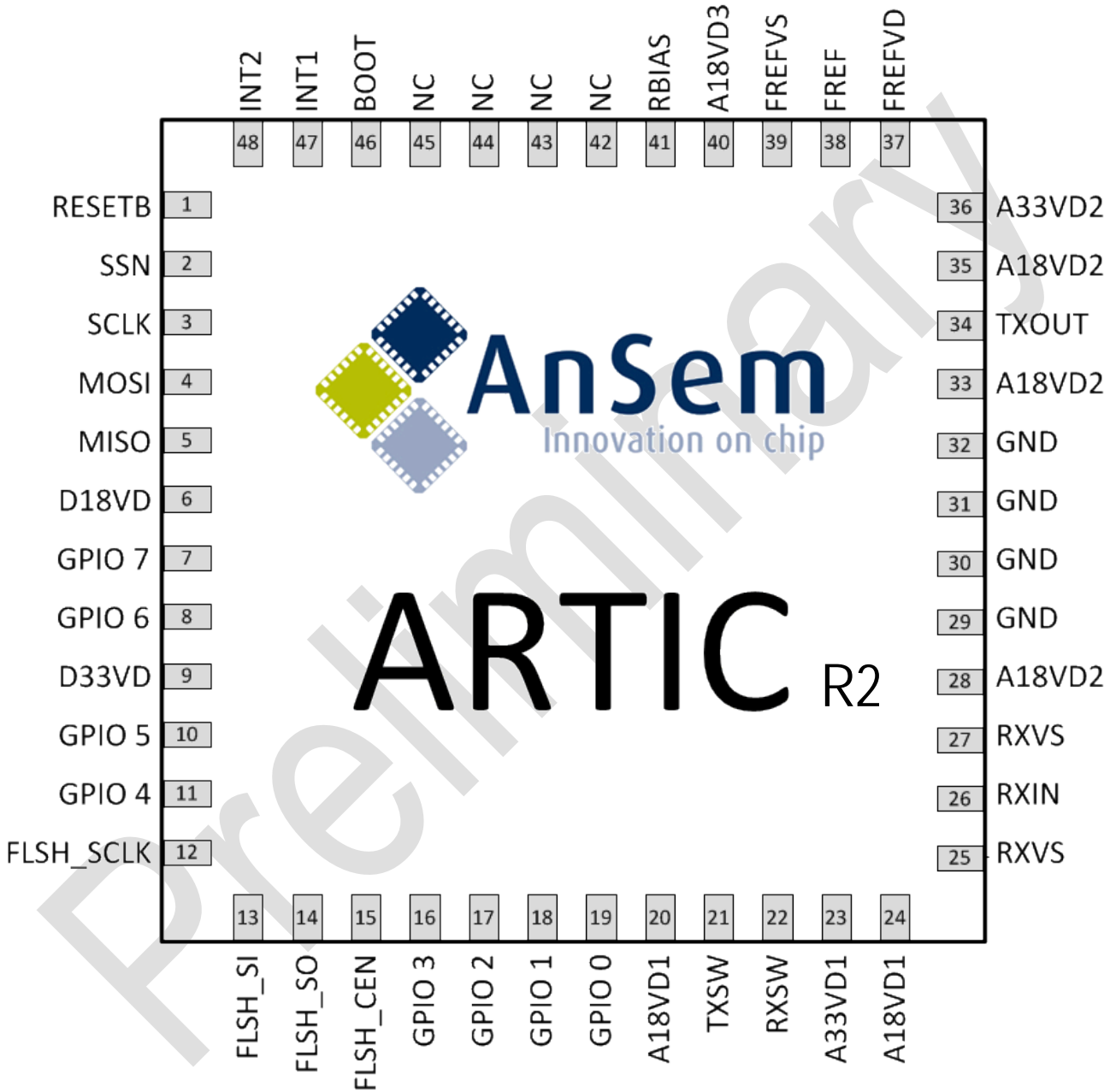
Figure 1 Functional Block Diagram

¹ Not yet supported in R2

1. Device Information

1.1 Pad Assignments

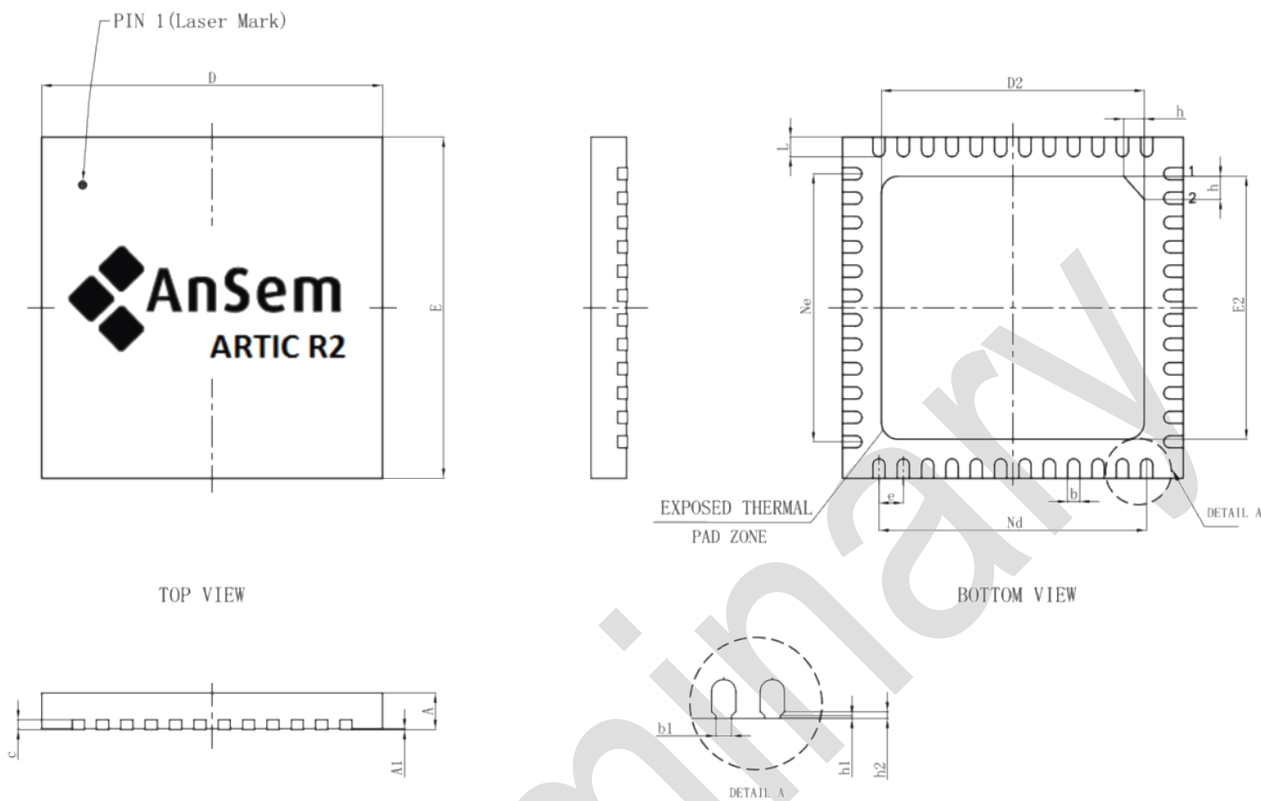
The ARTIC is assembled in a 7mm by 7mm, 48 lead QFN package, and 0.5mm pitch



1.2 Pin Descriptions

Pin	Name	Description	Voltage domain
1	RESETB	Global chip reset	3.3V
2	SSN	SPI slave select	3.3V
3	SCLK	SPI clock	3.3V
4	MOSI	SPI master out slave in pin	3.3V
5	MISO	SPI master in slave out pin	3.3V
6	D18VD	Digital 1.8V supply	1.8V
7	GPIO 7	General purpose input/output pin	3.3V
8	GPIO 6	General purpose input/output pin	3.3V
9	D33VD	Digital 3.3V supply	3.3V
10	GPIO 5	General purpose input/output pin	3.3V
11	GPIO 4	General purpose input/output pin	3.3V
12	FLSH_SLK	SPI Flash clock	3.3V
13	FLSH_SI	SPI Flash slave in pin	3.3V
14	FLSH_SO	SPI Flash slave out pin	3.3V
15	FLSH_CEN	SPI Flash slave select	3.3V
16	GPIO 3	General purpose input/output pin	3.3V
17	GPIO 2	General purpose input/output pin	3.3V
18	GPIO 1	General purpose input/output pin	3.3V
19	GPIO 0	General purpose input/output pin	3.3V
20	A18VD1	Analog 1.8V supply	1.8V
21	TXSW	Transmit switch control signal	3.3V
22	RXSW	Receive switch control signal	3.3V
23	A33VD1	Analog 3.3V supply	3.3V
24	A18VD1	Analog 1.8V supply	1.8V
25	RXVS	RX input ground pin	1.8V
26	RXIN	RX input	1.8V
27	RXVS	RX input ground pin	1.8V
28	A18VD2	Analog 1.8V supply	1.8V
29-32	VSS	Ground connection	
33	A18VD2	Analog 1.8V supply	1.8V
34	TXOUT	Low power PA output	1.8V
35	A18VD2	Analog 1.8V supply	1.8V
36	A33VD2	Analog 3.3V supply	3.3V
37	FREFVD	TCXO supply	1.8V
38	FREF	TCXO input	1.8V
39	FREFVS	TCXO ground	1.8V
40	A18VD3	Analog 1.8V supply	1.8V
41	RBIAS	External bias resistor	1.8V
42-45	NC	Not connected	-
46	BOOT	Digital 3.3V input	3.3V
47	INT1	Interrupt 1	3.3V
48	INT2	Interrupt 2	3.3V
PAD	VSS	Ground connection	GND

1.3 Package dimensions



Symbol	Millimetres		
	Min	Nom	Max
A	0.70	0.75	0.8
A1	-	0.02	0.05
b	0.18	0.25	0.30
b1	0.11	0.16	0.21
c	0.18	0.20	0.23
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e	0.50BSC		
Ne	5.50BSC		
Nd	5.50BSC		
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
h1	0.03REF		
h2	0.10REF		

1.4 Storage

The packages have a Moisture Sensitivity Level (MSL) rating of 3; please see the latest IPC/JEDEC J-STD-033 standard for MSL description and MSL 3 bake conditions.

Maximum recommended shelf life for dry packed SMD packages shall be a minimum of 12 months from the bag seal date, when stored in a noncondensing atmospheric environment of <math><40^{\circ}\text{C}/90\% \text{RH}</math>.

For an unopened bag, packaged in a sealed MBB (Moisture Barrier Bags) with desiccant, the shelf life of SMD is greater than 5 years for MSL 3 parts. This assumes that the MBB remains intact; therefore, double-bagging is recommended for extremely long-term storage.

Maximum recommended shelf life in unsealed/exposed to oxygen packaging is 6 months.

Floor Life (out of bag) at factory ambient $\leq 30^{\circ}\text{C}/60\% \text{RH}$: MSL3: 168 hours. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions $\leq 30^{\circ}\text{C}/60\% \text{RH}$.

1.5 Soldering

Reflow soldering with long industrial convection ovens is the preferred method of soldering the ARTIC chip to a printed circuit board or PCB. The temperature profile in Figure 2 acts as a temperature guideline for soldering the ARTIC QFN. The required peak temperature is $240 \pm 5^{\circ}\text{C}$.

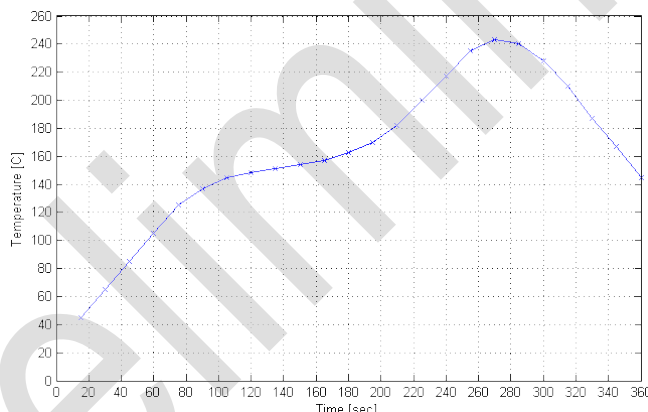


Figure 2 Reflow temperature profile

1.6 Typical usage

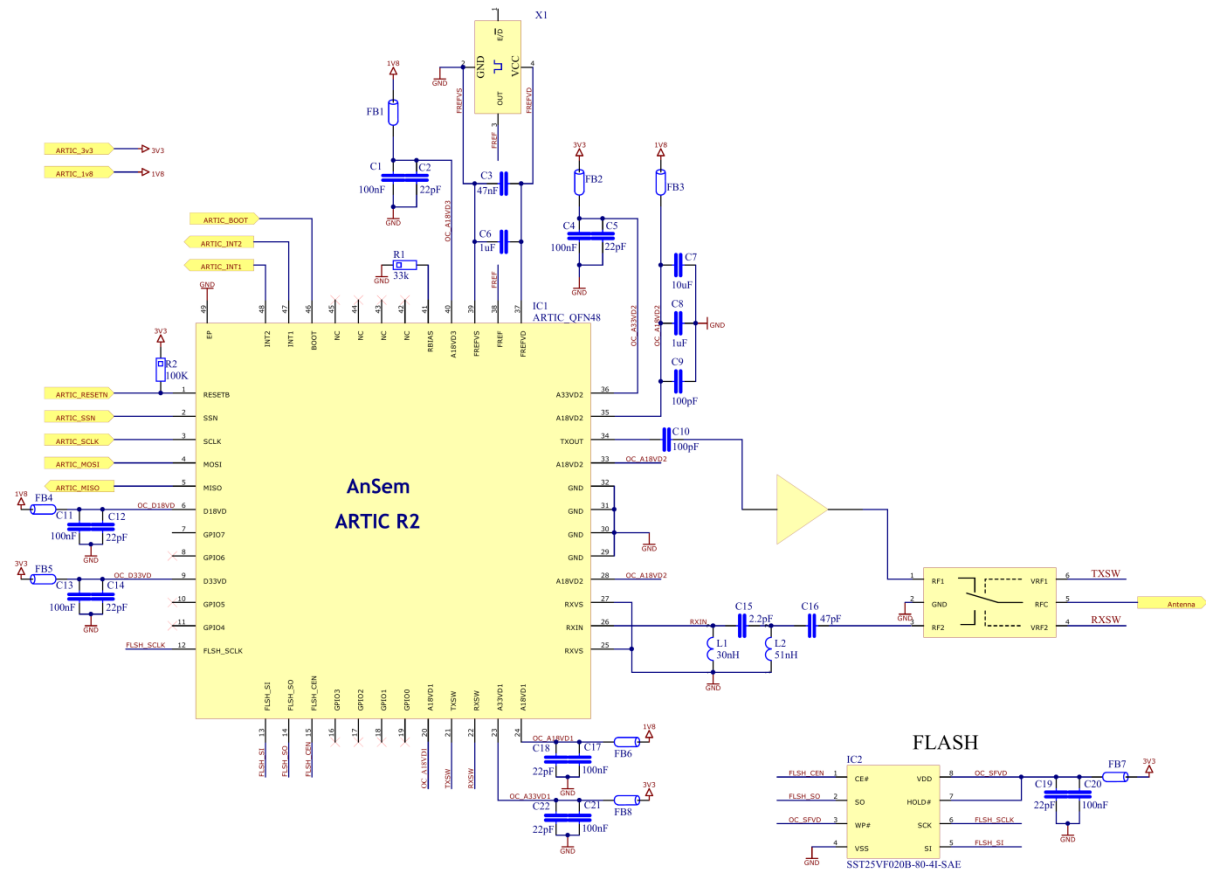


Figure 3 Typical usage of the ARTIC chip

Build of material:

Designator	Qty	Manufacturer	Part number	Cap.	Volt.	Res.	Ind.	Curr.	Tol.
FB1, FB2, FB4, FB5, FB6, FB7, FB8	7	MUR	BLM15AG221SN1D					300mA	25%
FB3	1	MUR	BLM15EG221SN1D					700mA	25%
IC1	1	ANS	ARTIC_QFN48						
IC2	1	MIC	SST25VF020B-80-4I-SAE						
X1	1	KYOCERA			1.8V				
C1, C4, C11, C13, C17, C20, C21	7	XXX	MC0402B104K160CT	100nF	16V				10%
C9, C10	2	MUL	MC000274	100pF	50V				5%
C7	1	AVX	C1005X5R0J106M050BC	10uF	6V3				20T
C6, C8	2	MUR	GRM155R60J105KE19D	1uF	6.3V				10T
C15	1	MUL	MC000282	2.2pF	50V				2.3%
C2, C5, C12, C14, C18, C19, C22	7	MUL	CBR04C220J5GAC	22pF	50V				5%
C3	1	MUR	GRM155R71C473KA01D	47nF	16V				10T
C16	1	KER	CBR04C470F3GAC	47pF	25V				1%
L1	1	CLC	0402HP-30NXGLU			0.35	30nH	450mA	2%
L2	1	CLC	0402HP-51NXGLU			0.7R	51nH	360mA	2%
R1	1	YAG	RC0402FR-0733KL			33k			1%
R2	1	MUL	MCMR04X1003FTL			100K			1%

Note:

More information on the external amplifier and RF switch can be found in the report (AnSem, 20/12/2019).

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

	VALUE	UNIT
Supply voltage, A33VD1, A33VD2, D33VD with respect to VSS	0 to 3.63V	V
Supply voltage, A18VD1, A18VD2, A18VD3 and D18VD with respect to VSS	0 to 1.9V	V
RXIN input power	10	dBm
Power consumption	300	mW
Maximal junction temperature	+125	°C
Storage temperature range	-40 to +125	°C
Operating temperature range	-40 to +85	°C

If stresses are applied that are beyond those listed above permanent damage may be caused to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may degrade device reliability.

2.2 Electrical Characteristics

(A18VD1 = A18VD2 = A18VD3 = D18VD = 1.8V, A33VD1 = A33VD2 = D33VD = 3.3V, Tj = -40 to +85°C, unless otherwise noted. Typical values are at Tj = 25°C)

2.2.1 Receiver

2.2.1 a) Argos3

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input power level					dBm
ARGOS 3 normal mode	Tj = 25°C	-126		-112	
ARGOS 3 backup mode	Tj = 25°C	-128		-112	
Noise figure	Tj = 25°C			5.7	dB
ADC resolution			7		Bits
ADC sampling frequency			650		kHz
Allowed spurious levels	For f at f _c +15kHz>f>f _c -15kHz			-145	dBm
	For f: f _c +200kHz>f>f _c +50kHz f _c -50kHz>f>f _c -200kHz			-97	dBm
	For f: f _c +1MHz>f>f _c +880kHz f _c -880kHz>f>f _c -1MHz			-72	dBm
Allowed Phase noise	f=1Hz			-24	dBc/Hz
	10kHz>f>100Hz			-90	dBc/Hz

2.2.1 b) Argos4

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input power level	$T_j = 25^\circ\text{C}$	-130		-112	dB
Noise figure	$T_j = 25^\circ\text{C}$			5.8	dB
ADC resolution			5		Bits
ADC sampling frequency			2		MHz
Demodulator loss				2	dB
Allowed spurious levels	In-band			-145	dBm
	Out-of-band	1MHz offset		-97	dBm
		2MHz offset		-92	dBm
		5MHz offset		-77	dBm
		10MHz offset		-67	dBm
Allowed Phase noise	$f=1\text{Hz}$			-24	dBc/Hz
	$10\text{kHz}>f>100\text{Hz}$			-90	dBc/Hz

2.2.2 Transmitter

2.2.2 a) General characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
TX output power			1		mW
SSB phase noise	100Hz		-83		dBc/Hz
	1kHz		-91		dBc/Hz
	10kHz		-94		dBc/Hz
	100kHz		-95		dBc/Hz
	1MHz		-124		dBc/Hz
Phase accuracy			1.06		Deg.
Amplitude accuracy			0.3		dB

2.3 SPI Interface

This is the interface between the MCU and the ARTIC. The SPI interface makes use of the standard generic ANSEM SPI interface, which is a 4-wire interface (SCLK, SSN, MOSI, and MISO). Its behaviour is quasi real time meaning that during accesses the provided/requested data word is been processed by the embedded DSP before the next word arrives/is requested.

Following SPI modes are implemented in the ARTIC: standard access mode, burst mode and command mode.

2.3.1 SPI Timing Characteristics

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{CKH}	SCLK high time	20	-	ns
T_{CKL}	SCLK low time	20	-	ns
T_{SSS}	SSN falling to first SCLK edge	20	-	ns
T_{SSH}	Last SCLK edge to SSN rising	20	-	ns
T_{SIS}	MOSI valid to SCLK sample edge	10	-	ns
T_{SIH}	SCLK sample edge to MOSI change	10	-	ns
T_{SOH}	SCLK shift edge to MISO change	-	10	ns

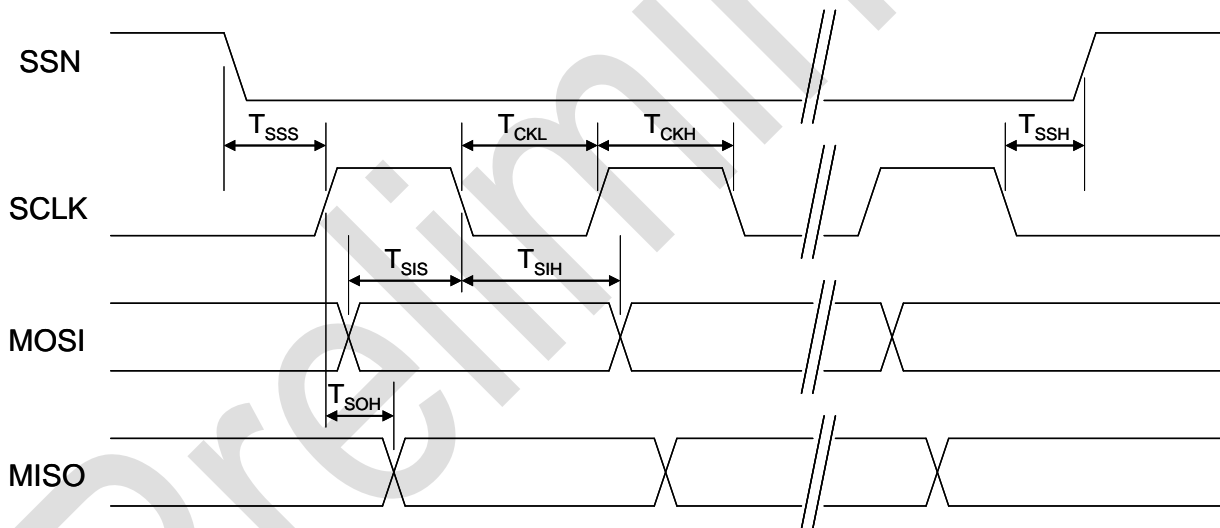


Figure 4 - SPI Interface Timing Diagram

2.3.2 Standard mode

In the standard mode the protocol first sends an address (7 b), followed by an opcode bit (indicating read or write), and finally the data (24 b, send by master or slave, depends on the opcode bit). See Figure 5.

Opcode bit:

- Read : 1
- Write : 0

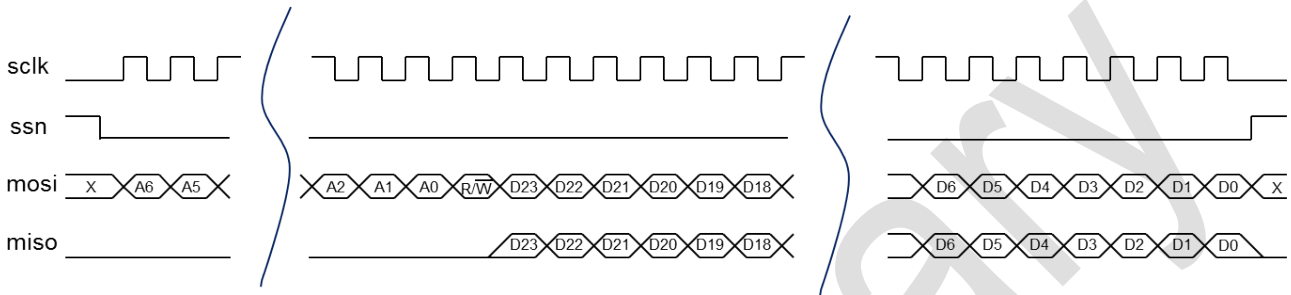


Figure 5 - SPI Interface Communication Protocol

The registers that can be accessed using the standard access mode are listed in Table 1. Their usage is explained further on.

Table 1 - Standard mode register map

address	R/W	Name
0x00	W	BURSTMODE_REG
0x01	RW/R	

2.3.2 a) BURSTMODE_REG

Table 2 - BURSTMODE register

R/W	Reset	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	00000000	reserved				burst_mode_on	burst_mem_sel<1:0>		burst_r_nw_mode
	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	00000000	burst_start_add<15:8>							
	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	00000000	burst_start_add<7:0>							

- Bit 19 burst_mode_on '1', the next SPI access is considered a burst access.
- Bit 18:17 burst_mem_sel<1:0> Selects which memory is accessed by the SPI burst.
 "00" : Program memory
 "01" : X memory
 "10" : Y memory
 "11" : I/O memory.
- Bit 16 burst_r_nw_mode Indicates if the SPI burst is a read or a write burst.
 '0' : write burst
 '1' : read burst.
- Bit 15:0 burst_start_add<15:0> Indicates the location of the register that is first accessed by the SPI burst.

2.3.3 Burst mode

The default SPI protocol is extended with an extra feature: burst mode (for both read and write actions). The burst mode allows access to the memory regions used by the DSP and can be used to transfer large amounts of data.

A burst mode is configured by performing a standard mode write to the dedicated 'burst mode' register, followed by the actual burst. The SSN line must be released briefly after the 'burst mode' register is written to allow the ARTIC to configure for the burst. The next time the SSN goes low the actual burst starts.

See Table 2 for the content of the burst mode register. This register is not used for any other purpose then to control burst mode, and is write only.

The data width used during burst mode is automatically selected, based on the selected memory section. X, Y and shared IO memory use 24 bits. Program memory P uses 32 bits. See 2.4 for more information about the ARTIC memories.

2.3.3 a) Write

During a burst write access, the first 24/32 bits received via the MOSI line are written to the register at the address as specified by `burst_start_add<15:0>`. Next the internal address pointer is incremented by 1. The next 24/32 bits are written to this new address location (`=burst_start_address+ 1`). Next the internal address pointer is again incremented by 1. This mechanism continues during the complete duration of the burst.

The data is sent or received MSBit first. The SSN line needs to remain active low during the complete duration of the burst, since a rising edge on the SSN line is used to indicate the end of the burst. In this event, the next SPI access will be treated again as a standard access. In order to perform another burst access, first bit 'burst_mode_on in register 'burst mode' must be written again.

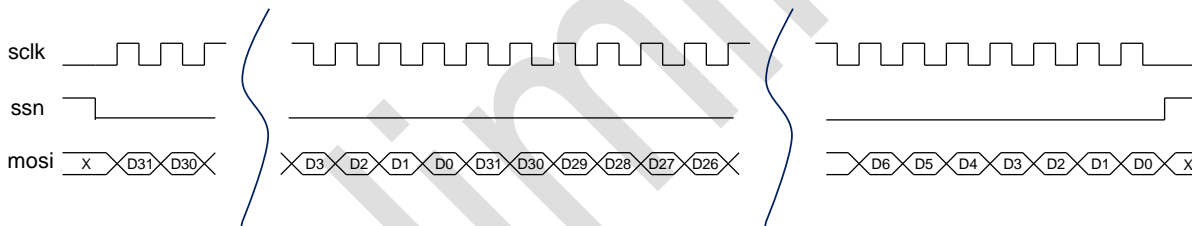


Figure 6 - SPI interface, burst write access with burst duration = 1 register

2.3.3 b) Read

During a burst read access, the 24/32 bit content of the register at the address as specified by 'burst_start_add<15:0>' is output via the MISO line (MSBit first).

The user has to wait for the duration of 24 SPI clock cycles after configuring the burst read mode, before starting the first read. This allows some time for the internal memory access block to retrieve the first data sample.

A next read is triggered when the previous read data starts to be shifted out by the SPI interface. The address is incremented automatically, as is the case during a write burst.

The SSN line needs to remain active low during the complete duration of the burst. A rising edge on the SSN line indicates the end of a burst. In this event, the next SPI access is treated again as a standard access.

The data during a burst is sent or received MSBit first (like it is the case during a normal access).

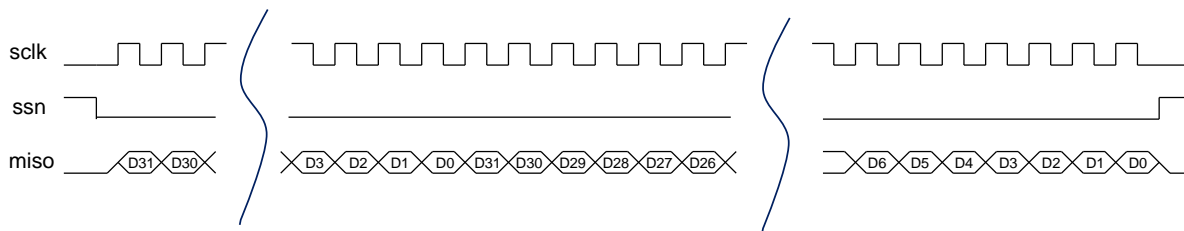


Figure 7 - SPI interface, burst read access with burst duration = 1 register

2.3.4 Command access

The SPI protocol is extended with a second feature: command access. A command access exists of a short SPI access of only 8 clock cycles. If the SSN line goes inactive after 8 clock cycles, the ARTIC will interpret the 8-bit as a command access, see Figure 8. With this feature, 256 different commands can be sent directly to the DSP, see section 3.3 for a complete list of commands.

In case the ARTIC is up and running, one of the 2 interrupts lines will be set when the command has been processed by the DSP. For each interrupt line that is set, additional information can be accessed as described in 3.2.

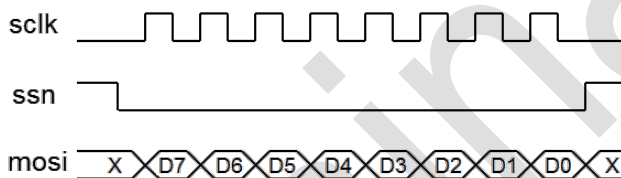


Figure 8 - SPI 8-bit command access

2.4 ARTIC Memories

The ARTIC has 4 types of memory which can only be accessed using the SPI burst mode. The maximum speed at which the SPI can operate depends on the memory that is accessed. See Table 3 for a description.

Table 3 - ARTIC memory widths

Memory	Word size	Memory size [words]	Max SPI clock speed[MHz]		Description
			Read	Write	
P	32 bit	10240	1.5	5	DSP Program memory
X	24 bit	21845	1.25	3.5	DSP X memory
Y	24 bit	6826	1.25	3.5	DSP Y memory
IO	24 bit	-	1.25	3.5	ARTIC IO memory

The P, X and Y memories must be loaded each time after reset. Only firmware that is supplied by ANSEM can be used. Using other software will void all warranties immediately.

The firmware can be loaded by the MCU or the ARTIC can automatically download firmware from an external memory. See 3.1

2.5 Boot configuration

The ARTIC can boot the firmware from an external flash or the user can supply the firmware via SPI. The ARTIC will boot from the [onboard] external flash memory when the boot pin is high and reset is released. If the boot pin is held low at reset the ARTIC will wait for the MCU to upload the Firmware. The boot pin must be connected either through GND or VCC using a pulldown or pullup resistor.

2.6 Bias

Use a 33k Ω 1% tolerance resistor as bias reference for the ARTIC. [pin 41]. This resistor is used to generate all internal reference currents.

2.7 Reset

The reset is active low [pin 1]. Use a 100k Ω pullup resistor to activate the ARTIC at power-up.

2.8 GPIO

The ARTIC has 8 GPIO's available. Currently only GPIO7 is used as an output to activate an external PA during transmission.

2.9 Flash interface

A Flash memory can be attached to store the ARTIC firmware. The ARTIC is able to boot from the flash memory. See section 3.1.1 how this boot method is accessed. The external flash memory is connected to the ARTIC through a dedicated SPI interface, which f.i. can be found on the SST25VF020B from Microchip.

2.10 TCXO interface

The ARTIC uses a 26MHz TCXO. The stability of the TCXO is crucial to meet the ARGOS requirements. All tests were performed using the KT1612AWC26000. The TCXO is only activated during transmission or reception in order to save power. The rest of the time an internal oscillator running at 500 kHz is used.

3. Operating the device

This chapter covers the operating instructions of the ARTIC chip:

- Start-up and Boot process.
- Reading the ARTIC status
- Controlling the ARTIC.
- Transmit and receive messages.

3.1 Start-up sequence

The ARTIC requires firmware to be loaded after each power up or reset. The firmware can be uploaded by SPI or using an external flash memory. Both options are described in this paragraph.

3.1.1 Flash memory

To boot the ARTIC chip from the attached flash memory the following actions have to be made:

1. Apply the 3.3V and 1.8V supplies of the ARTIC chip.
2. Pull the BOOT pin to 3.3V
3. Pull the RESETB pin to 3.3V

The ARTIC will read the external flash memory and starts booting. Interrupt 2 (INT 2) will be set

4. Wait until INT1 pin is high. [2.25 sec]

The ARTIC chip is ready to accept commands.

3.1.2 SPI booting

Following actions have to be made to boot the ARTIC chip by transferring the program over SPI:

1. Apply the 3.3V and 1.8V supplies of the ARTIC chip.
2. Pull the BOOT pin to 0V
3. Pull the RESETB pin to 3.3V

The ARTIC is brought out of reset. Interrupt 2 (INT 2) will be set

4. Write the DSP program memory using SPI
 - a. Write to the top register *burstmode_reg* with following information:
 - i. Memory type: program memory (00b)
 - ii. Address range (0b)
 - iii. write mode (0b)

The 32b sequence written via SPI will be 0x00080000

- b. Next in a SPI burst mode the data is written to the program memory

5. Write the DSP X memory using SPI
 - a. Write to the top register *burstmode_reg* with following information:
 - i. Memory type: X data memory (01b)
 - ii. Address range (0d)
 - iii. write mode (0b)

The 32b sequence written via SPI will be 0x000A0000

- b. Next in a SPI burst mode the data is written to the Y memory

6. Write the DSP Y memory using SPI

- a. Write to the top register *burstmode_reg* with following information:
 - i. Memory type: Y data memory (10b)
 - ii. Address range (0d)
 - iii. write mode (0b)The 32b sequence written via SPI will be 0x000C0000
 - b. Next in a SPI burst mode the data is written to the Y memory
7. Perform one 24 bit write access to the top level *register dsp_ctrl_reg* to activate the DSP.
 - i. The 32b sequence written via SPI will be 0x02000000The ARTIC will start booting.
 8. Wait until INT1 pin is high. [250msec]
The ARTIC chip is ready to accept commands.

Note:

- Step 1 and 2 may be concurrent by connecting the RESETB pin on the PCB to the 3.3V supply.
- During the booting process CRC's are calculated, see 0.

3.2 Firmware status – interrupt flags

The ARTIC firmware will talk to the MCU using 2 interrupt lines (INT1, INT2) and a number of internal flags. These flags provide more insight why a specific interrupt is set. The firmware state can also be consulted.

The user can access the firmware status/interrupt flags by reading a single register. This 24-bit register is present in the IO memory at address 0x8018 and can be accessed using an SPI burst. This register can only be read.

The complete 32-bit sequence is 0x000F8018. Next in a 24-bit SPI burst the register is read.

Table 4 - Firmware status - interrupt flags

BIT	Signal		Description
0	IDLE	Current Firmware state	The firmware is idle and ready to accept commands.
1	RX_IN_PROGRESS		The firmware is receiving.
2	TX_IN_PROGRESS		The firmware is transmitting.
3	BUSY		The firmware is changing state.
4	RX_VALID_MESSAGE	Interrupt 1 flags	A message has been received.
5	RX_SATELLITE_DETECTED		A satellite has been detected.
6	TX_FINISHED		The transmission was completed.
7	MCU_COMMAND_ACCEPTED		The configuration command has been accepted.
8	CRC_CALCULATED		CRC calculation has finished.
9	IDLE_STATE		Firmware returned to the idle state.
10	RX_CALIBRATION_FINISHED		RX offset calibration has completed.
11	-		-
12	-		-
13	RX_TIMEOUT		Interrupt 2 flags
14	SATELLITE_TIMEOUT	No satellite was detected within the specified time.	
15	RX_BUFFER_OVERFLOW	A received message is lost. No buffer space left.	
16	TX_INVALID_MESSAGE	Incorrect TX payload length specified.	
17	MCU_COMMAND_REJECTED	Incorrect command send or Firmware is not in idle.	
18	MCU_COMMAND_OVERFLOW	Previous command was not yet processed.	
19	-	-	
20	-	-	
21	INTERNAL_ERROR	An internal error has occurred.	
22	dsp2mcu_int1		Interrupt 1 pin status
23	dsp2mcu_int2		Interrupt 2 pin status

3.3 MCU commands

If the user transfers only 8 bit over SPI (indicated by SSN going high after 8 bits), the data is interpreted as a command. The list of available commands is separated into 3 sets:

- Configuration
- Instructions
- Housekeeping

Note:

These commands are handled by the DSP and can require some time to be processed. The DSP does not buffer these commands. If a previous command is not completed, the ARTIC will set interrupt 2 with the MCU_COMMAND_OVERFLOW flag. This second command is lost.

3.3.1 Configuration

The following commands are available supporting all ARGOS 2/3/4 standards. The user should check which commands are supported by the firmware as specified in the README file.

These commands will configure the DSP into the correct ARGOS mode. If the command is processed, the DSP will respond by setting INT 1 high and by stating MCU_COMMAND_ACCEPTED as described in 3.2.

The ARTIC will reject configuration commands send during reception or transmission. If a command is rejected INT 2 will be set with the MCU_COMMAND_REJECTED flag.

If an unsupported command is send, INT 2 will also be set with the MCU_COMMAND_REJECTED flag.

Table 5 - Configuration commands

8 bit command	Configuration command	Description
00000001b	Set ARGOS 4 RX mode	Configure the receiver in ARGOS 4 mode
00000010b	Set ARGOS 3 RX mode	Configure the receiver in ARGOS 3 mode
00000011b	Set ARGOS 3 RX backup mode	Configure the receiver in ARGOS 3 backup mode
00000100b	Set PTT-A2 TX mode	Configure the transmitter in ARGOS 2 mode
00000101b	Set PTT-A3 TX mode	Configure the transmitter in ARGOS 3 mode
00000110b	Set PTT-ZE TX mode	Configure the transmitter in ARGOS ZE mode
00000111b	Set ARGOS 3 PTT-HD TX mode	Configure the transmitter in ARGOS 3-HD mode
00001000b	Set ARGOS 4 PTT-HD TX mode	Configure the transmitter in ARGOS 4-HD mode
00001001b	Set ARGOS 4 PTT-MD TX mode	Configure the transmitter in ARGOS 4-MD mode
00001010b	Set ARGOS 4 PTT-VLD TX mode	Configure the transmitter in ARGOS 4-VLD mode

When an ARGOS 4 transmission command is used, the receiver will be automatically configured for ARGOS 4. Equally, using an ARGOS 3 transmission command will configure the receiver in ARGOS 3.

3.3.1 a) *Verify configuration*

The configuration of the ARTIC can be verified by reading the 'ARGOS configuration' register. The content of this register is explained in Table 6.

See 3.4 for how to access the 'ARGOS configuration' register. This register is read only.

Table 6 - ARGOS configuration register

R/W	Reset	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
R	00000000	reserved							
	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	00000000	reserved							
	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	00010000	RX configuration				TX configuration			

Bit 7-4 RX configuration

- 0x0 : ARGOS 3 RX [default]
- 0x1 : ARGOS 3 RX backup mode
- 0x2 : ARGOS 4 RX

Bit 3-0 TX configuration

- 0x0 : ARGOS PTT-A2 [default]
- 0x1 : ARGOS PTT-A3
- 0x2 : ARGOS PTT-ZE
- 0x3 : ARGOS PTT-HD
- 0x4 : ARGOS PTT-A4-MD
- 0x5 : ARGOS PTT-A4-HD
- 0x6 : ARGOS PTT-A4-VLD

3.3.2 **Instructions**

The commands in Table 7 are used to start receiving or to transmit a message. Each command is explained separately alongside a list of all the possible interrupt flags that can be set during the execution.

Table 7 - Instruction commands

8 bit command	Instruction command
01000001b	Start continuous reception
01000010b	Start receiving 1 message
01000011b	Start receiving 2 messages
01000110b	Start reception for fixed time
01001000b	Transmit one package and go to idle
01001001b	Transmit one package and start reception for fixed time
01010000b	Go to idle
01010101b	Satellite detection

Note:

- Both interrupts and all interrupt flags will be cleared automatically whenever an instruction command is send.

3.3.2 a) *Start continuous reception*

Start the ARTIC in receiving mode for an unlimited time and unlimited number of messages. The user has to use the 'Go to idle' command to stop the receiver. See 3.6.2 for the interrupt explanation.

Possible interrupt flags	Interrupt
RX_VALID_MESSAGE	1
RX_BUFFER_OVERFLOW	2
RX_SATELLITE_DETECTED	-

3.3.2 b) *Start receiving 1 message*

Start the ARTIC in receiving mode for an unlimited time until 1 message has been received. If the message is received the Artic will go to IDLE. The user can abort the reception using the 'Go to idle' command. See 3.6.2 for the interrupt explanation.

Possible interrupt flags	Interrupt
RX_VALID_MESSAGE	1
RX_SATELLITE_DETECTED	-

3.3.2 c) *Start receiving 2 messages*

Start the ARTIC in receiving mode for an unlimited time until 2 messages have been received. If the 2 messages are received the ARTIC will go to IDLE. The user can abort the reception using the 'Go to idle' command. See 3.6.2 for the interrupt explanation.

Possible interrupt flags	Interrupt
RX_VALID_MESSAGE	1
RX_SATELLITE_DETECTED ²	-

3.3.2 d) *Start reception for fixed time*

Start the ARTIC in receiving mode for a programmable time and for an unlimited amount of messages. After the programmed time has finished the ARTIC will go to IDLE. The user can abort the reception using the 'Go to idle' command. After the receiver has been active for the programmed amount of time, INT 2 will be set with the 'RX_TIMEOUT' flag. See 3.6.2 for the explanation of the other interrupts. See 3.6.4 on how to configure the timeout.

Possible interrupt flags	Interrupt
RX_VALID_MESSAGE	1
IDLE_STATE	1
RX_TIMEOUT	2
RX_BUFFER_OVERFLOW	2
RX_SATELLITE_DETECTED ²	-

² During reception the 'RX_SATELLITE_DETECTED' flag will be set high as long as the ARTIC is receiving 0x7E flags.

3.3.2 e) *Transmit one package and go to idle*

The ARTIC will transmit the payload message according to the configured ARGOS mode and will go to IDLE. See 3.4.1 for more information

Possible interrupt flags	Interrupt
TX_FINISHED	1
IDLE_STATE	1
TX_INVALID_MESSAGE	2

3.3.2 f) *Transmit one package and start reception for fixed time*

The ARTIC will transmit the payload message according to the configured ARGOS mode and will switch to reception mode as described in 'Start reception for fixed time'. See 3.4.1 for more information about the transmission.

Possible interrupt flags	Interrupt
TX_FINISHED	1
RX_VALID_MESSAGE	1
RX_TIMEOUT	2
RX_BUFFER_OVERFLOW	2
TX_INVALID_MESSAGE	2
RX_SATELLITE_DETECTED ³	-

3.3.2 g) *Go to idle*

The ARTIC will return to idle mode. This command will not have an effect whenever the ARTIC is in 'BUSY' state. Once the ARTIC has returned to the idle state, interrupt 1 will be raised and the IDLE_STATE flag will be set.

Possible interrupt flags	Interrupt
IDLE_STATE	1

3.3.2 h) *Satellite detection*

The ARTIC will start looking for a satellite for a specified amount of time. If no satellite is detected, INT 2 will be set with the 'SATELLITE_TIMEOUT' flag. If a satellite was detected, by receiving 5 consecutive 0x7E flags, INT 1 will be set with the 'RX_SATELLITE_DETECTED' flag. See 3.6.4 on how to configure the timeout.

Possible interrupt flags	Interrupt
RX_SATELLITE_DETECTED ²	1
SATELLITE_TIMEOUT	2

3.3.3 **Housekeeping**

Following commands can be used to clear the interrupt and the corresponding flags. The ARTIC chip will not re-raise an interrupt before it is cleared by the MCU. Henceforth it is good practice to clear an interrupt once it has been set.

³ During reception the 'RX_SATELLITE_DETECTED' flag will be set high as long as the ARTIC is receiving 0x7E flags.

8 bit command word	housekeeping commands
10XXXXXXb	Clear interrupt line 1
11XXXXXXb	Clear interrupt line 2

Preliminary

3.4 Memory locations

Table 8 is a list of the memory locations that are needed to configure the Firmware. All these parameters are located in the X memory and must be accessed using the burst mode as described in 2.3.3.

Table 8 - Parameter memory locations

Parameter name	Start address [hex]	Size [24-bit words]	Read / Write
ARGOS configuration	0x0384	1	R
RX payload	0x0200	9	R
RX filtering configuration	0x0209	104	R/W
RX timeout	0x0271	1	R/W
Satellite detection timeout	0x0272	1	R/W
TX payload	0x0273	220	W
TX frequency Argos 2/3	0x034F	1	R/W
TX frequency Argos 4	0x035F	1	R/W
TCXO warmup time	0x036F	1	R/W
TCXO control	0x0370	1	R/W
CRC results	0x0371	3	R
TX certification interval	0x0379	1	R/W

3.4.1 Read example

Read the 'CRC results' at address 0x0371, length: 3-words

1. Configure SPI burst to read X memory at address 0x0371
SPI Write 0x000B0371 [32-bit]
2. Read the CRC results
SPI read 0x000000 0x000000 0x000000 [3x 24-bit]

The SSN line must be raised briefly between step 1 and 2. See 0 for more information about the CRC check.

3.4.2 Write example

Write the 'RX timeout' parameter at address 0x0271 with value 0x00000A [= 10 seconds timeout]

3. Configure SPI burst to write X memory at address 0x0271
SPI Write 0x000A0271 [32-bit]
4. Write the 24-bit parameter
SPI write 0x00000A [24-bit]

The SSN line must be raised briefly between step1 and 2.

3.5 Transmission

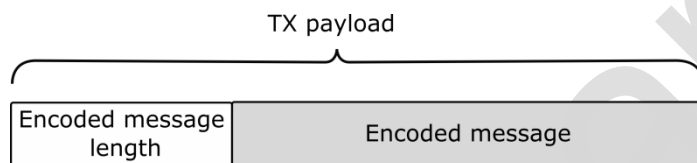
The ARTIC is able to transmit messages according the various ARGOS modulation standards. See 3.3.1 on how to configure the ARTIC. Only 1 transmission will occur for each TX command.

3.5.1 Transmission payload

Depending on the configured ARGOS mode different message lengths can be transmitted. The user has to ensure that the message makes sense to the satellite. The ARTIC only checks the maximum allowed message length.

Some ARGOS transmission standards require specific bits to be added for correct reception by the satellite. For each standard a brief overview is given. Please read the ARGOS transmission standard specifications to comprehend the message content thoroughly.

The transmission payload must be written before any transmission command is issued.



The payload buffer contains 2 items:

- Encoded message length:
 - Defines the length of the TX user message in bits.
 - This user message length occupies the first 24-bit word of the TX payload.
- Encoded message
 - This is the encoded message as described in
 - Starts at the second 24-bit word of the TX payload.
 - The first bit of the Uplink message is aligned with the MSB of the second 24-bit word of the payload buffer. Bit 25 of the Uplink message is aligned with the MSB of the third 24-bit word of the payload buffer. In this way the total Uplink message occupies a number of consecutive 24-bit words in the payload buffer.
 - In case the total length of the Uplink message is not a multiple of 24 bits, the last used 24-bit word of the payload buffer should be stuffed by the MCU with 0's at the LSB locations.

Note that if the TX payload is smaller than the TX payload buffer (220 x 24 bit words), the not used words at the end of the buffer don't need to be written by the MCU.

The location of the TX payload can be found in Table 8.

Following tables explain the uplink message composition according to the different ARGOS standards.

3.5.1 a) ARGOS 2

Table 9 - ARGOS 2 uplink messages

Message length [bits]	ID number [bits]	User data [bits]
4	28	24
		56
		88
		120
		152
		184
		216
		248

Preliminary

3.5.1 b) ARGOS 3

Table 10 - ARGOS 3 uplink messages

Message length [bits]	ID number [bits]	User data [bits]	Tail bits [bits]
4	28	24	7
		56	8
		88	9
		120	7
		152	8
		184	9
		216	7
		248	8

3.5.1 c) ARGOS ZE

Table 11 - ARGOS ZE uplink message

Message length [bits]	ID number [bits]	Tail bits [bits]
0	28	8

3.5.1 d) ARGOS 3-HD

Table 12 - ARGOS 3 HD uplink messages

Message length [bits]	ID number [bits]	User data [bits]	Tail bits [bits]
4	28	32	8
		512	8
		1024	9
		1536	7
		2048	8
		2560	9
		3072	7
		3584	8
		4096	9
		4608	7

3.5.1 e) ARGOS 4 MD

The message length is coded inside the synchronization pattern which is added by the ARTIC. After each block of 512 bits the MCU has to add 1 parity bit and 2 tail bits. The Frame check sequence is only used during PMT mode and can be used for additional data in PTT mode. For more details read the document A4-SS-TER-SP-0078-CNS.

Table 13 - ARGOS4 MD uplink messages

ID number [bits]	User data [bits]	Frame check sequence [bits]
28	452	32
	964	

3.5.1 f) ARGOS 4 HD

The message length is coded inside the synchronization pattern which is added by the ARTIC. For each block of 1024 bits the MCU has to add 1 parity bit and 2 tail bits. The Frame check sequence is only used during PMT mode and can be used for additional data in PTT mode. For more details read the document A4-SS-TER-SP-0078-CNS.

Table 14 - ARGOS 4 HD uplink messages

ID number [bits]	User data [bits]	Frame check sequence [bits]
28	964	32
	1988	
	3012	
	4036	
	5060	

3.5.1 g) ARGOS 4 VLD

The message length is coded inside the synchronization pattern which is added by the ARTIC.

Table 15 - ARGOS 4 VLD uplink messages

ID number [bits]	User data [bits]
28	0
	28

3.5.2 TCXO warm up time

Some TCXO's require a warmup time before each transmission in order to stabilize the frequency and to meet the certification requirements. This warm up time is set by default to 10 seconds but can be altered if another TCXO is used. The TCXO warmup time will start after sending a TX instruction command. During this time the ARTIC will appear in BUSY mode. See 3.4 for the 'TCXO warmup' memory location. If the warmup time is set to 0, no frequency stabilization is performed.

Parameter	Unit	Default
TCXO warmup time	Seconds	10

3.5.3 Transmission frequency

Before transmitting the TX frequency should be set by the MCU. The ARTIC uses separate transmission frequency parameters for ARGOS 2/3 and ARGOS 4, the frequency can be adjusted up to a few Hz.

In order to change the transmission frequency, the fractional PLL parameter has to be calculated as follows:

$$fractional\ part = round \left(2^{22} * \left(\frac{(tx_{freq} * 4)}{26e6} - 61 \right) \right)$$

Example for 401.65MHz:

$$fractional\ part = round \left(2^{22} * \left(\frac{(401.65e6 * 4)}{26e6} - 61 \right) \right) = 3323179 = 0x32b52b$$

This fractional number must be written in the 'TX frequency ARGOS x' memory locations as specified in 3.4.

Transmission frequency shall be chosen adequately, and follow the frequency allocation defined by Kinéis.

3.6 Reception

The ARTIC can buffer 2 messages internally and can be programmed to filter messages based upon their ID. The CRC of each received message can be automatically verified.

3.6.1 Configuring the downlink message filtering

The downlink message filtering can be configured by the MCU via the X data memory. See 0 for the 'RX filtering configuration' parameter for the memory location. First the address map is shown, next the features are explained.

Table 16 - Downlink message filtering memory map

Address offset	Content	Reset
0	EnableCRC	0x000001
1	TransparentMode	0x000000
2	Not used	-
3	Length of address LUT	0x000000
4	Address LUT – ID number 1, LSBits	-
5	Address LUT – ID number 1, MSBits	-
6	Address LUT – ID number 2, LSBits	-
7	Address LUT – ID number 2, MSBits	-
...	...	
104	Address LUT – ID number 50, LSBits	-
105	Address LUT – ID number 50, MSBits	-

EnableCRC:

Each downlink message contains a CRC field. During normal operation only messages with a valid CRC are passed to the MCU.

- If set to 0x000001, the CRC check is enabled. [Default]
- If set to 0x000000, the CRC check is disabled. All received messages are considered valid.

TransparentMode:

In the default situation only messages with an ID mentioned in the Address LUT are sent to the MCU. This filtering can be bypassed by activating the transparent mode.

- If set to 0x000001, the transparent mode is enabled. All messages are sent to the MCU.
- If set to 0x000000, the filtered mode is enabled. [Default]

Length of address LUT

- This word determines the length of the Address LUT.
- The max length is 50

Address LUT

- The Address LUT lists all the ID numbers that should be compared against the addressee Identification field of an incoming message during filtered mode, in order to determine if the incoming message should be signalled to the MCU via INT1.
- Since an ID number is 28 bits long, it is spread over 2 consecutive LUT words.
- The 24 LSBits are stored at the lowest address.
- The 4 MSBits are stored at the highest address, using format 0x00000Y, with Y = 4 MSBits.
- The content of each 28 bit ID number can be anything, but to be compliant to the ARGOS standards, it should be one of the following
 - Unique Node ID number as assigned by CLS
 - Group ID of group(s) to which the PMT belongs.
 - All cast ID supported by the PMT

3.6.2 Reception signalling and buffering

The ARTIC can buffer 2 messages internally before the third message arrives, then this third message will be discarded. On this event INT 2 will be set with the RX_BUFFER_OVERFLOW flag.

When the ARTIC receives a valid downlink message, it raises INT 1 with the RX_VALID_MESSAGE flag. The MCU can then use an SPI burst access to read the downlink message from the X data memory.

After reading the downlink message, the ARTIC reception buffer must be cleared. This is done by sending the 'Clear interrupt 1' command.

If a second message was received it will be moved to the 'RX payload' buffer upon the 'Clear interrupt 1' command. In this case INT 1 will be re-raised after 100usec. The MCU can read the RX payload again and use the 'Clear interrupt 1' command.

3.6.3 Read downlink messages

A part of the X data memory is reserved for a downlink message. This part is referred to as RX payload. The RX payload buffer occupies 9 x 24-bit words and starts at the address location described in 0

The RX payload buffer contains 2 items:

- Downlink payload length:
 - Defines the length of the downlink message in bits.
 - The downlink message length occupies the first 24-bit word of the payload buffer.

- Downlink message
 - Downlink message as defined by ARGOS standard *A4-SYS-IF-0086-CNES*, see Table 17.
 - Starts at the second 24-bit word of the payload buffer.
 - The first bit of the Downlink message is aligned with the MSB of the second 24-bit word of the payload buffer. Bit 25 of the Downlink message is aligned with the MSB of the third 24-bit word of the payload buffer. In this way the total Downlink message occupies a number of consecutive 24-bit words in the payload buffer.
 - In case the total length of the Downlink message is not a multiple of 24 bits, the last used 24-bit word of the payload buffer is stuffed by the DSP with 0's at the LSB locations.

Table 17 - Downlink message format

Addressee Identification	A-DCS @	Service	Data	FCS
28 bits	4 bits	8 bits	$n \times 8$ (with $2 \leq n \leq 17$ bits)	16 bits

3.6.4 Configuring timeouts

Instructions like "Start reception for fixed time" and "Satellite detection" have a programmable timeout. . Values are in seconds, maximum timeout is 2^20 seconds. See 3.4 for the memory locations.

Table 18 - Default timeouts values

Parameter	Unit	Default
RX Timeout	Seconds	10
Satellite Detection Timeout	Seconds	2

3.7 CRC Check

During the firmware boot process a CRC is calculated on the memories. The MCU can check these values with the CRC results supplied by the firmware of the ARTIC to ensure that the downloaded content is correct.

When initialization (and CRC check) is finished, INT 1 is set. At this time the MCU can read the CRC checksum results and compare them against the reference values, which are provided with the firmware files.

There are 3 x 24-bit checksums which can be read back from XMEM. See 3.4 for the 'CRC results' memory location

Table 19 - CRC results map

Address offset [word]	Content
0	P memory CRC results
1	X memory CRC results
2	Y memory CRC results

3.8 Firmware version

The firmware version is hardcoded in program memory and is located in Program memory at word 0x10 and has a length of 2 x 32 bit words. See Table 20 for the content of the version information.

Table 20 - Version content map

Byte	Content
0 - 4	ASCII string: ARTIC
5 - 7	ASCII Firmware version 000-999

SPI sequence to read the firmware version string:

1. Configure SPI burst to read program memory at address 0x0010:
 SPI write: 0x00090010
2. Read version string
 SPI read 2x32 bit

3.9 TCXO control feature

The ARTIC has the option to be fed by either 1.8V, 3.3V or a more precise power supply provided in small steps of 0.1V. Selecting 1V8 trumps 3V3 select, which trumps on its turn 1V3 to 2V7 selection.

The ARTIC can be programmed to keep the TCXO on after a TX or RX command.

See word parameter 'TCXO control' under 3.4 for the memory location.

Table 21 - TCXO control values

R/W	Reset	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	00000000	Not used		3V3 select	1V8 select	1V3 to 2V7 select			
	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	00000000	Not used							
	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	00000000	Not used							

Table 22 – TCXO control Description

Register name	Description
1V8 select	TCXO is fed by PLLVD=1.8V
3V3 select	TCXO is fed by A33VD2=3.3V
1V3 to 2V7 select	Select the TCXO supply voltage acc. $V_{out} = 1.3 + 0.1 * reg$
Auto disable	Set if TCXO shall remain active after an instruction command

3.10 GPIO

The ARTIC has 8 general purpose input/output pins. Each pin can be individually controlled by the DSP as input or output. Upon customer request, specialized firmware to read / control these pins can be created.

Currently GPIO7 is programmed to activate an external PA during a transmission. This control signal will be set high 10msec before the transmission starts and is set low at the end of the transmission.

GPIO's 4-7 can drive 11.6mA; GPIO 3-0 can drive 3.9 mA.

3.11 Power consumption

The current consumption of the ARTIC chip is displayed in Table 23. The currents are measured during different ARTIC states. The power consumption is calculated taking a DC/DC convertor efficiency of 95% to go from 3.3V to 1.8V.

Figure 9 shows the typical power consumption during the 'Transmit one package and start reception for fixed time' instruction command.

Table 23 - ARTIC Power consumption

ARTIC state	1.8V [mA]	3.3V [mA]	Power consumption [mW]
Reset	0.212	0.0014	0.4
Start up	12.3	1.52	28.3
IDLE	0.135	0.0014	0.26
TCXO warmup	0.475	1.14	4.7
RX	22.1	2.38	49.6
TX	28.6	2.26	61.5

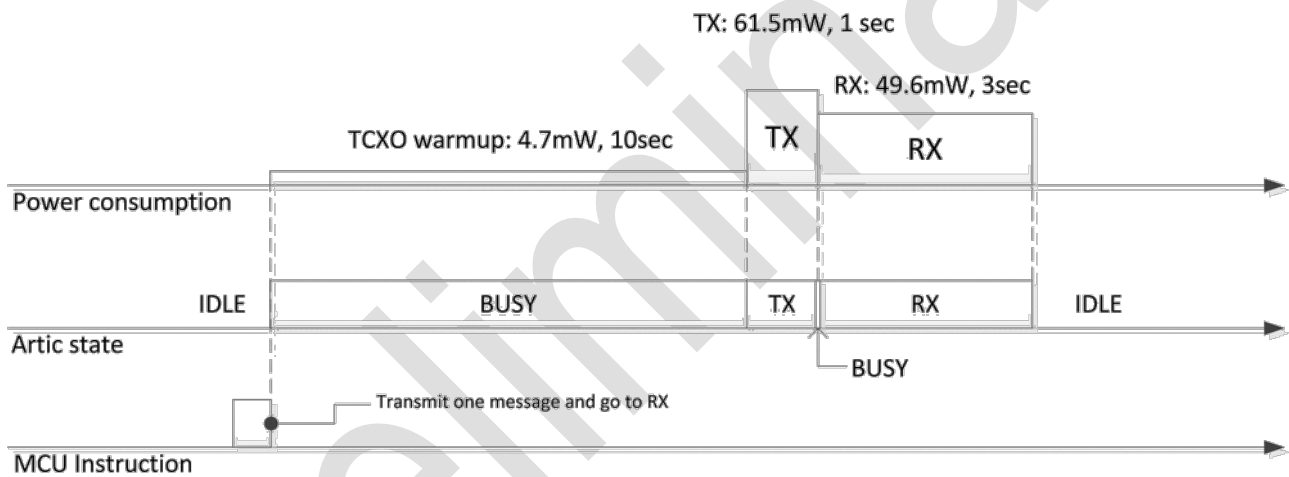


Figure 9 - Typical power consumption.

3.12 Timing transmission and receiving

The timing of different transceiver states and output signals of the ARTIC are given in Figure 10, Figure 11 and Figure 12. Each figure displays another command type. The 3 output signals coming from the ARTIC are TXSW, RXSW and PA_EN. A signal will not be displayed when the data does not change during the command execution. There can be some variability on the edges e.g. searching for the carrier of a packet can vary in time due to the spacing between packets and the different methods used. The transmission and reception time depends on the packet type and is shown in paragraph 3.13. The duration of the TCXO warmup can be directly configured using the TCXO control register.

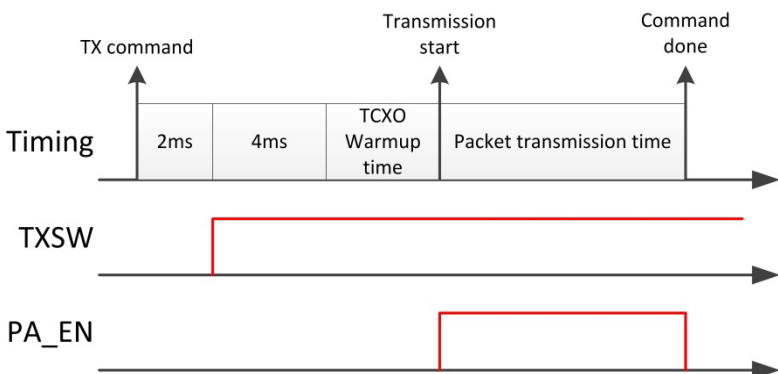


Figure 10 Timing of a transmission command

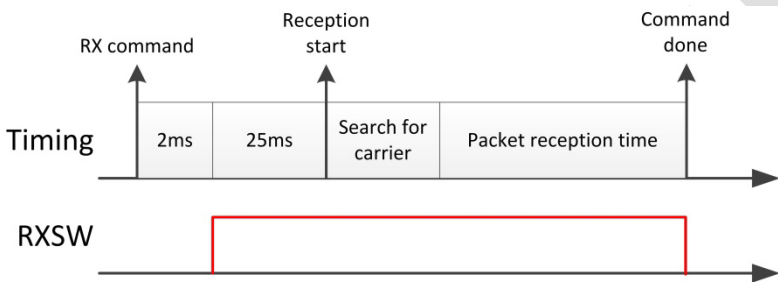


Figure 11 Timing of a reception command

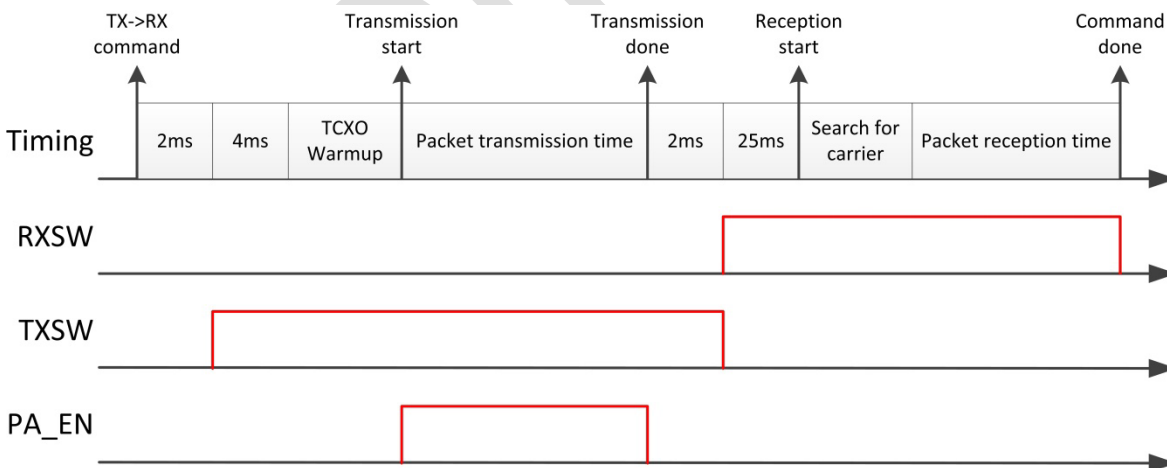


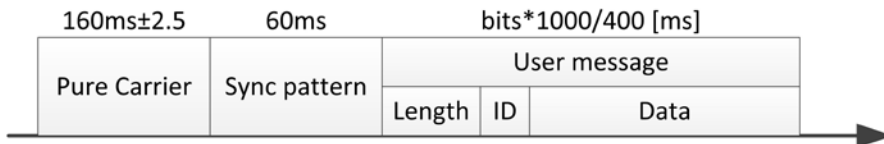
Figure 12 Timing of a combined transmission and reception command

3.13 Packet timing

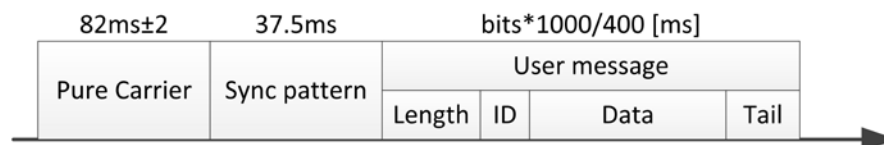
In Figure 13 the timings are shown for the different Argos transmit and receive messages. Each message has a variable amount of user message bits; therefore the time needed by the user message itself should be calculated using the

amount of bits used and the formula given. The total time needed for the packet may have small tolerances of around 1-2%. Most bit-lengths of the user message elements can be found in chapter 3.5 or 3.6, except for the SYNC part. This part is added by the ARTIC, but its size can be calculated using the formula: $\text{floor}(\text{BS}/775) * 16$.

ARGOS 2



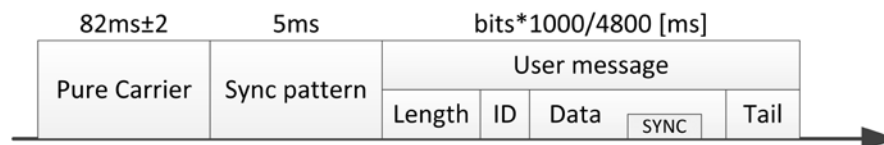
ARGOS 3



ARGOS ZE



ARGOS 3 HD



ARGOS RECEIVE

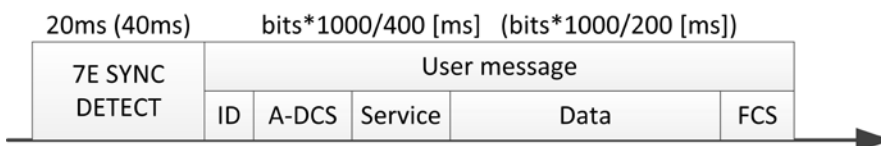


Figure 13 Timings of the different packet types used by argos

3.14 Examples

In this paragraph some situations are described to give an idea how to interact with the ARTIC chip.

In each example the Y-Axis displays the time [not always proportional]. The main objective of these examples is to create a correct understanding of the ARTIC state machine and how to control it.

3.14.1 Transmit one package and start continuous reception

This example shows the usage of the 'Transmit one package and start reception for fixed time' command. It involves the transmission preparation and the reception of a message.

- MCU sends a configuration command to configure the ARTIC to the correct ARGOS mode.
- Wait until INT 1 is set with the MCU_COMMAND_ACCEPTED flag.
- INT 1 is cleared by the MCU using the 'Clear interrupt 1 flag'
- The TX payload is prepared by the MCU and written to the ARTIC.
- The MCU sends the 'Transmit one package and start continuous reception' instruction command.
- The ARTIC transmits the payload and starts receiving.
- After some time a downlink message is received which is signalled to the MCU by setting INT 1.
- The message is read by the MCU and the MCU sends the 'clear interrupt 1' command on which the ARTIC lowers interrupt 1.
- After some more time to MCU sends the 'Go to idle'. This makes the ARTIC to go to idle.
- Once the ARTIC has returned to idle, INT 1 is set with the IDLE_STATE flag.
- Interrupt 1 is cleared by the MCU using the 'Clear interrupt 1 flag'

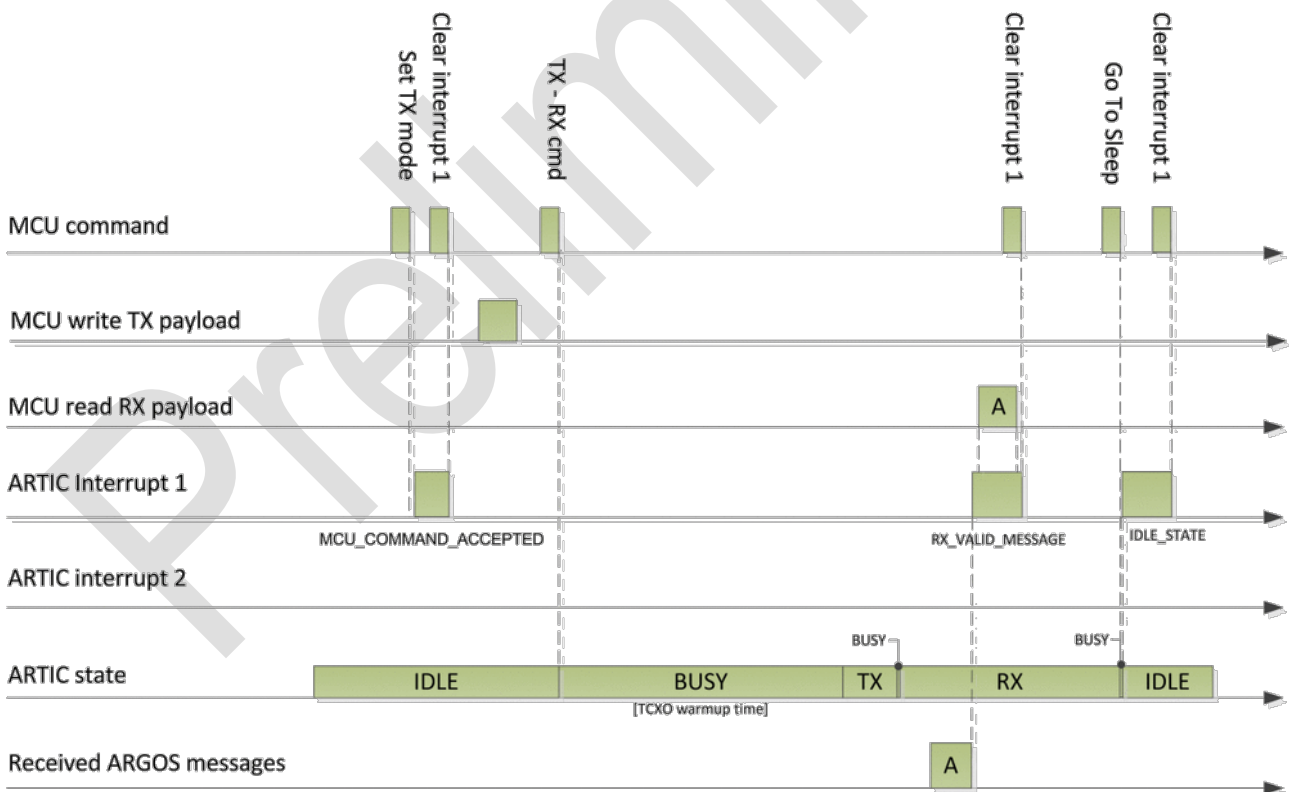


Figure 14 - Transmit one package and start fixed time reception

3.14.2 Reception of multiple messages

This example shows the behaviour of the ARTIC while receiving multiple messages, including a buffer overflow.

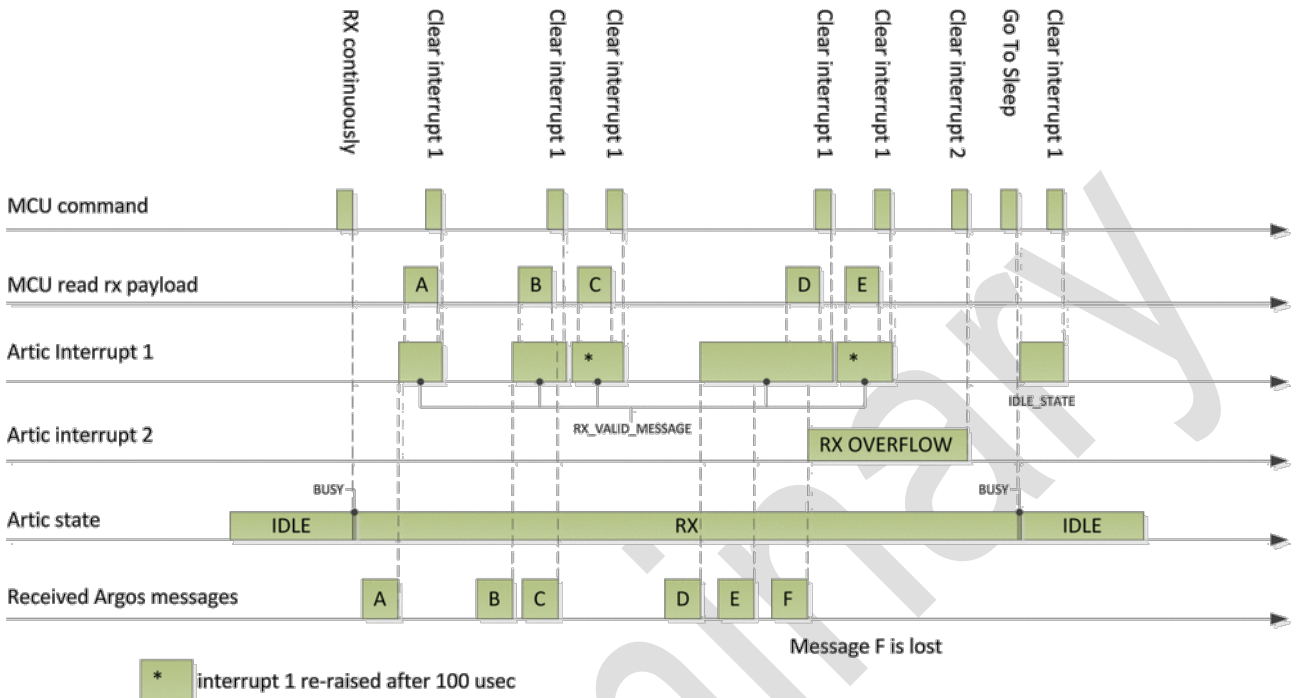


Figure 15 - Reception of multiple messages

4. Layout considerations

Following layout examples should be considered for an optimal performance of the ARTIC chip.

4.1 PCB buildup

Good RF designs use at least a 4 layer PCB. The top layer is used for all components. Layer 2 and 3 are GND planes and the bottom layer is used for additional routing. The middle layers create a very low impedance GND plane to avoid any ground issues.

4.2 TCXO

The ARTIC needs a 26MHz clipped sine TCXO for the onboard synthesizer. This TCXO is powered by the FREFVD and FREFVS signals. A 1 μ F decoupling capacitor must be placed as close possible to the ARTIC for decoupling, see C25 in Figure 16. On the evaluation board the KT1612ACW26000TAN TCXO from Kyosera is placed. The PCB layout however also allows the usage of the KT2016ACW26000Txx which is slightly larger. A 47nF decoupling capacitor is placed close to the TCXO as required by Kyosera.

The FREFVS signal must be connected to GND as close possible to the GND connection of the TCXO.

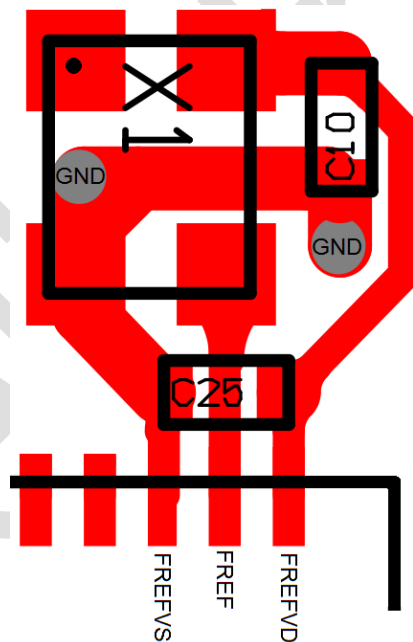


Figure 16 - TCXO PCB layout

4.3 Receiver

The RX filter circuit is the most sensitive part of the ARTIC as it must cope with input signals of -130dBm. Therefore all switching signals [DC/DC convertors, oscillators,...] must be placed far away.

The filter circuit components must be placed as close possible to the ARTIC. The PCB layout of the RX signal should be completely routed in the top layer [No via's]. The 2 RXVS pins surrounding the RXIN pin should be used to form a guard ring around the matching circuit and should be connected to ground. The GND layer under the RX components must be cut away to minimize coupling effects. See Table 24 for the recommended components.

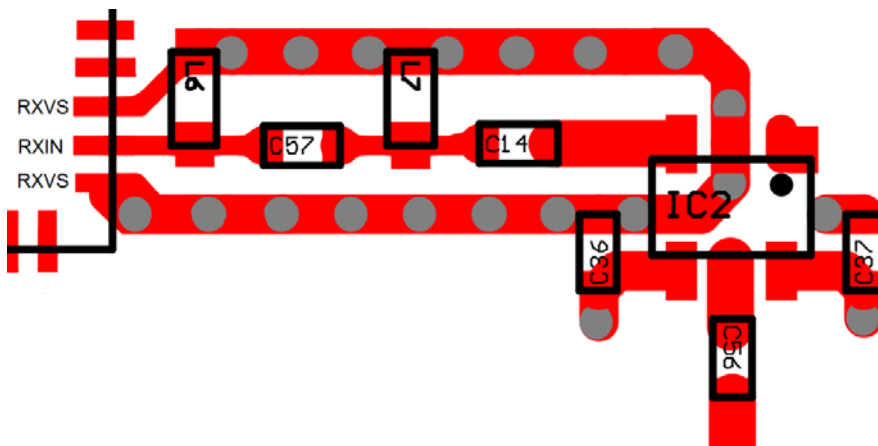


Figure 17 - Top PCB layer with RX path, guard ring and RF switch

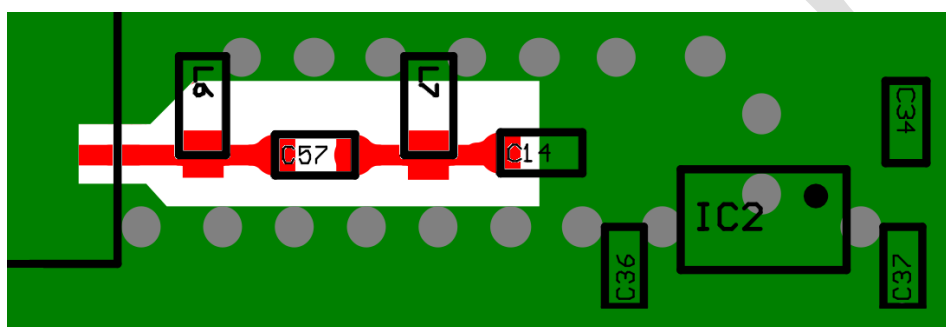


Figure 18 - PCB layer 2 with cut-out underneath RX path

Table 24 - RX components

Designator	Value	Package	Manufactory	Manufactory Number
C57	2.2pF	0402	MULTICOMP	MC000282
C14	47pF	0402	KEMET	CBR04C470F3GAC
L6	30nH	0402	COILCRAFT	0402HP-30NXGLU
L7	51nH	0402	COILCRAFT	0402HP-51NXGLU