ANALOG DEVICES

EVAL-AD7383FMCZ Evaluation Board User Guide
UG-1770

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Evaluating the AD7383 Dual, Simultaneous Sampling, 16-Bit, 4 MSPS, SAR ADC, Pseudo Differential Input

FEATURES

- Fully featured evaluation board for the multichannel, simultaneous sampling AD7383
- On-board reference, reference buffer, and ADC driver
- On-board power supplies
- SDP-H1 controller board compatible
- PC software for control and data analysis

EVALUATION KIT CONTENTS

- EVAL-AD7383FMCZ evaluation board
- ACE software download instructions

EQUIPMENT NEEDED

- EVAL-SDP-CH1Z (SDP-H1) controller board
- USB cable (provided in the SDP-H1 kit)
- 12 V wall wart signal source (provided in the SDP-H1 kit)
- PC running Windows Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port

DOCUMENTS NEEDED

- AD7383 data sheet

SOFTWARE NEEDED

- ACE software
- AD738x ACE plug-in (provided in the ACE software)

GENERAL DESCRIPTION

The EVAL-AD7383FMCZ is a fully featured evaluation board that evaluates all features of the AD7383 analog-to-digital converter (ADC). The EVAL-AD7383FMCZ is controlled by the EVAL-SDP-CH1Z (SDP-H1) system demonstration platform (SDP) via the 160-way SDP connector, J4. The SDP-H1 controls the EVAL-AD7383FMCZ through the USB port of a PC using the Analysis | Control | Evaluation (ACE) software, which is available to download from the ACE software page or the AD7383 product page.

The EVAL-AD7383FMCZ can be used to evaluate the AD7384 (14-bit, 4 MSPS), the AD4682 (16-bit, 1 MSPS), and the AD4683 (16-bit, 500 kSPS) pseudo differential, successive approximation register (SAR) ADCs. The AD7383 and the AD7384 only differ in the number of clock cycles when clocking out the conversion results, which are related to the resolution of the device. The AD4682 and AD4683 have a slower throughput rate than the AD7383.

For full details on the AD7383, see the AD7383 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-AD7383FMCZ. In addition, full details on the SDP-H1 are available on the SDP-H1 product page, and the comprehensive ACE user guide is available on the ACE software page.

Figure 1 shows the typical setup of the EVAL-AD7383FMCZ.

EVALUATION BOARD CONNECTION DIAGRAM

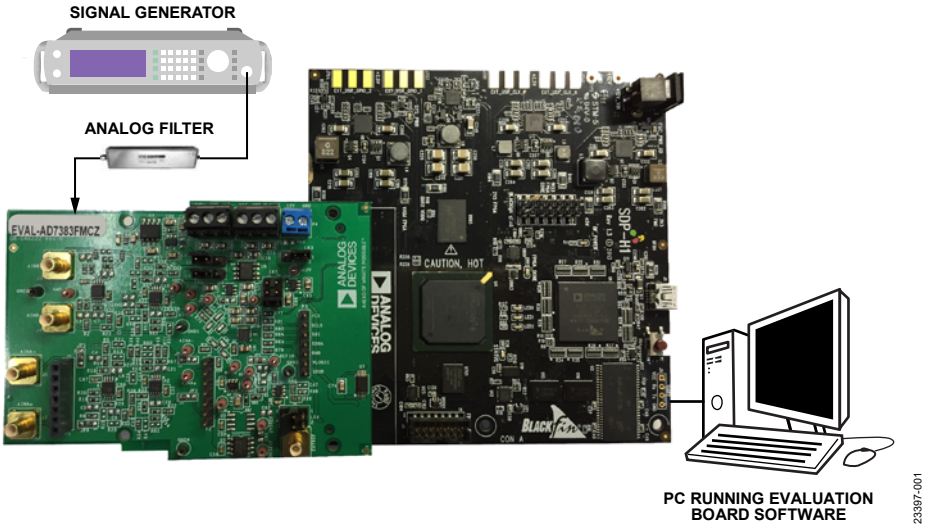

Figure 1.

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REVISION HISTORY

10/2020—Rev. 0 to Rev. A

Changes to General Description Section ... 1

8/2020—Revision 0: Initial Version

EVALUATION BOARD QUICK START GUIDE

The EVAL-AD7383FMCZ is powered by the SDP-H1 by default. External power supplies can be applied to the EVAL-AD7383FMCZ. See Table 1 for a description of the optional external power supply connectors and Table 2 for the required link option function descriptions. Take the following steps to evaluate the AD7383:

1. Download and install the ACE software, which is available on the ACE software page or the AD7383 product page. Details of the ACE installation are available on the internal label of the EVAL-AD7383FMCZ box. When installing the ACE software, ensure that the SDP-H1 is disconnected from the USB port of the PC. The PC may need to be restarted after the installation.
2. Ensure that the link options are configured as detailed in Table 2.
3. Connect the SDP-H1 to the EVAL-AD7383FMCZ, as shown in Figure 2.
4. Connect the SDP-H1 to the PC via the USB cable. If prompted by the operating system, choose to automatically search for the SDP-H1 drivers.
5. Launch the ACE software from the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
6. Connect an analog signal to Channel A or Channel B of the AD7383 via J2 for Channel A and J4 for Channel B. The $A_{IN}A-$ and $A_{IN}B-$ inputs are directly connected to VCM on the EVAL-AD7383FMCZ.

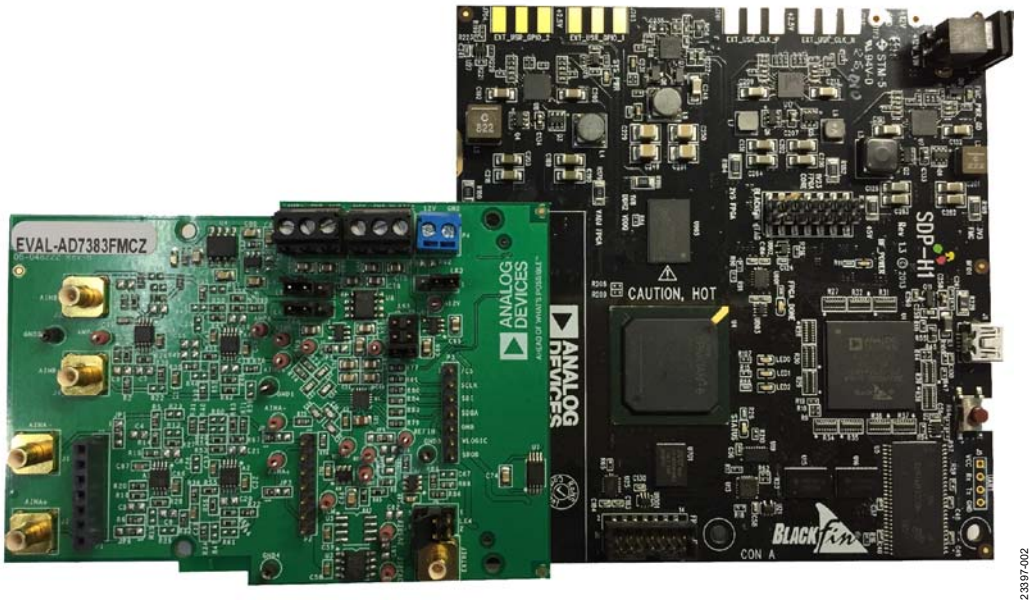

Figure 2. EVAL-AD7383FMCZ (Left) Connected to the SDP-H1 (Right)

EVALUATION BOARD HARDWARE

EVAL-AD7383FMCZ DESCRIPTION

The EVAL-AD7383FMCZ is an evaluation board for the AD7383, a 16-bit, dual, simultaneous sampling, high speed, low power, SAR ADC with a pseudo differential input.

POWER SUPPLIES

Ensure that all link positions are set according to the required operating mode before applying power and signals to the EVAL-AD7383FMCZ. See Table 2 for the complete list of link options.

The EVAL-AD7383FMCZ is powered by the SDP-H1 by default. External power supplies can be applied to the EVAL-AD7383FMCZ. See Table 1 for a description of the optional external power supply connectors and Table 2 for the required link option function descriptions. The EVAL-AD7383FMCZ has low dropout (LDO) linear regulators (the ADP7182, ADP7104, and ADP166) that supply power to the AD7383 and its supporting circuitry, such as the ADA4896-2 amplifiers and the ADR4533 reference circuit. An external 2.5 V power supply can also be used with AD7383. The EVAL-AD7383FMCZ has a footprint ready to place an ADR4525 when an external 2.5 V power supply is required for evaluation. A pseudo differential signal can be connected on the Subminiature Version B (SMB) connectors, J1 to J4.

Table 1. Optional External Power Supplies

Power Supply	Connector	Voltage Range (V)	Description
12 V	P4-1	12 ± 10%	Main board power supply for all internal voltage regulators
GND	P4-2	0	Ground
V_{CC}	P5-1	3.0 to 3.6	ADC analog power supply
GND	P5-2	0	Ground
V_{LOGIC}	P5-3	1.65 to 3.6	Digital serial peripheral interface (SPI) power supply
AMP+	P6-1	5 ± 5%	Amplifier positive power supply
GND	P6-2	0	Ground
AMP−	P6-3	−2.5 ± 5%	Amplifier negative power supply

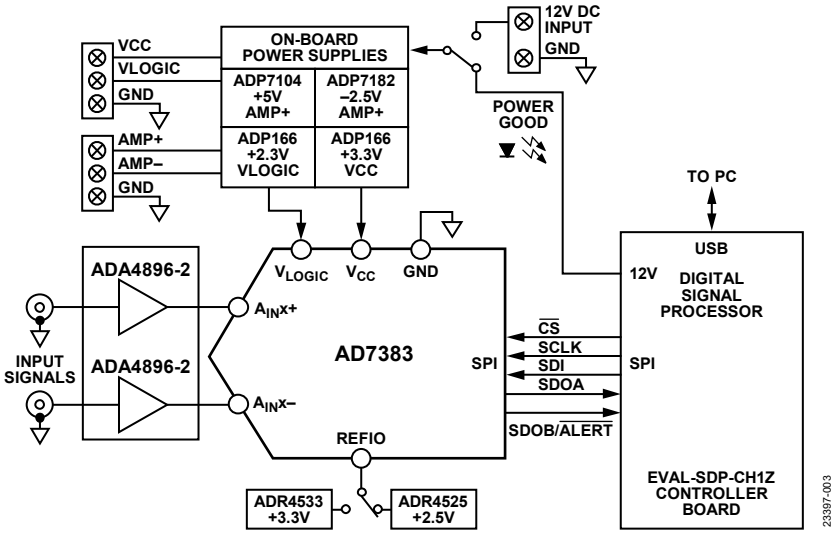

Figure 3. EVAL-AD7383FMCZ Functional Block Diagram

LINK CONFIGURATION OPTIONS

Multiple link options must be set properly to select the appropriate operating setup before using the EVAL-AD7383FMCZ. Table 2 details the function descriptions of these link options.

Setup Conditions

Ensure that all link positions are set as required by the selected operating mode before applying power and signals to the EVAL-AD7383FMCZ. Table 2 shows the default positions of the link options when the EVAL-AD7383FMCZ is packaged.

Table 2. Link Option Function Descriptions

Link Name	Function	Position[1]	Description
LK1	AMP−	1 (default)	Use the internal −2.5 V from U9 (ADP7182) for AMP−.
		3	Use the external −2.5 V via P6-3 (see Table 1).
LK2	AMP+	1 (default)	Use the internal 5 V from U8 (ADP7104) for AMP+.
		3	Use the external 5 V via P6-1 (see Table 1).
LK3	External 12 V supply	1 (default)	Use the 12 V power supply from the SDP-H1.
		3	Use the external 12 V power supply via P4-1 (see Table 1).
LK4	Reference voltage (V_{REF})	1	Use the external V_{REF} source connected via EXTREF (see Table 3).
		3 (default)	Use the internal 3.3 V from U3 (ADR4533) for V_{REF}.
		5	This option is not available. The ADR4525 footprint is in place.
LK5	V_{LOGIC}	3	Use the internal 2.3 V from U6 (ADP166) for V_{LOGIC}.
JP1	$A_{IN}A-$	1 (SMD resistor)	Connect the external SMB connector, J1, to A1 (ADA4896-2).
JP2	$A_{IN}A-$	1 (SMD resistor)	Connect the internal signal from A2 (ADA4896-2) to the AD7383 input, $A_{IN}A-$.
JP3	$A_{IN}A+$	1 (SMD resistor)	Connect the internal signal from A2 (ADA4896-2) to the AD7383 input, $A_{IN}A+$.
JP4	REFIO	1 (SMD resistor)	Use the internal 2.5 V V_{REF} on the AD7383. When using this option, do not insert the R3 resistor on the EVAL-AD7383FMCZ.
		3 (SMD resistor, default)	The REFIO pin is driven with the external on-board reference.
JP5	V_{CC}	1	Use the internal 3.3 V from U2 (ADP166) for V_{CC}.
JP6	$A_{IN}A+$	1 (SMD resistor)	Connect the external SMB connector, J2, to A1 (ADA4896-2).

[1] The SMD resistor is the surface-mount device resistor.

EVALUATION BOARD CIRCUITRY

SOCKETS AND CONNECTORS

The connectors and sockets on the EVAL-AD7383FMCZ are described in Table 3.

Table 3. On-Board Connectors

Connector	Function
J1	Negative analog input for Channel A ($A_{IN}A–$)
J2	Positive analog input for Channel A ($A_{IN}A+$)
J3	Negative analog input for Channel B ($A_{IN}B–$)
J4	Positive analog input for Channel B ($A_{IN}B+$)
P1	Amplifier mezzanine card inputs
P2	Amplifier mezzanine card outputs
P3	Digital SPI signals
P4	Main board power supply (12 V) for all internal voltage regulators
P5	ADC power supply and digital SPI power supply
P6	Amplifier power supply
P7	Field programmable gate array (FPGA) mezzanine card (FMC) to low pin count (LPC) connector
EXTREF	External voltage reference

The default interface to the EVAL-AD7383FMCZ is achieved via the 160-way connector. The connector attaches the EVAL-AD7383FMCZ to the SDP-H1. When using the EVAL-AD7383FMCZ in standalone mode, communication is achieved via the P3 header pins.

TEST POINTS

There are several test points and single in line (SIL) headers on the EVAL-AD7383FMCZ. These test points provide access to the signals from the EVAL-AD7383FMCZ for probing, evaluation, and debugging.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

Download the ACE software from the ACE software page or the AD7383 product page. Install ACE on a PC before using the EVAL-AD7383FMCZ.

The ACE installation process in the Installing the ACE Software section includes the ACE software installation and the SDP-H1 driver installation.

Install the ACE software and SDP-H1 drivers before connecting the EVAL-AD7383FMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

Installing the ACE Software

To install the ACE software, take the following steps:

1. Download the ACE software to a Windows®-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation (see Figure 4).

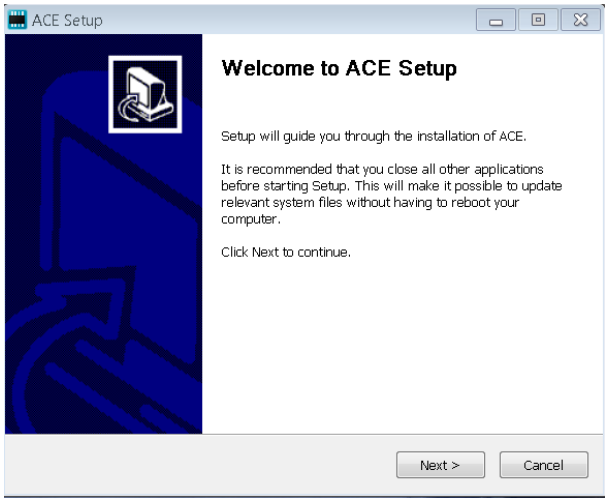

Figure 4. ACE Software Installation Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 5).

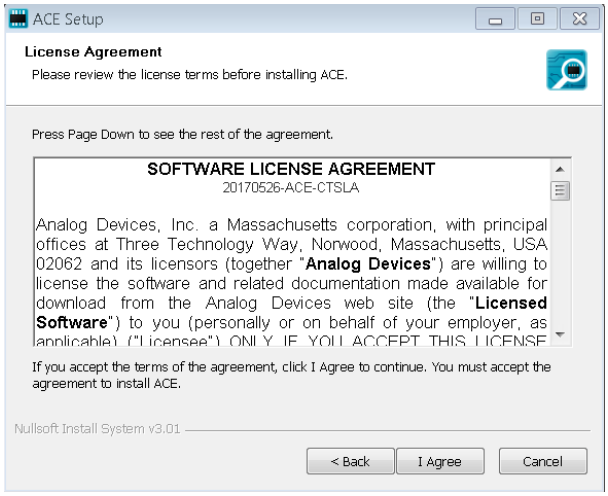

Figure 5. License Agreement

6. Click **Browse …** to choose the installation location and then click **Next >** (see Figure 6).

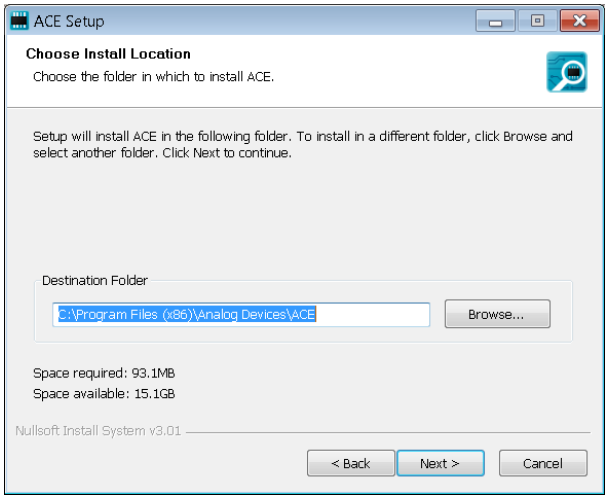

Figure 6. Choose Installation Location

7. The ACE software components to install are preselected (see Figure 7). Click **Install**.

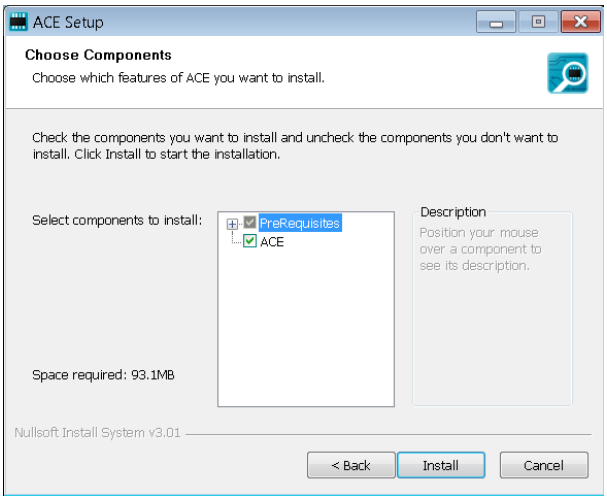

Figure 7. Choose Components

8. The **Windows Security** window opens (see Figure 8). Click **Install**. Figure 9 shows the installation in progress. No action is required.

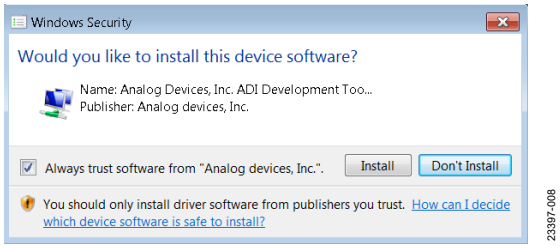

*Figure 8. **Windows Security** Window*

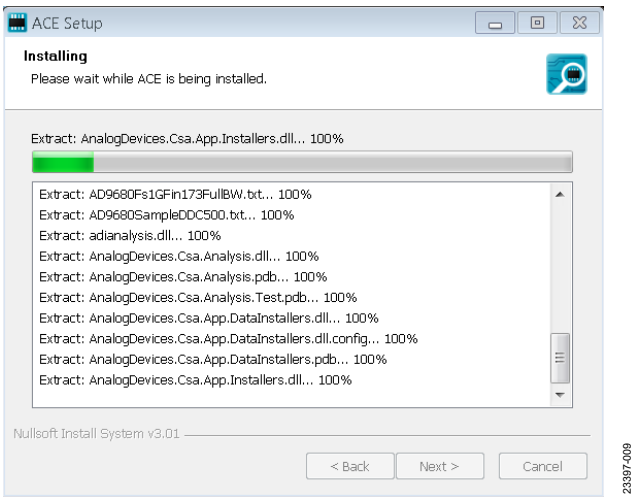

Figure 9. Installation in Progress

9. When the installation is complete, click **Next >** (see Figure 10), and then click **Finish** to complete the installation process.

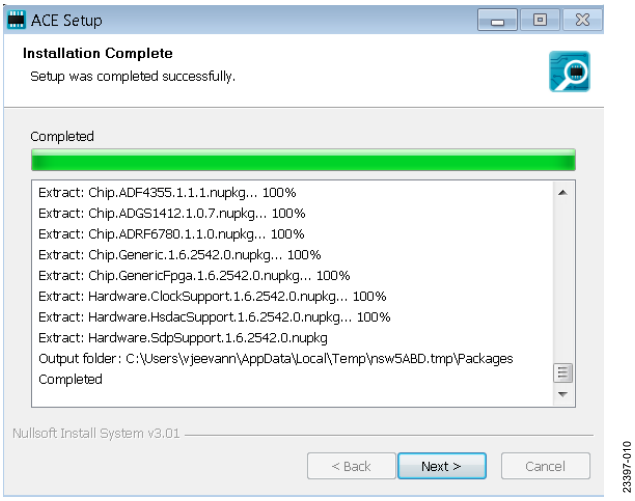

Figure 10. Installation Complete

EVALUATION BOARD SETUP PROCEDURES

The EVAL-AD7383FMCZ connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EVAL-AD7383FMCZ. Figure 2 shows a diagram of the connections between the EVAL-AD7383FMCZ and the SDP-H1.

Connecting the EVAL-AD7383FMCZ and the SDP-H1 to a PC

After the ACE software is installed, take the following steps to set up the EVAL-AD7383FMCZ and the SDP-H1.

1. Ensure that all configuration links are in the appropriate positions, as detailed in Table 2.
2. Connect the EVAL-AD7383FMCZ to the 160-way connector on the SDP-H1. The EVAL-AD7383FMCZ does not require an external power supply adapter.
3. To power up the SDP-H1, insert the 12 V, dc barrel jack (provided in the SDP-H1 kit) into the barrel connector labeled +12V_VIN on the SDP-H1.
4. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

Verifying the Board Connection

After connecting the power and the USB cable from the SDP-H1 to the PC, take the following steps to verify the board connection:

1. After connecting the SDP-H1 to the PC, allow the **Found New Hardware Wizard** to run. Choose to automatically search for the drivers for the SDP-H1 if prompted by the operating system.
2. Navigate to the **Device Manager** window on the PC (see Figure 11).
3. A dialog box may open asking for permission to allow the program to make changes to the computer. Click **Yes**.
4. The **Computer Management** window opens. From the list labeled **System Tools**, click **Device Manager**. If the SDP-H1 driver is installed and the board is properly connected to the PC, **Analog Devices SDP-H1** is shown in the **ADI Development Tools** list in the **Device Manager** window, as shown in Figure 11.

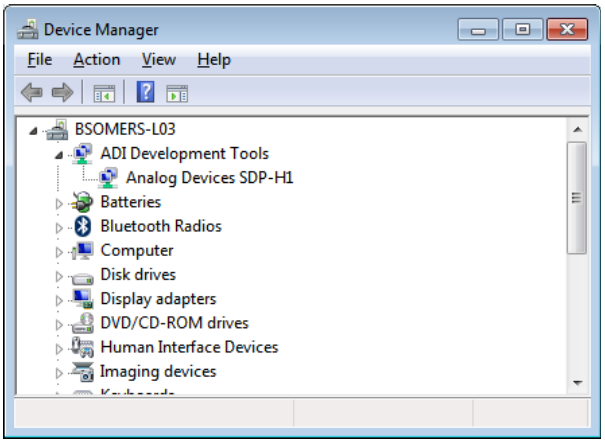

*Figure 11. **Device Manager** Window*

Disconnecting the EVAL-AD7383FMCZ

Disconnect power from the SDP-H1, or press the reset tact switch located alongside the mini USB port on the SDP-H1, before removing the EVAL-AD7383FMCZ from the SDP-H1.

ACE SOFTWARE OPERATION

LAUNCHING THE SOFTWARE

After the EVAL-AD7383FMCZ and SDP-H1 are properly connected to the PC, launch the ACE software by taking the following steps:

1. From the **Start** menu of the PC, select **All Programs > Analog Devices > ACE> ACE.exe** to open the ACE software main window shown in Figure 12.
2. If the EVAL-AD7383FMCZ is not connected to the USB port via the SDP-H1 when the software launches, the **AD7383 Eval Board** icon does not appear in the **Attached Hardware** section in ACE (see Figure 12).To make the **AD7383 Eval Board** icon appear, connect the EVAL-AD7383FMCZ and the SDP-H1 to the USB port of the PC, wait a few seconds, and then follow the instructions in the dialog box that opens.
3. Double click the **AD7383 Eval Board** icon to open the **AD7383 Eval Board** view window shown in Figure 13.
4. Double click the **AD7383** chip icon in the **AD7383 Eval Board** view window to open the **AD7383** chip view window shown in Figure 14.
5. Click **Software Defaults** and then click **Apply Changes** to apply the default settings to the AD7383 (see Figure 14).

DESCRIPTION OF CHIP VIEW WINDOW

After completing the steps in the Software Installation Procedures section and the Evaluation Board Setup Procedures section, set up the system for data capture by taking the following steps:

1. Block icons that are dark blue are programmable blocks. Click a dark blue block icon to open a configurable pop-up window to customize the data capture. Figure 15 shows the **Over Sampling** configurable pop-up window.
2. Click the **REF** block in Figure 16 to access the **Reference Voltage** configurable pop-up window, and select **External** from the **Reference Voltage** dropdown menu. The default value for the external reference is set to 3.3 V and 2.5 V for the internal reference.

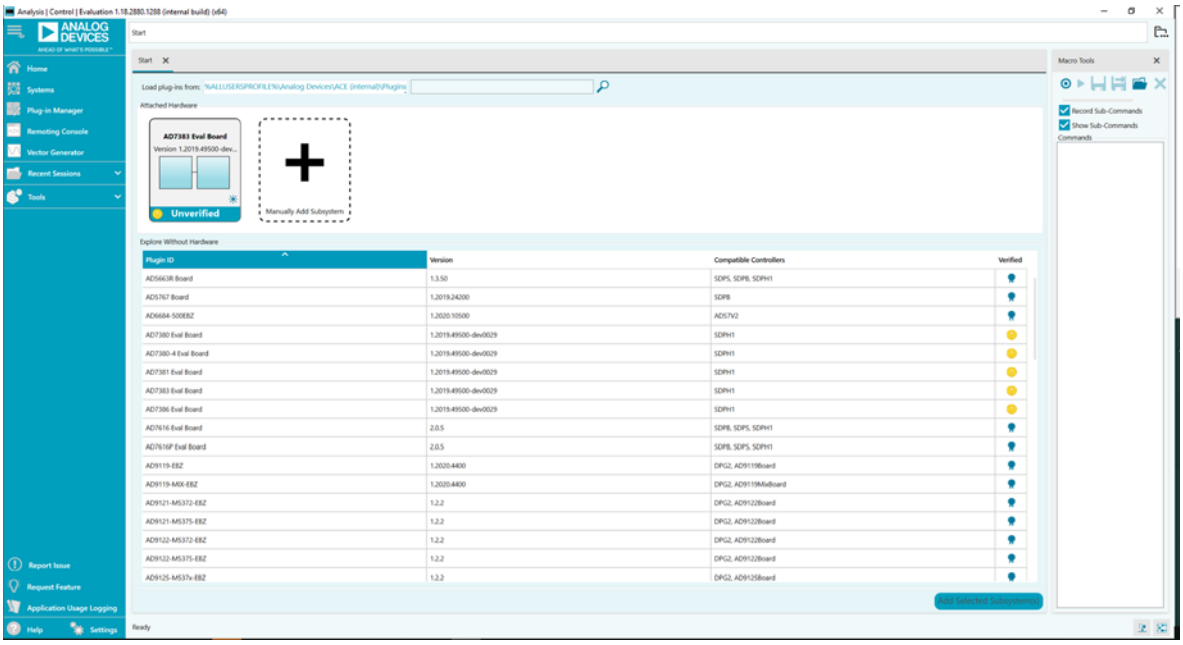

Figure 12. ACE Software Main Window

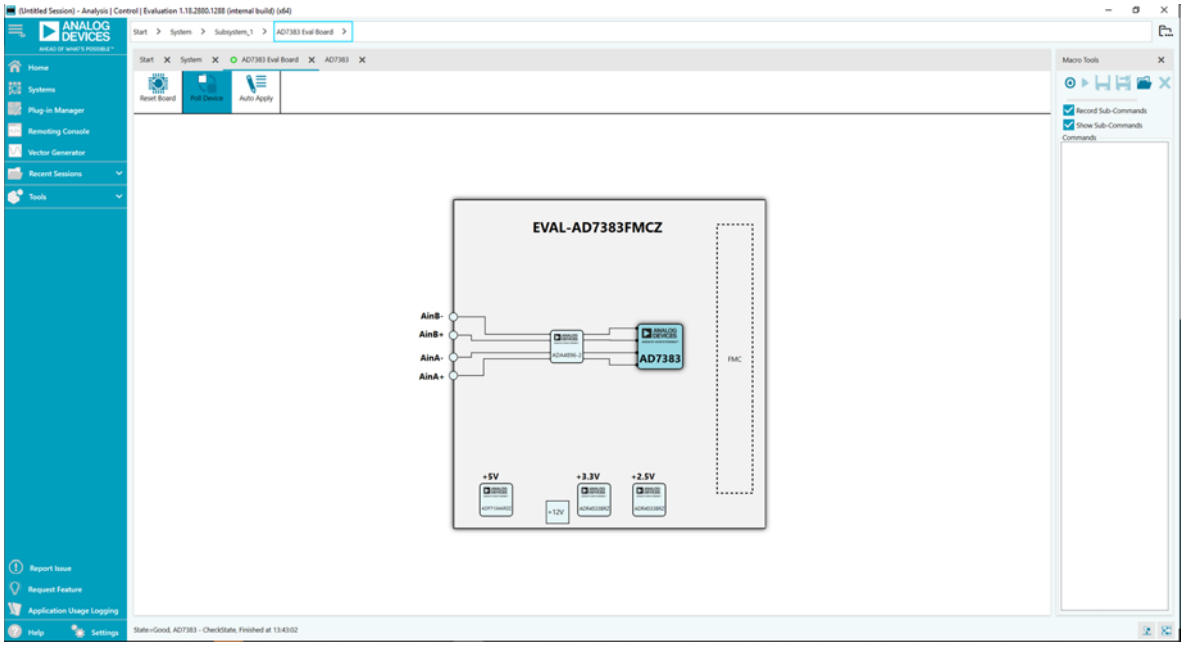

*Figure 13. **AD7383 Eval Board** View Window*

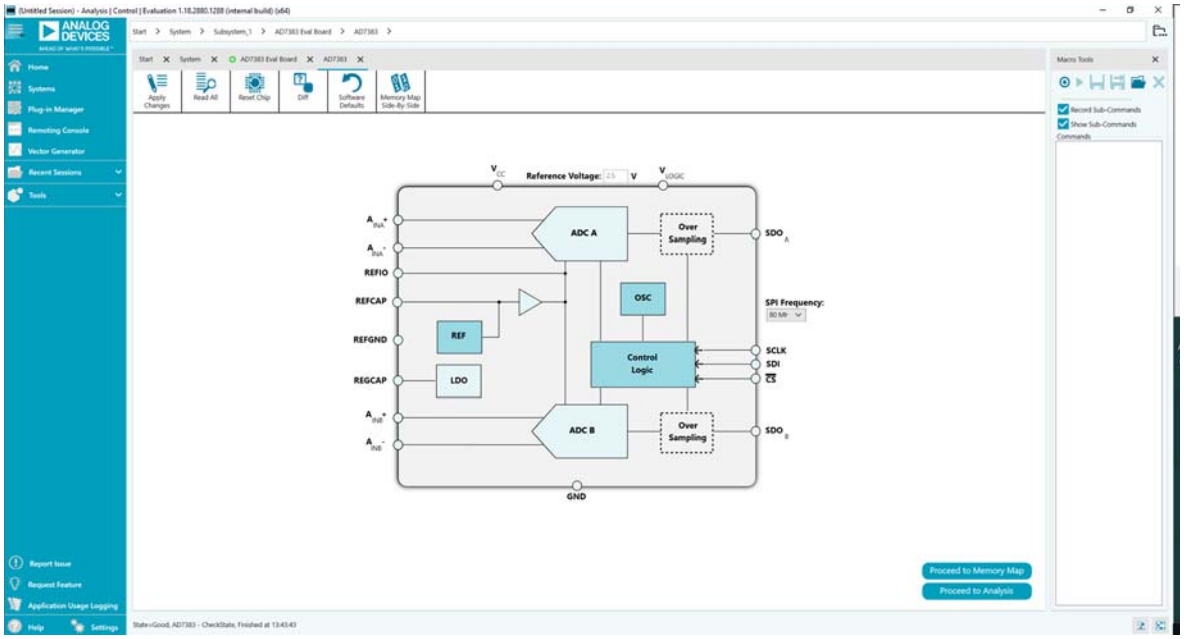

*Figure 14. **AD7383** Chip View Window*

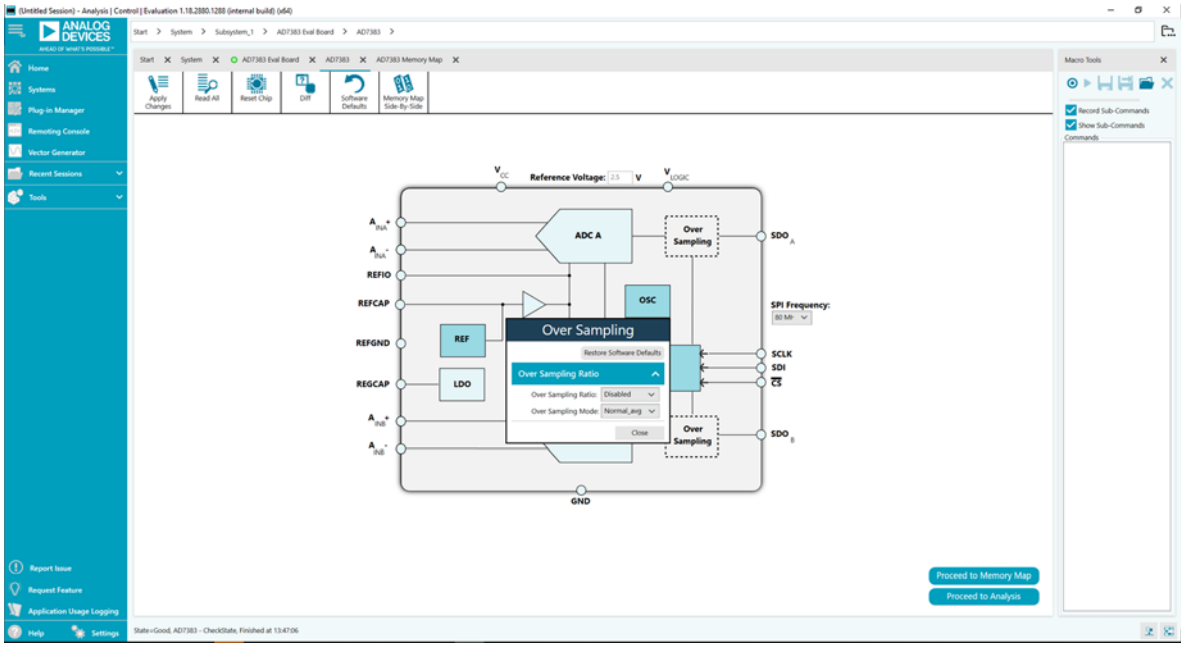

*Figure 15. **Over Sampling** Configurable Pop-Up Window*

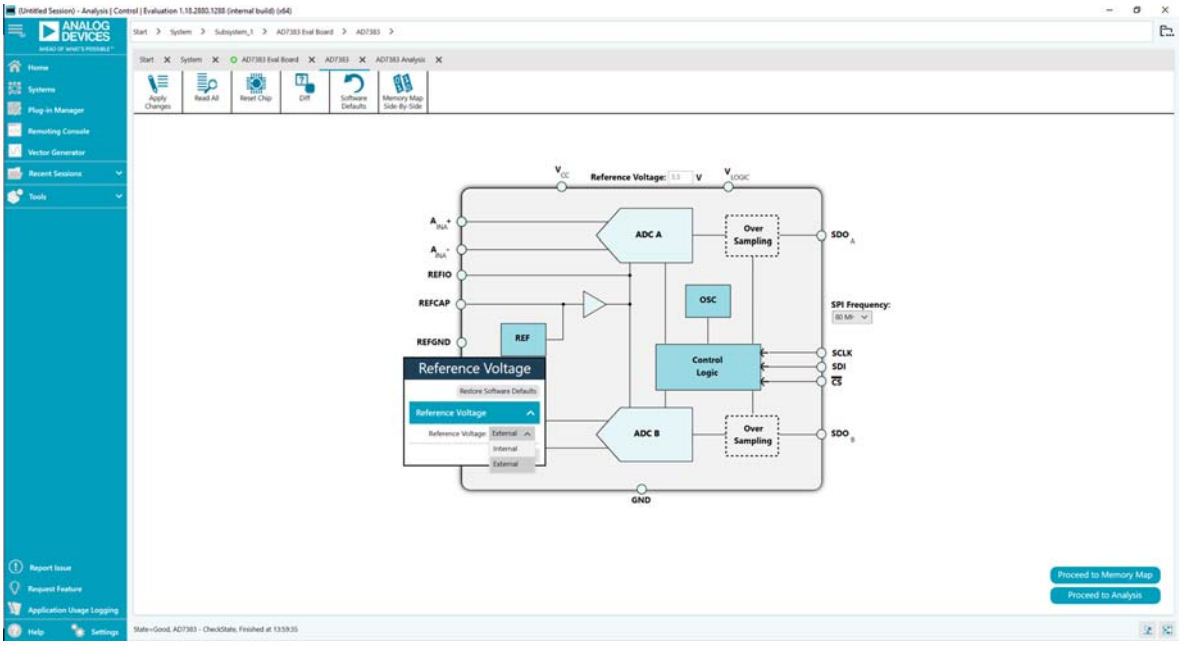

*Figure 16. **Reference Voltage** Configurable Pop-Up Window*

DESCRIPTION OF MEMORY MAP VIEW WINDOW

Click **Proceed to Memory Map** in the **AD7383** chip view window (see Figure 14) to open the **AD7383 Memory Map** view window shown in Figure 17. The **AD7383 Memory Map** view window shows all registers of the AD7383.

The registers of the AD7383 are populated with default values when powered up. To implement the values changed in all of the registers, click **Apply Changes** to write to the registers.

In some cases, the values of every register have been changed, but the user wants to implement changes on a selected register only. Click **Apply Selected** to write the new value on the selected register to the AD7383.

Click **Read All** to read the values of all the registers from the chip.

Click **Read Selected** to read the selected register from the chip.

Click **Reset Chip** to prompt the software to reset the AD7383.

Click **Diff** to check for differences in register values between the software and the chip.

To revert all the register values back to their defaults, click **Software Defaults**, and then click **Apply Changes** to write to the AD7383.

DESCRIPTION OF ANALYSIS VIEW WINDOW

Click **Proceed to Analysis** in the **AD7383** chip view window (see Figure 14) to open the **AD7383 Analysis** view window shown in Figure 18. The **AD7383 Analysis** view window contains the **Waveform** tab, **Histogram** tab, and **FFT** tab.

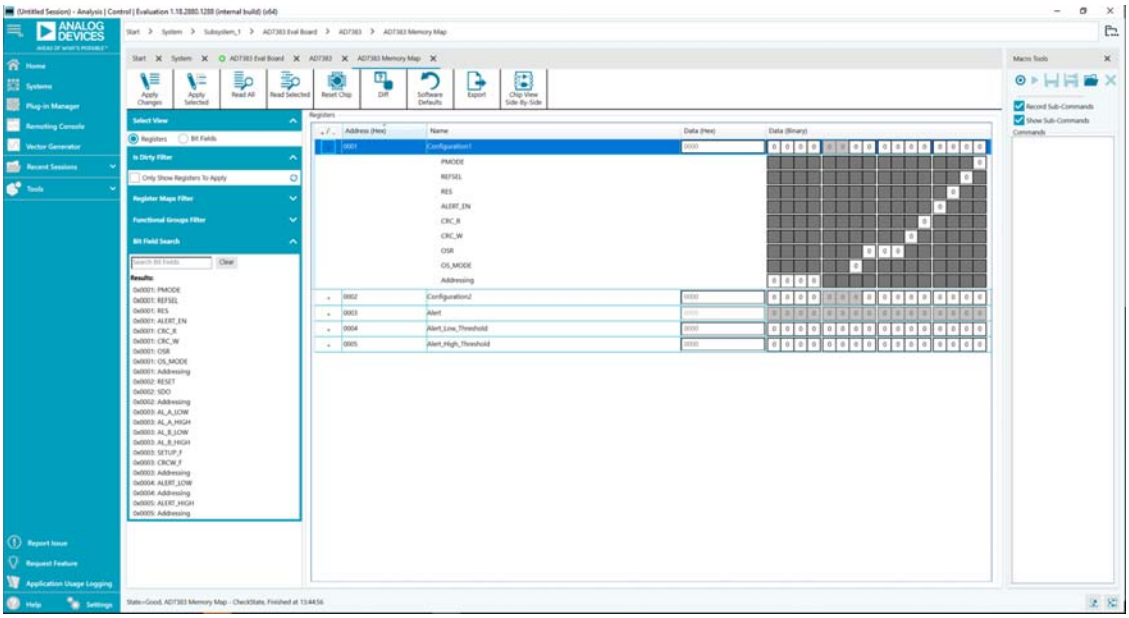

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*Figure 17. **AD7383 Memory Map** View Window*

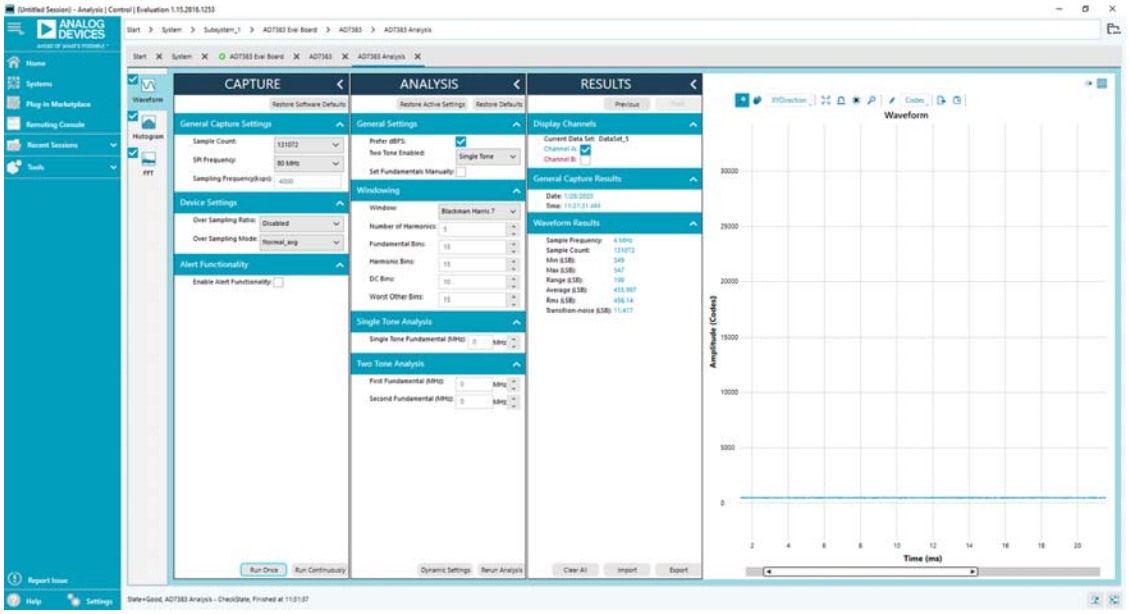

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*Figure 18. **AD7383 Analysis** View Window*

Waveform Tab

The **Waveform** tab displays data in the form of time vs. discrete data values with the results, as shown in Figure 19.

CAPTURE Pane

The **CAPTURE** pane contains the capture settings. These settings reflect onto the registers automatically before data capture.

The **Sample Count** pulldown menu in the **General Capture Settings** section allows the user to select the number of samples per channel per capture (see Figure 19).

The **SPI Frequency** pulldown menu allows the user to select the SPI clock frequency used to transfer data between the FPGA device and the AD7383 during device register reads and writes and during data capture (see Figure 19). This frequency must be set relatively higher than the set throughput rate.

The user can enter the input sample frequency in kSPS in the **Sampling Frequency(ksps)** box (see Figure 19). Refer to the AD7383 data sheet to determine the maximum sampling frequency for the selected mode.

The **Over Sampling Ratio** pulldown menu, when enabled, can be set between 2 and 32 and provide improved signal-to-noise ratio (SNR) performance (see Figure 19). Refer to the AD7383 data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

The **Over Sampling Mode** pulldown menu allows the user to select the mode of oversampling (see Figure 19). This setting is only applicable when oversampling is enabled.

Click **Run Once** to start a data capture of the samples at the sample rate specified in the **Sample Count** pulldown menu (see Figure 19). These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time (see Figure 19). This operation runs the **Run Once** operation continuously.

RESULTS Pane

The **Display Channels** section allows the user to select the channels to capture (see Figure 19). The channel data is shown only if that channel is selected before the capture.

The **Waveform Results** section displays the amplitude, **Sample Frequency**, and noise analysis data for the selected channels (see Figure 19).

Click **Export** to export the captured data (see Figure 19). The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

The data **Waveform** graph shows each successive sample of the ADC output (see Figure 19). The user can zoom in on and pan over the **Waveform** graph using the embedded waveform tools above the graph. Select the channels to display in the **Display Channels** section.

Under the **Display Units** dropdown menu, select **Codes** above the **Waveform** graph (see Figure 19) to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

When either **y-scale dynamic** or **x-scale dynamic** is selected, the corresponding axis width automatically adjusts to show the entire range of the ADC results after each batch of samples.

Histogram Tab

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 20.

The **RESULTS** pane displays the information related to the dc performance.

The **Histogram** graph displays the number of hits per code within the sampled data (see Figure 20). The **Histogram** graph is useful for dc analysis and indicates the noise performance of the AD7383.

FFT Tab

The **FFT** tab displays fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 21).

ANALYSIS Pane

The **General Settings** section allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed (see Figure 21). The fundamental is set manually.

The **Windowing** section allows the user to select the windowing type used in the FFT analysis, the number of **Harmonic Bins**, and the number of **Fundamental Bins** that must be included (see Figure 21).

The **Single Tone Analysis** and **Two Tone Analysis** sections allow the user to select the fundamental frequency included in the FFT analysis (see Figure 21). Use the **Two Tone Analysis** settings when analyzing two frequencies.

RESULTS Pane

The **Signal** section displays the **Sample Frequency**, **Fund Frequency**, and **Fund Power** (see Figure 21).

The **Noise** section displays the **SNR** and other noise performance results (see Figure 21).

The **Distortion** section displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis (see Figure 21).

EXITING THE SOFTWARE

To exit the ACE software, click **File** and then click **Exit**.

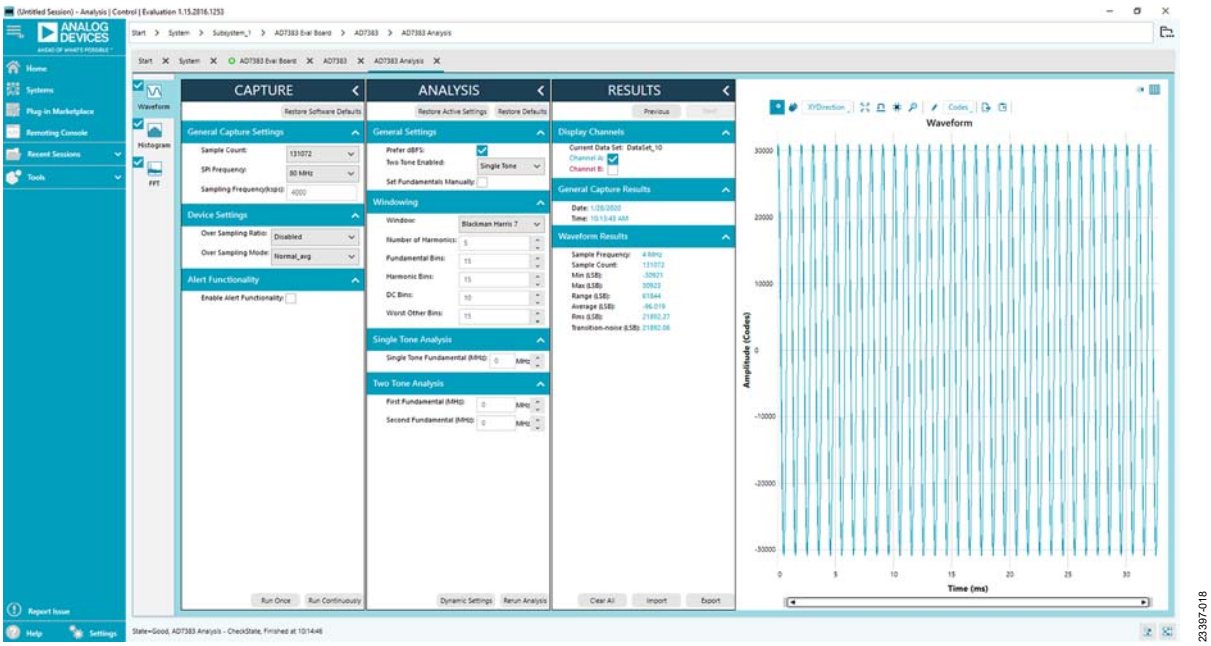

*Figure 19. **Waveform** Tab*

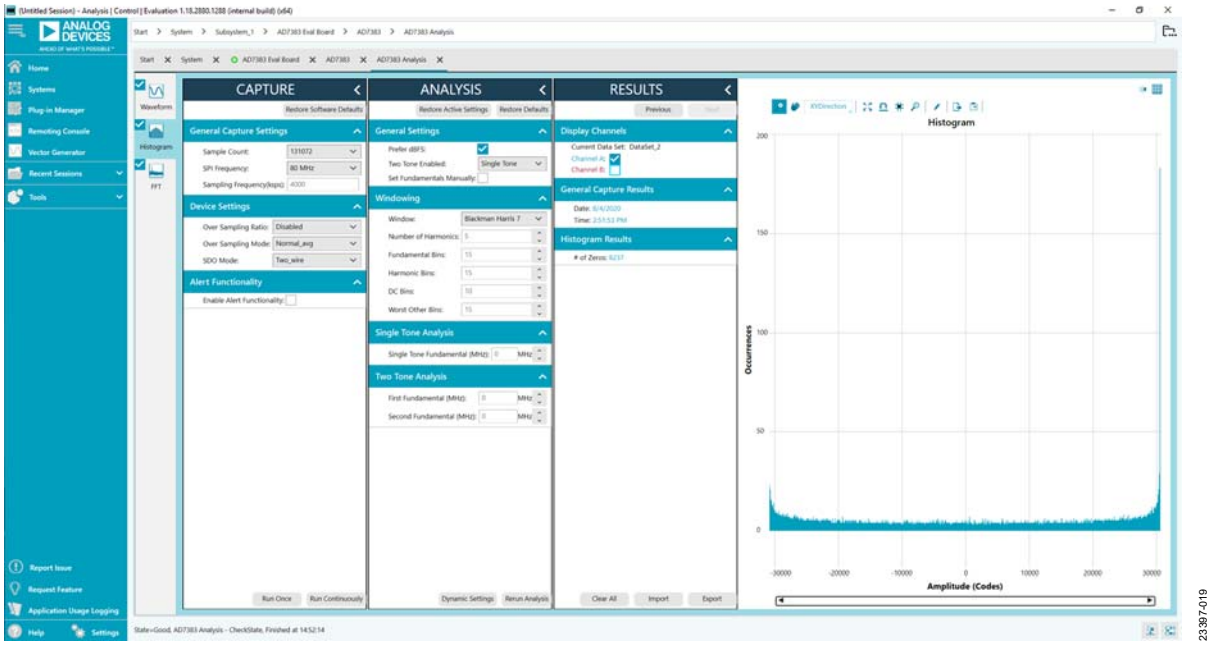

*Figure 20. **Histogram** Tab*

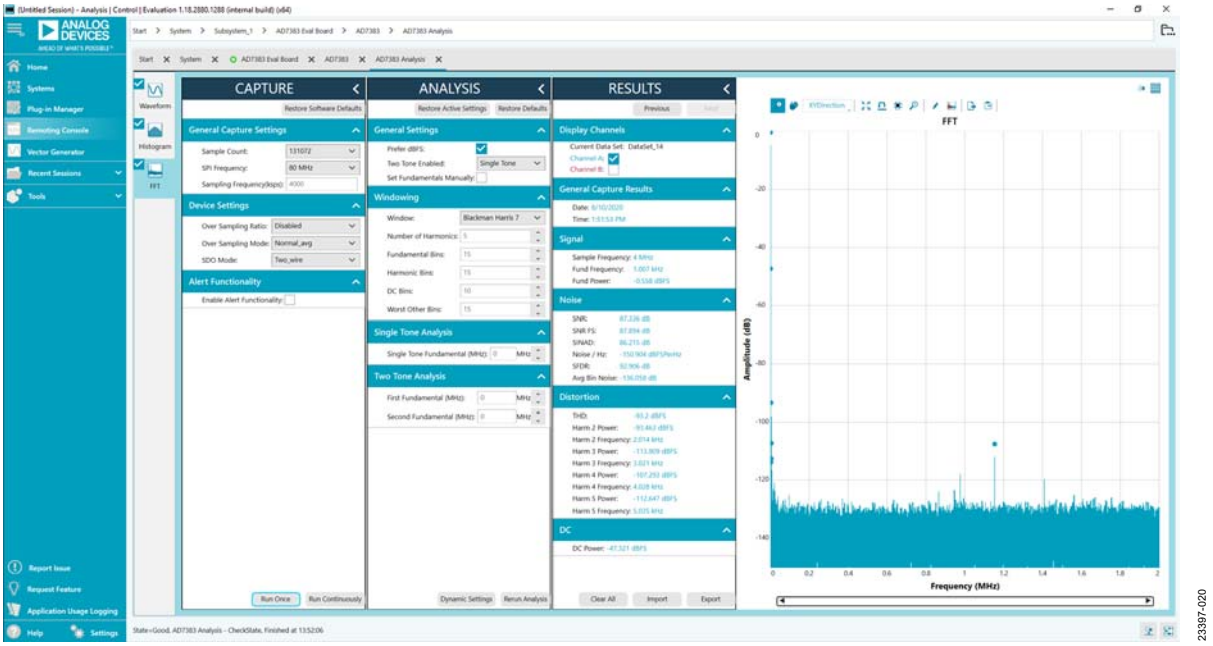

*Figure 21. **FFT** Tab*

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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