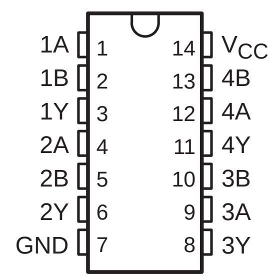
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

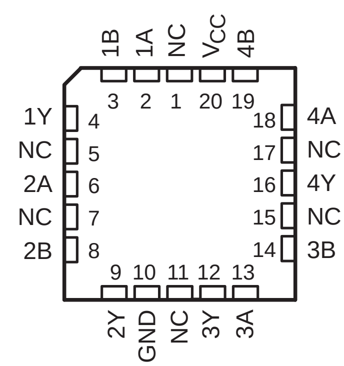
These devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC00 is characterized for operation from –40°C to 85°C.

SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC00 . . . FK PACKAGE
(TOP VIEW)

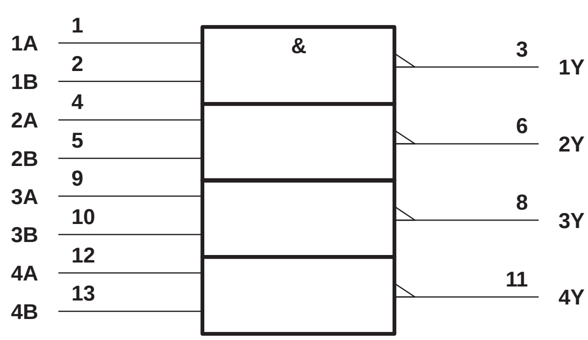


NC – No internal connection

FUNCTION TABLE
(each gate)

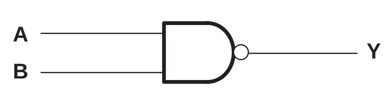
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 127°C/W
N package . . . . 78°C/W
PW package . . . . 170°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC00			SN74HC00			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54HC00 MIN	SN54HC00 MAX	SN74HC00 MIN	SN74HC00 MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

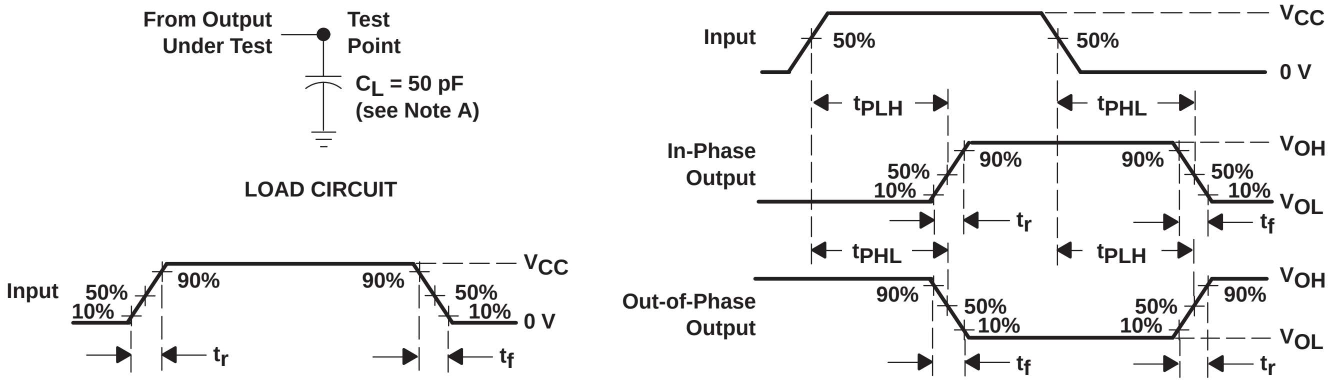
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54HC00 MIN	SN54HC00 MAX	SN74HC00 MIN	SN74HC00 MAX	UNIT
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

SN54HC00, Quadruple 2-Input Positive-NAND Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HC00
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
No. of Gates	4

FEATURES

Back to Top

- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

DESCRIPTION

Back to Top

These devices contain four independent 2-input NAND gates. They perform the Boolean function Y = A \•\ B\ or Y = A\ + B\ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC00 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: scls181b.pdf (76 KB) (Updated: 05/01/1997)
Full datasheet in Zipped PostScript: scls181b.psz (76 KB)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- CMOS Power Consumption And CPD Calculation (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (SDYA009C - Updated: 06/01/1997)
- HCMOS Design Considerations (SCLA007 - Updated: 04/01/1996)
- Implications of Slow or Floating CMOS Inputs (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications And Restrictions (SCLA011 - Updated: 05/01/1996)
- Using High Speed CMOS And Advanced CMOS In Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

Back to Top

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

PRICING/AVAILABILITY

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (ºC)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	DSCC NUMBER	PRICING/AVAILABILITY
84037012A	FK	20	-55 TO 125	ACTIVE	6.71	1		Check stock or order
8403701DA	W	14	-55 TO 125	ACTIVE	8.29	1		Check stock or order
JM38510/65001B2A	FK	20	-55 TO 125	ACTIVE	7.65	1		Check stock or order
JM38510/65001BCA	J	14	-55 TO 125	ACTIVE	3.93	1		Check stock or order
JM38510/65001BDA	W	14	-55 TO 125	ACTIVE	9.30	1		Check stock or order
SN54HC00J	J	14	-55 TO 125	ACTIVE	0.87	1		Check stock or order
SNJ54HC00FK	FK	20	-55 TO 125	ACTIVE	6.71	1	84037012A	Check stock or order
SNJ54HC00J	J	14	-55 TO 125	ACTIVE	1.03	1		Check stock or order
			-55					

SNJ54HC00W	W	14	TO 125	ACTIVE	8.29	1	8403701DA	Check stock or order

Table Data Updated on: 11/10/2000

SN74HC00, Quadruple 2-Input Positive-NAND Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74HC00
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	-4/4
No. of Gates	4
Static Current	0.02
tpd(max) (ns)	20

FEATURES

Back to Top

- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

DESCRIPTION

Back to Top

These devices contain four independent 2-input NAND gates. They perform the Boolean function Y = A \•\ B\ or Y = A\ + B\ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC00 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: scls181b.pdf (76 KB) (Updated: 05/01/1997)

Full datasheet in Zipped PostScript: scls181b.psz (76 KB)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- CMOS Power Consumption and CPD Calculation (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (SDYA009C - Updated: 06/01/1997)
- HCMOS Design Considerations (SCLA007 - Updated: 04/01/1996)
- Implications of Slow or Floating CMOS Inputs (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications And Restrictions (SCLA011 - Updated: 05/01/1996)
- Using High Speed CMOS and Advanced CMOS In Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

Back to Top

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

PRICING/AVAILABILITY

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (ºC)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
SN74HC00ADBLE	DB	14	-40 TO 85	OBSOLETE			
SN74HC00ADBR	DB	14	-40 TO 85	NRND	0.33	2000	Check stock or order
SN74HC00D	D	14	-40 TO 85	ACTIVE	0.25	50	Check stock or order
SN74HC00DR	D	14	-40 TO 85	ACTIVE	0.28	2500	Check stock or order
SN74HC00N	N	14	-40 TO 85	ACTIVE	0.23	25	Check stock or order
SN74HC00N3	N	14	-40 TO 85	OBSOLETE			
SN74HC00NSR	NS	14	-40 TO 85	ACTIVE	0.33	2000	Check stock or order
SN74HC00PWLE	PW	14	-40 TO 85	OBSOLETE			
SN74HC00PWR	PW	14	-40 TO 85	ACTIVE	0.25	2000	Check stock or order

Table Data Updated on: 11/15/2000