

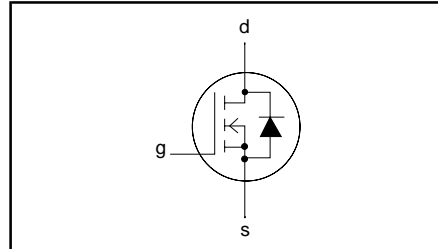
N-channel TrenchMOS™ transistor

**PHP18NQ10T, PHB18NQ10T
PHD18NQ10T**

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 100\text{ V}$
$I_D = 18\text{ A}$
$R_{DS(ON)} \leq 90\text{ m}\Omega$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology.

Applications:-

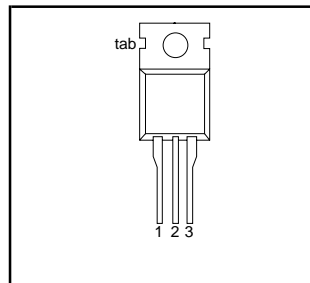
- d.c. to d.c. converters
- switched mode power supplies

The PHP18NQ10T is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB18NQ10T is supplied in the SOT404 (D²PAK) surface mounting package.
The PHD18NQ10T is supplied in the SOT428 (DPAK) surface mounting package.

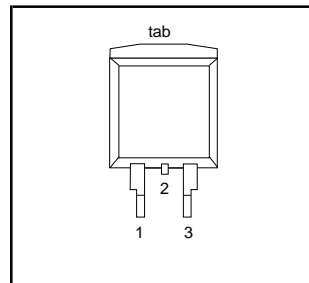
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

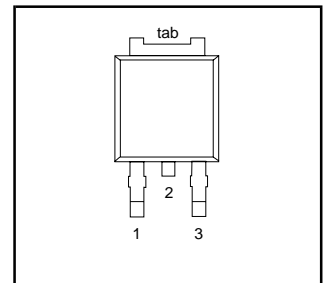
SOT78 (TO220AB)



SOT404 (D²PAK)



SOT428 (DPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	18	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	13	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	72	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	79	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.

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PHP18NQ10T, PHB18NQ10T
PHD18NQ10T**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 11$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig:15	-	70	mJ
I_{AS}	Peak non-repetitive avalanche current		-	18	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	SOT78 package, in free air SOT404 & SOT428 packages, pcb mounted, minimum footprint	-	-	1.9	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	60	-	K/W
			-	50	-	K/W

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$	100 89	-	-	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2 1	3	4	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 9$ A $T_j = 175^\circ\text{C}$	-	80	90	m Ω m Ω
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$ V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100$ V; $V_{GS} = 0$ V $T_j = 175^\circ\text{C}$	-	0.05	10	μ A μ A
$Q_{g(tot)}$	Total gate charge	$I_D = 18$ A; $V_{DD} = 80$ V; $V_{GS} = 10$ V	-	21	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	8	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 50$ V; $R_D = 2.7$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load	-	6	-	ns
t_r	Turn-on rise time		-	36	-	ns
t_{doff}	Turn-off delay time		-	18	-	ns
t_f	Turn-off fall time		-	12	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	633	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	61	-	pF

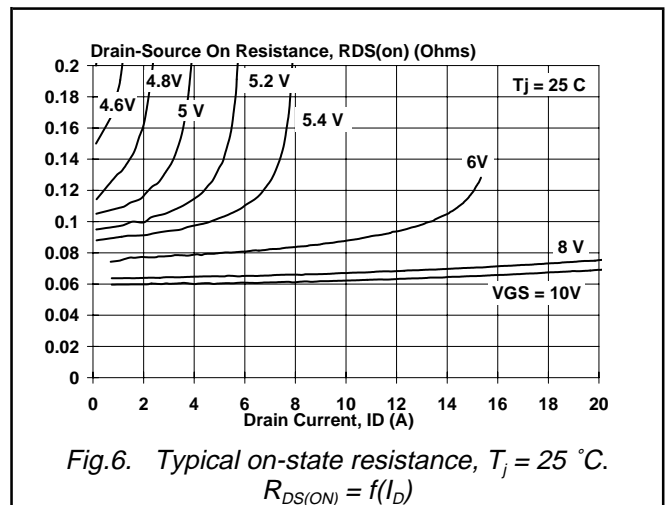
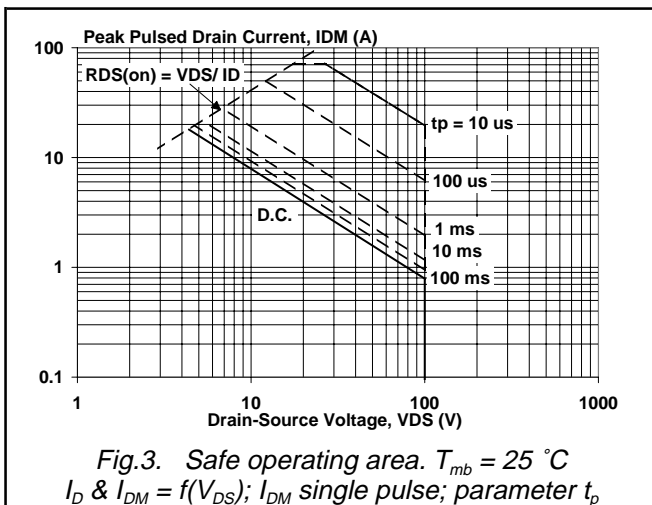
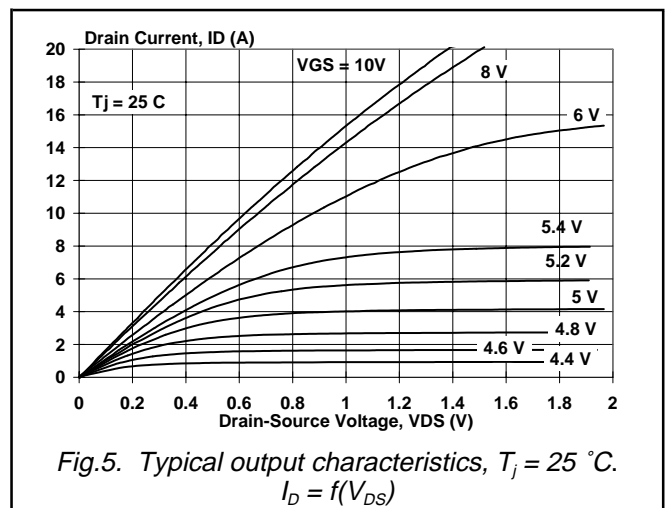
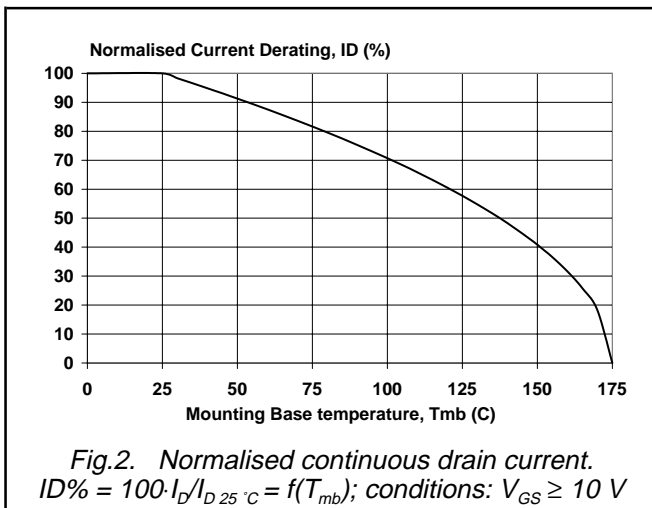
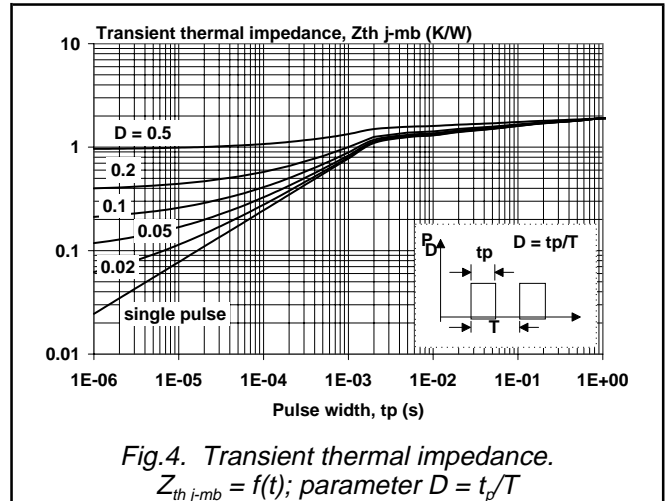
N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	18	A
I_{SM}	Pulsed source current (body diode)		-	-	72	A
V_{SD}	Diode forward voltage	$I_F = 18\text{ A}; V_{GS} = 0\text{ V}$	-	0.92	1.2	V
t_{rr}	Reverse recovery time	$I_F = 18\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 25\text{ V}$	-	55	-	ns
Q_{rr}	Reverse recovery charge		-	135	-	nC

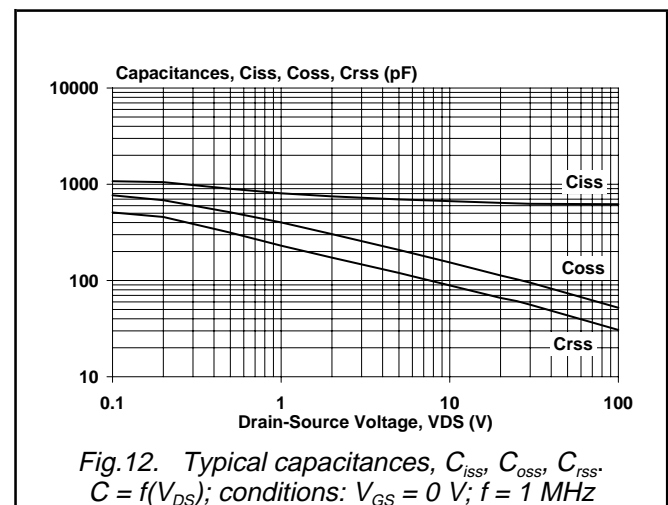
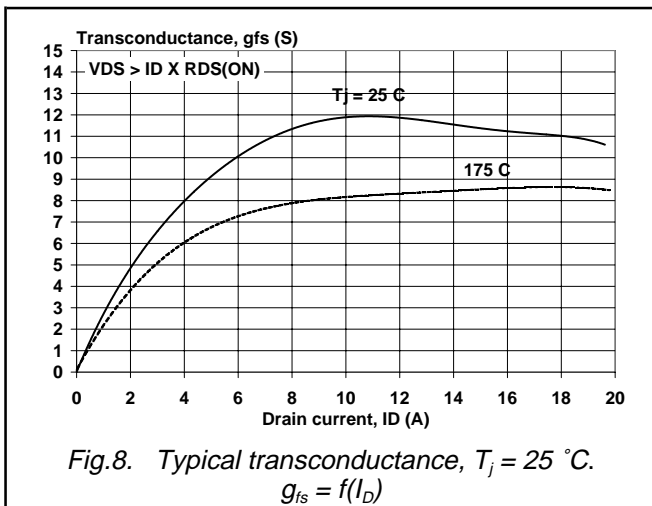
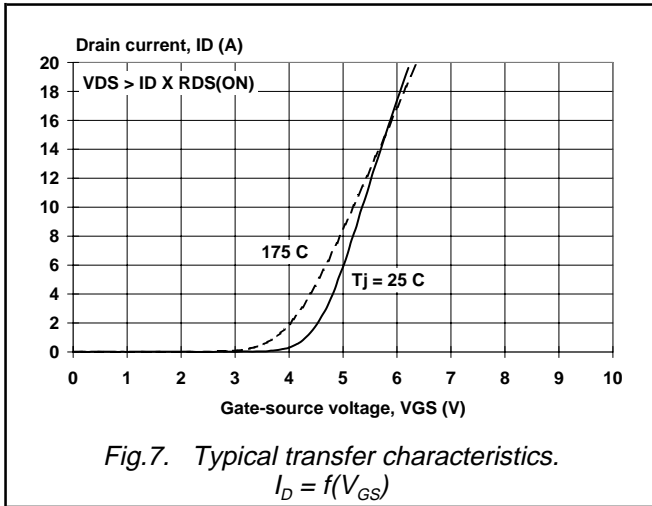
N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T



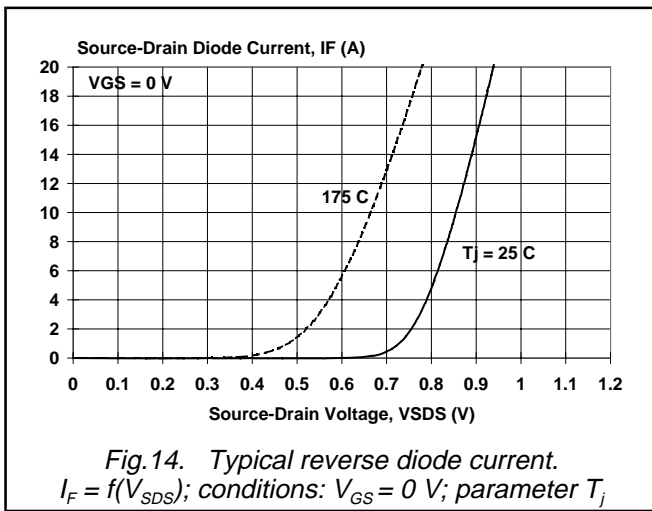
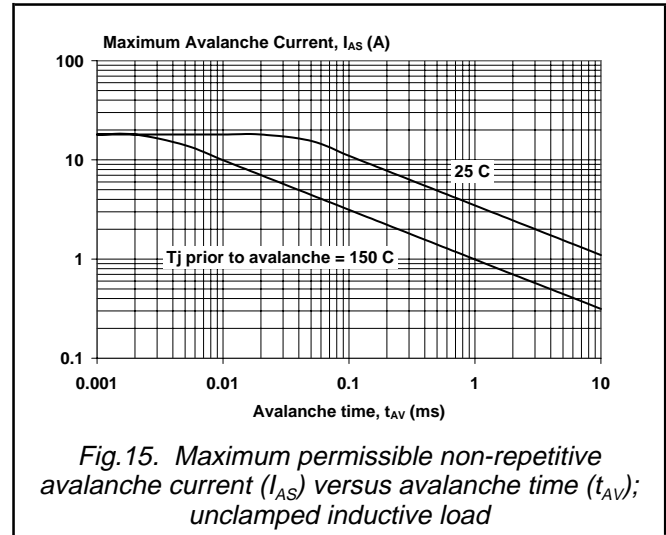
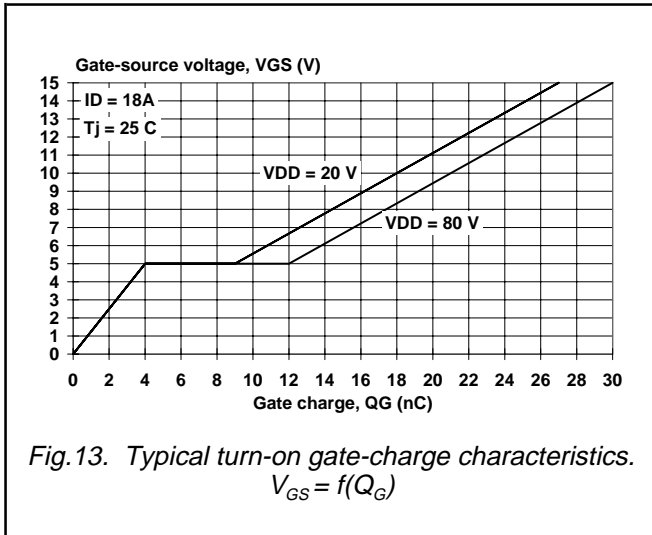
N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T



N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T



N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T

MECHANICAL DATA



Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

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PHP18NQ10T, PHB18NQ10T
PHD18NQ10T

MECHANICAL DATA



Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
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MOUNTING INSTRUCTIONS

Dimensions in mm



Fig.18. SOT404 : soldering pattern for surface mounting.

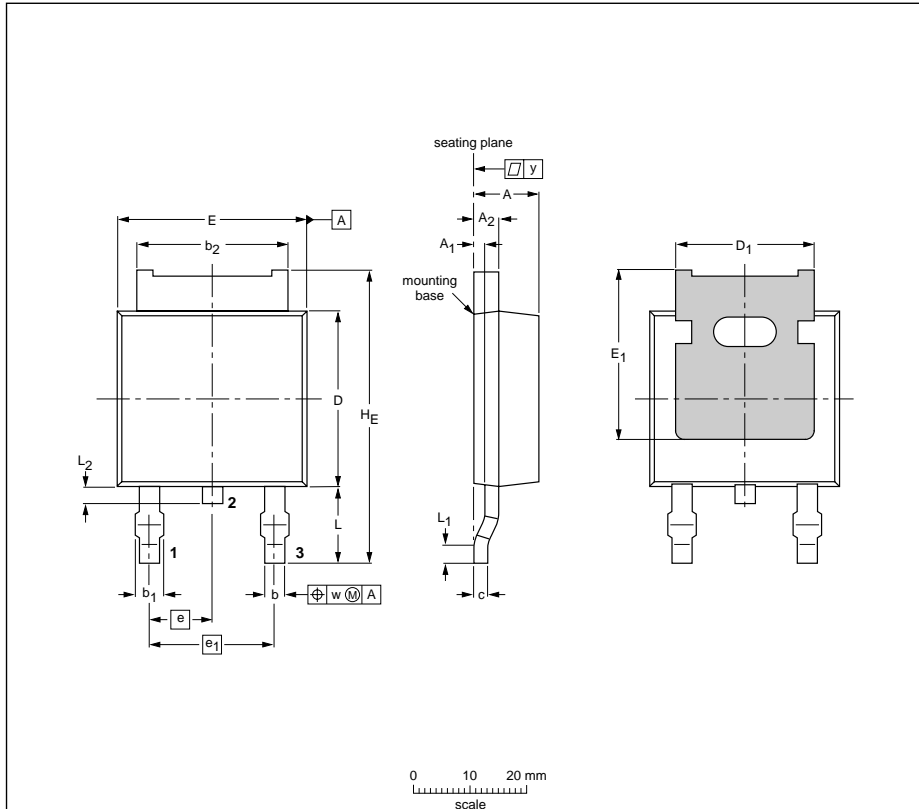
N-channel TrenchMOS™ transistor

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MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁ ⁽¹⁾	A ₂	b	b ₁ max.	b ₂	c	D max.	D ₁ max.	E max.	E ₁ min.	e	e ₁	H _E max.	L	L ₁ min.	L ₂	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						98-04-07

Fig.19. SOT428 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T

MOUNTING INSTRUCTIONS

Dimensions in mm

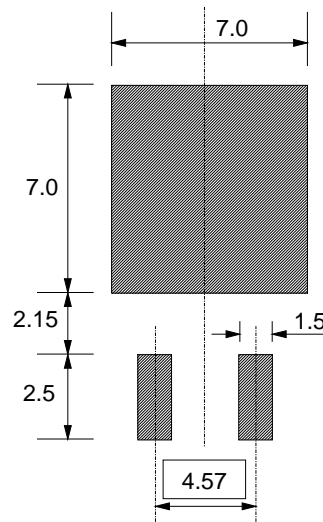


Fig.20. SOT428 : soldering pattern for surface mounting.

N-channel TrenchMOS™ transistor

PHP18NQ10T, PHB18NQ10T
PHD18NQ10T**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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