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# LMH6732

## High Speed Op Amp with Adjustable Bandwidth

### General Description

The LMH6732 is a high speed op amp with a unique combination of high performance, low power consumption, and flexibility of application. The supply current is adjustable, over a continuous range of more than 10 to 1, with a single resistor,  $R_P$ . This feature allows the device to be used in a wide variety of high performance applications including device turn on/ turn off (Enable/ Disable) for power saving or multiplexing. Typical performance at any supply current is exceptional. The LMH6732's design has been optimized so that the output is well behaved, eliminating spurious outputs on "Enable".

The LMH6732's combination of high performance, low power consumption, and large signal performance makes it ideal for a wide variety of remote site equipment applications such as battery powered test instrumentation and communications gear. Other applications include video switching matrices, ATE and phased array radar systems.

The LMH6732 is available in the SOIC and SOT23-6 packages. To reduce design times and assist in board layout, the LMH6732 is supported by an evaluation board.

### Features

- Exceptional Performance at any Supply Current:  
 $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $A_V = +2V/V$ ,  $V_{OUT} = 2V_{PP}$ , Typical unless Noted:

$I_{CC}$ (mA)	-3dB BW (MHz)	DG/DP (%/deg.) PAL	Slew Rate (V/ $\mu$ s)	THD 1MHz (dBc)	Output Current (mA)
1.0	55	0.020/ 0.036	400	-70.0	9
3.4	180	0.022 / 0.017	2100	-78.5	45
9.0	540	0.025 / 0.010	2700	-79.6	115

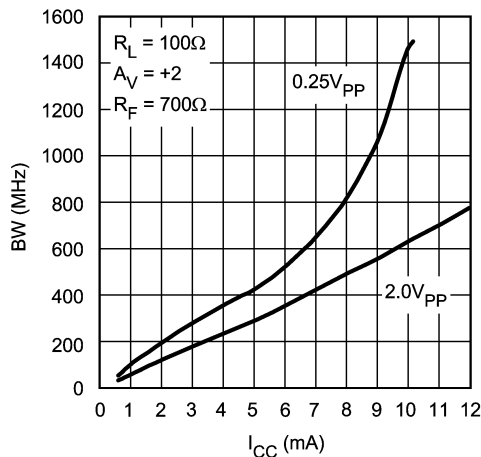
- Ultra High Speed (-3dB BW) 1.5GHz ( $I_{CC} = 10mA$ ,  $0.25V_{PP}$ )
- Single resistor adjustability of supply current
- Fast enable/ disable capability 20ns ( $I_{CC} = 9mA$ )
- "Popless" output on "Enable" 15mV ( $I_{CC} = 1mA$ )
- Ultra low disable current <1 $\mu$ A
- Unity gain stable
- Improved Replacement for CLC505 & CLC449

### Applications

- Battery powered systems
- Video switching and distribution
- Remote site instrumentation
- Mobile communications gear

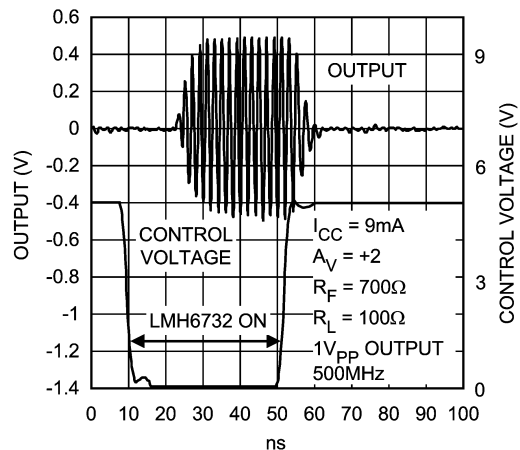
LMH6732 High Speed Op Amp with Adjustable Bandwidth

-3dB BW vs.  $I_{CC}$



20060262

Turn-On/Off Characteristics



20060250

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_S$	±6.75V
$I_{OUT}$	(Note 3)
$I_{CC}$	14mA
Common Mode Input Voltage	$V^-$ to $V^+$
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C
ESD Tolerance (Note 4)	

Human Body Model	2000V
Machine Model	200V

**Operating Ratings** (Note 1)

Thermal Resistance		
Package	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (°C/W)
8-Pin SOIC	65°C/W	166°C/W
6-Pin SOT23	120°C/W	198°C/W
Operating Temperature	-40°C to +85°C	
Nominal Supply Voltage	±4.5V to ±6V	
Operating Supply Current	0.5mA < $I_{CC}$ < 12mA	

**Electrical Characteristics  $I_{CC} = 9mA$**  (Note 2)

$A_V = +2$ ,  $R_F = 700\Omega$ ,  $V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_P = 39k\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
<b>Frequency Domain Response</b>						
SSBW	-3dB Bandwidth	$V_{OUT} = 2V_{PP}$		540		MHz
LSBW	-3dB Bandwidth	$V_{OUT} = 4.0V_{PP}$		315		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	$V_{OUT} = 2V_{PP}$		180		MHz
GFP	Frequency Response Peaking	DC to 200MHz, $V_{OUT} = 2V_{PP}$		0.01		dB
GFR	Frequency Response Rolloff	DC to 200MHz, $V_{OUT} = 2V_{PP}$		0.15		dB
LPD	Linear Phase Deviation	DC to 200MHz, $V_{OUT} = 2V_{PP}$		0.6		deg
		DC to 140MHz, $V_{OUT} = 2V_{PP}$		0.1		
DG	Differential Gain	$R_L = 150\Omega$ , 4.43MHz		0.025		%
DP	Differential Phase	$R_L = 150\Omega$ , 4.43MHz		0.010		deg
<b>Time Domain Response</b>						
TRS	Rise Time	2V Step		0.8		ns
TRL	Fall Time	2V Step		0.9		
$T_S$	Settling Time to 0.04%	$A_V = -1$ , 2V Step		18		ns
OS	Overshoot	2V Step		1		%
SR	Slew Rate	5V Step, 40% to 60% (Note 5)		2700		V/ $\mu$ s
<b>Distortion And Noise Response</b>						
HD2	2nd Harmonic Distortion	$2V_{PP}$ , 20MHz		-60		dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$ , 20MHz		-64		dBc
THD	Total Harmonic Distortion	$2V_{PP}$ , 1MHz		-79.6		dBc
$V_N$	Input Referred Voltage Noise	>1MHz		2.5		nV/ $\sqrt{Hz}$
$I_N$	Input Referred Inverting Noise Current	>1MHz		9.7		pA/ $\sqrt{Hz}$
$I_{NN}$	Input Referred Non-Inverting Noise Current	>1MHz		1.8		pA/ $\sqrt{Hz}$
SNF	Noise Floor	>1MHz		-154		dBm <sub>1Hz</sub>
INV	Total Integrated Input Noise	1MHz to 200MHz		60		$\mu$ V
<b>Static, DC Performance</b>						
$V_{IO}$	Input Offset Voltage			±3.0	±8.0 9.9	mV
$DV_{IO}$	Input Offset Voltage Average Drift	(Note 8)		16		$\mu$ V/°C

**Electrical Characteristics  $I_{CC} = 9\text{mA}$**  (Note 2) (Continued) $A_V = +2$ ,  $R_F = 700\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 100\Omega$ ,  $R_P = 39\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
$I_{BN}$	Input Bias Current	Non Inverting (Note 7)		-2	$\pm 11$ <b><math>\pm 12</math></b>	$\mu\text{A}$
$DI_{BN}$	Input Bias Current Average Drift	Non-Inverting (Note 8)		5		$\text{nA}/^\circ\text{C}$
$I_{BI}$	Input Bias Current	Inverting (Note 7)		-9	$\pm 20$ <b><math>\pm 30</math></b>	$\mu\text{A}$
$DI_{BI}$	Input Bias Current Average Drift	Inverting (Note 8)		-14		$\text{nA}/^\circ\text{C}$
+PSRR	Positive Power Supply Rejection Ratio	DC	52 <b>50</b>	62		dB
-PSRR	Negative Power Supply Rejection Ratio	DC	51 <b>48</b>	56		dB
CMRR	Common Mode Rejection Ratio	DC	49 <b>46</b>	52		dB
$I_{CC}$	Supply Current	$R_L = \infty$ , $R_P = 39\text{k}\Omega$	7.5 <b>6.6</b>	9.0	10.5 <b>11.7</b>	mA
$I_{CC}^I$	Supply Current During Shutdown			<1		$\mu\text{A}$
<b>Miscellaneous Performance</b>						
$R_{IN}$	Input Resistance	Non-Inverting		4.7		$\text{M}\Omega$
$C_{IN}$	Input Capacitance	Non-Inverting		1.8		pF
$R_{OUT}$	Output Resistance	Closed Loop		32		$\text{m}\Omega$
$V_O$	Output Voltage Range	$R_L = \infty$	$\pm 3.60$ <b><math>\pm 3.55</math></b>	$\pm 3.75$		V
$V_{OL}$		$R_L = 100\Omega$	$\pm 2.90$ <b><math>\pm 2.85</math></b>	$\pm 3.10$		
CMIR	Common Mode Input Range	Common Mode		$\pm 2.2$		V
$I_O$	Output Current	Closed Loop $-40\text{mV} \leq V_O \leq 40\text{mV}$	$\pm 75$	$\pm 115$		mA
TON	Turn-on Time	0.5 $V_{PP}$ Sine Wave, 90% of Full Value		20		ns
TOFF	Turn-off Time	0.5 $V_{PP}$ Sine Wave, <5% of Full Value		9		
$V_{O\_glitch}$	Turn-on Glitch			50		mV
FDTH	Feed-Through	$f = 10\text{MHz}$ , $A_V = +2$ , Off State		-61		dB

**Electrical Characteristics  $I_{CC} = 3.4\text{mA}$**  (Note 2) $A_V = +2$ ,  $R_F = 1\text{k}\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 100\Omega$ ,  $R_P = 137\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
<b>Frequency Domain Response</b>						
SSBW	-3dB Bandwidth	$V_{OUT} = 2V_{PP}$		180		MHz
LSBW	-3dB Bandwidth	$V_{OUT} = 4.0V_{PP}$		100		MHz
$GF_{0.1\text{dB}}$	0.1dB Gain Flatness	$V_{OUT} = 2V_{PP}$		50		MHz
GFP	Frequency Response Peaking	DC to 75MHz, $V_{OUT} = 2V_{PP}$		0.15		dB
GFR	Frequency Response Rolloff	DC to 75MHz, $V_{OUT} = 2V_{PP}$		0.05		dB
LPD	Linear Phase Deviation	DC to 55MHz, $V_{OUT} = 2V_{PP}$		0.5		deg
		DC to 25MHz, $V_{OUT} = 2V_{PP}$		0.1		
DG	Differential Gain	$R_L = 150\Omega$ , 4.43MHz		0.022		%
DP	Differential Phase	$R_L = 150\Omega$ , 4.43MHz		0.017		deg
<b>Time Domain Response</b>						

**Electrical Characteristics  $I_{CC} = 3.4\text{mA}$**  (Note 2) (Continued) $A_V = +2$ ,  $R_F = 1\text{k}\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 100\Omega$ ,  $R_P = 137\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
TR <sub>S</sub>	Rise Time	2V Step		1.7		ns
TR <sub>L</sub>	Fall Time	2V Step		2.1		
T <sub>S</sub>	Settling Time to 0.04%	$A_V = -1$ , 2V Step		18		ns
OS	Overshoot	2V Step		2		%
SR	Slew Rate	5V Step, 40% to 60% (Note 5)		2100		V/ $\mu\text{s}$
<b>Distortion And Noise Response</b>						
HD <sub>2</sub>	2nd Harmonic Distortion	2V <sub>PP</sub> , 10MHz		-51		dBc
HD <sub>3</sub>	3rd Harmonic Distortion	2V <sub>PP</sub> , 10MHz		-65		dBc
THD	Total Harmonic Distortion	2V <sub>PP</sub> , 1MHz		-78.5		dBc
V <sub>N</sub>	Input Referred Voltage Noise	>1MHz		4.1		nV/ $\sqrt{\text{Hz}}$
I <sub>N</sub>	Input Referred Inverting Noise Current	>1MHz		8.8		pA/ $\sqrt{\text{Hz}}$
I <sub>NN</sub>	Input Referred Non-Inverting Noise Current	>1MHz		1.1		pA/ $\sqrt{\text{Hz}}$
SNF	Noise Floor	>1MHz		-151		dBm <sub>1Hz</sub>
INV	Total Integrated Input Noise	1MHz to 100MHz		60		$\mu\text{V}$
<b>Static, DC Performance</b>						
V <sub>IO</sub>	Input Offset Voltage			$\pm 2.5$	$\pm 7.0$ <b><math>\pm 8.5</math></b>	mV
DV <sub>IO</sub>	Input Offset Voltage Average Drift	(Note 8)		10		$\mu\text{V}/^\circ\text{C}$
I <sub>BN</sub>	Input Bias Current	Non Inverting (Note 7)		-0.4	$\pm 4$ <b><math>\pm 6</math></b>	$\mu\text{A}$
DI <sub>BN</sub>	Input Bias Current Average Drift	Non-Inverting (Note 8)		8		nA/ $^\circ\text{C}$
I <sub>BI</sub>	Input Bias Current	Inverting (Note 7)		-1	$\pm 12$ <b><math>\pm 16</math></b>	$\mu\text{A}$
DI <sub>BI</sub>	Input Bias Current Average Drift	Inverting (Note 8)		-3		nA/ $^\circ\text{C}$
+PSRR	Positive Power Supply Rejection Ratio	DC	52 <b>50</b>	64		dB
-PSRR	Negative Power Supply Rejection Ratio	DC	51 <b>50</b>	57		dB
CMRR	Common Mode Rejection Ratio	DC	49 <b>48</b>	55		dB
I <sub>CC</sub>	Supply Current	$R_L = \infty$ , $R_P = 137\text{k}\Omega$	2.8 <b>2.6</b>	3.4	3.9 <b>4.1</b>	mA
I <sub>CC</sub> I	Supply Current During Shutdown			<1		$\mu\text{A}$
<b>Miscellaneous Performance</b>						
R <sub>IN</sub>	Input Resistance	Non-Inverting		15		M $\Omega$
C <sub>IN</sub>	Input Capacitance	Non-Inverting		1.7		pF
R <sub>OUT</sub>	Output Resistance	Closed Loop		50		m $\Omega$
V <sub>O</sub>	Output Voltage Range	$R_L = \infty$	$\pm 3.60$ <b><math>\pm 3.55</math></b>	$\pm 3.78$		V
V <sub>OL</sub>		$R_L = 100\Omega$	$\pm 2.90$ <b><math>\pm 2.85</math></b>	$\pm 3.10$		
CMIR	Common Mode Input Range	Common Mode		$\pm 2.2$		V
I <sub>O</sub>	Output Current	Closed Loop $-20\text{mV} \leq V_O \leq 20\text{mV}$	$\pm 30$	$\pm 45$		mA

**Electrical Characteristics  $I_{CC} = 3.4\text{mA}$**  (Note 2) (Continued) $A_V = +2$ ,  $R_F = 1\text{k}\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 100\Omega$ ,  $R_P = 137\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
TON	Turn-on Time	0.5V <sub>PP</sub> Sine Wave, 90% of Full Value		42		ns
TOFF	Turn-off Time	0.5V <sub>PP</sub> Sine Wave, <5% of Full Value		10		
V <sub>O glitch</sub>	Turn-on Glitch			25		mV
FDTH	Feed-Through	f = 10MHz, A <sub>V</sub> = +2, Off State		-61		dB

**Electrical Characteristics  $I_{CC} = 1.0\text{mA}$**  (Note 2) $A_V = +2$ ,  $R_F = 1\text{k}\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 500\Omega$ ,  $R_P = 412\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
<b>Frequency Domain Response</b>						
SSBW	-3dB Bandwidth	V <sub>OUT</sub> = 2V <sub>PP</sub>		55		MHz
LSBW	-3dB Bandwidth	V <sub>OUT</sub> = 4.0V <sub>PP</sub>		30		MHz
GF <sub>0.1dB</sub>	0.1dB Gain Flatness	V <sub>OUT</sub> = 2V <sub>PP</sub>		20		MHz
GFP	Frequency Response Peaking	DC to 25MHz, V <sub>OUT</sub> = 2V <sub>PP</sub>		0.11		dB
GFR	Frequency Response Rolloff	DC to 25MHz, V <sub>OUT</sub> = 2V <sub>PP</sub>		0.05		dB
LPD	Linear Phase Deviation	DC to 20MHz, V <sub>OUT</sub> = 2V <sub>PP</sub>		1		deg
		DC to 14MHz, V <sub>OUT</sub> = 2V <sub>PP</sub>		0.3		
DG	Differential Gain	R <sub>L</sub> = 500Ω, 4.43MHz		0.020		%
DP	Differential Phase	R <sub>L</sub> = 500Ω, 4.43MHz		0.036		deg
<b>Time Domain Response</b>						
TRS	Rise Time	2V Step		3.7		ns
TRL	Fall Time	2V Step		5.1		
T <sub>S</sub>	Settling Time to 0.04%	A <sub>V</sub> = -1, 2V Step		18		ns
OS	Overshoot	2V Step		2		%
SR	Slew Rate	5V Step, 40% to 60% (Note 5)		400		V/μs
<b>Distortion And Noise Response</b>						
HD2	2nd Harmonic Distortion	2V <sub>PP</sub> , 5MHz		-43		dBc
HD3	3rd Harmonic Distortion	2V <sub>PP</sub> , 5MHz		-65		dBc
THD	Total Harmonic Distortion	2V <sub>PP</sub> , 1MHz		-70.0		dBc
V <sub>N</sub>	Input Referred Voltage Noise	>1MHz		8.4		nV/√Hz
I <sub>N</sub>	Input Referred Inverting Noise Current	>1MHz		9.0		pA/√Hz
I <sub>NN</sub>	Input Referred Non-Inverting Noise Current	>1MHz		0.8		pA/√Hz
SNF	Noise Floor	>1MHz		-147		dBm <sub>1Hz</sub>
INV	Total Integrated Input Noise	1MHz to 100MHz		29		μV
<b>Static, DC Performance</b>						
V <sub>IO</sub>	Input Offset Voltage			±1.6	±6.0 ±7.3	mV
DV <sub>IO</sub>	Input Offset Voltage Average Drift	(Note 8)		4		μV/°C
I <sub>BN</sub>	Input Bias Current	Non Inverting (Note 7)		0.04	±2.0 ±2.5	μA
DI <sub>BN</sub>	Input Bias Current Average Drift	Non-Inverting (Note 8)		-1		nA/°C
I <sub>BI</sub>	Input Bias Current	Inverting (Note 7)		-0.1	±6 ±8	μA

## Electrical Characteristics $I_{CC} = 1.0\text{mA}$ (Note 2) (Continued)

$A_V = +2$ ,  $R_F = 1\text{k}\Omega$ ,  $V_S = \pm 5\text{V}$ ,  $R_L = 500\Omega$ ,  $R_P = 412\text{k}\Omega$ ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
$DI_{BI}$	Input Bias Current Average Drift	Inverting (Note 8)		-3		nA/°C
+PSRR	Positive Power Supply Rejection Ratio	DC	52 <b>51</b>	64		dB
-PSRR	Negative Power Supply Rejection Ratio	DC	51 <b>49</b>	59		dB
CMRR	Common Mode Rejection Ratio	DC	49 <b>47</b>	55		dB
$I_{CC}$	Supply Current	$R_L = \infty$ , $R_P = 412\text{k}\Omega$	0.70 <b>0.66</b>	1.0	1.3 <b>1.4</b>	mA
$I_{CC }$	Supply Current During Shutdown			<1		$\mu\text{A}$
<b>Miscellaneous Performance</b>						
$R_{IN}$	Input Resistance	Non-Inverting		46		M $\Omega$
$C_{IN}$	Input Capacitance	Non-Inverting		1.7		pF
$R_{OUT}$	Output Resistance	Closed Loop		100		m $\Omega$
$V_O$	Output Voltage Range	$R_L = \infty$	$\pm 3.60$ <b><math>\pm 3.55</math></b>	$\pm 3.78$		V
$V_{OL}$		$R_L = 500\Omega$	$\pm 2.90$ <b><math>\pm 2.85</math></b>	$\pm 3.10$		
CMIR	Common Mode Input Range	Common Mode		$\pm 2.2$		V
$I_O$	Output Current	Closed Loop $-15\text{mV} \leq V_O \leq 15\text{mV}$	$\pm 6$	$\pm 9$		mA
TON	Turn-on Time	$0.5V_{PP}$ Sine Wave, 90% of Full Value		95		ns
TOFF	Turn-off Time	$0.5V_{PP}$ Sine Wave, <5% of Full Value		40		
$V_{O\text{ glitch}}$	Turn-on Glitch			15		mV
FDTH	Feed-Through	$f = 10\text{MHz}$ , $A_V = +2$ , Off State		-61		dB

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

**Note 2:** Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Min/Max ratings are based on production testing unless otherwise specified.

**Note 3:** The maximum output current ( $I_O$ ) is determined by device power dissipation limitations.

**Note 4:** Human body model:  $1.5\text{k}\Omega$  in series with  $100\text{pF}$ . Machine model:  $0\Omega$  in series with  $200\text{pF}$ .

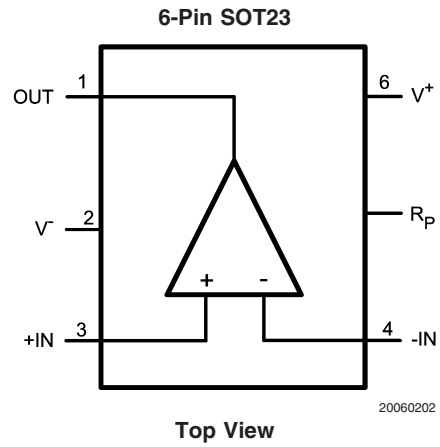
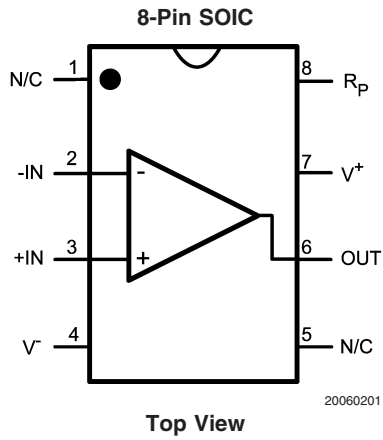
**Note 5:** Slew Rate is the average of the rising and falling edges.

**Note 6:** Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.

**Note 7:** Negative input current implies current flowing out of the device.

**Note 8:** Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change.

## Connection Diagrams

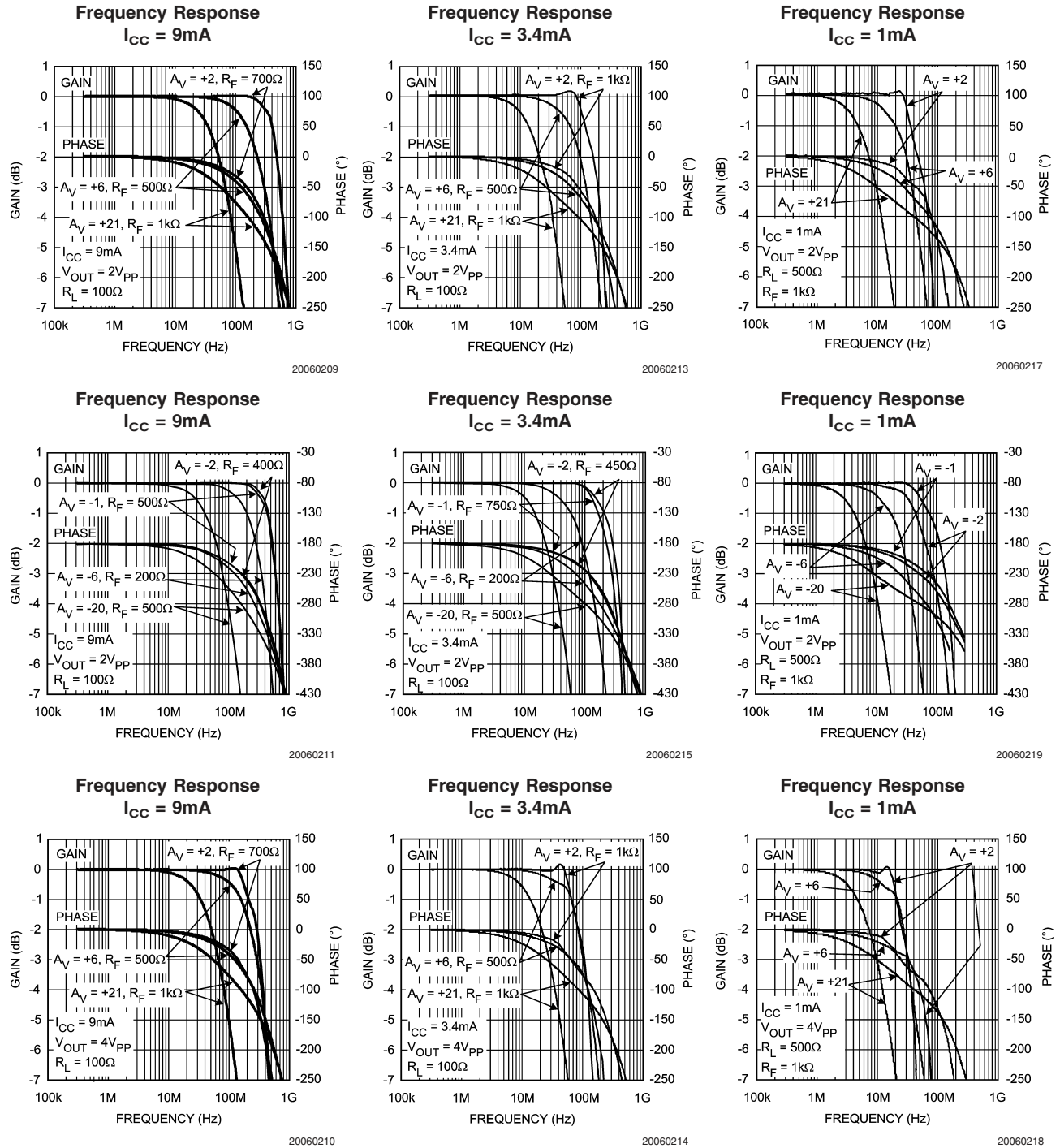


## Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-pin SOIC	LMH6732MA	LMH6732MA	95 Units/Rail	M08A
	LMH6732MAX		2.5k Units Tape and Reel	
6-Pin SOT23	LMH6732MF	A97A	1k Units Tape and Reel	MF06A
	LMH6732MFX		3k Units Tape and Reel	

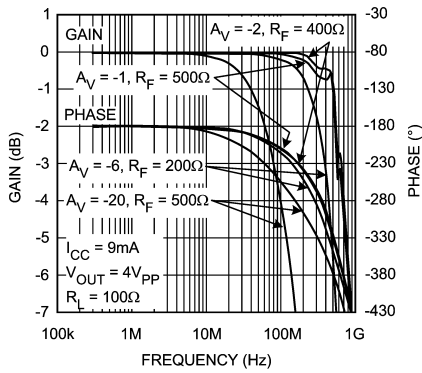


# Typical Performance Characteristics



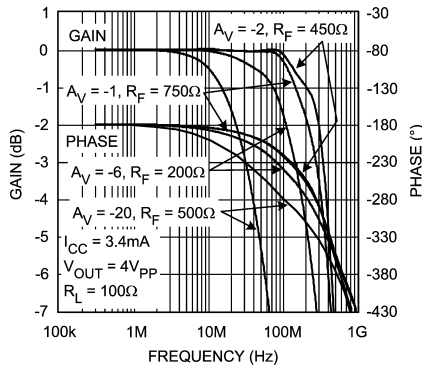
Typical Performance Characteristics (Continued)

Frequency Response  
I<sub>CC</sub> = 9mA



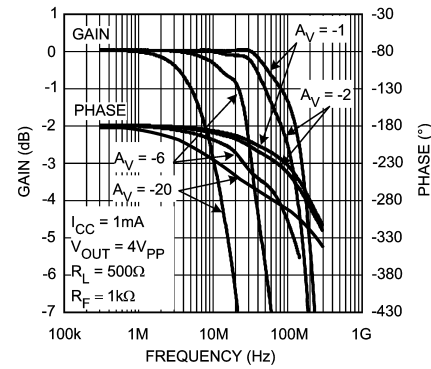
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Frequency Response  
I<sub>CC</sub> = 3.4mA



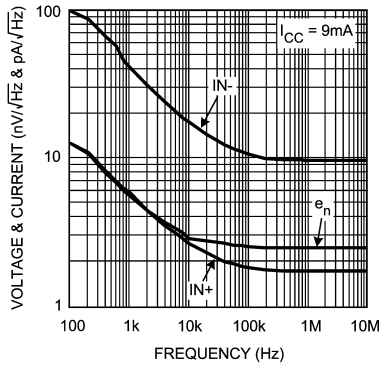
20060216

Frequency Response  
I<sub>CC</sub> = 1mA



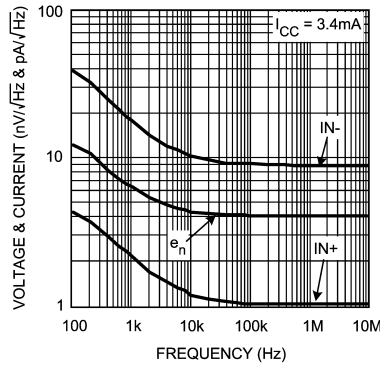
20060220

Noise  
I<sub>CC</sub> = 9mA



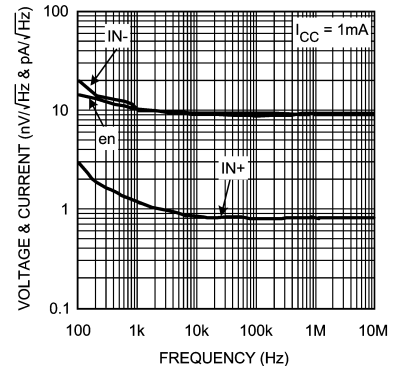
20060229

Noise  
I<sub>CC</sub> = 3.4mA



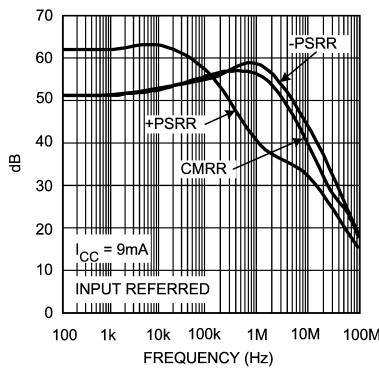
20060230

Noise  
I<sub>CC</sub> = 1mA



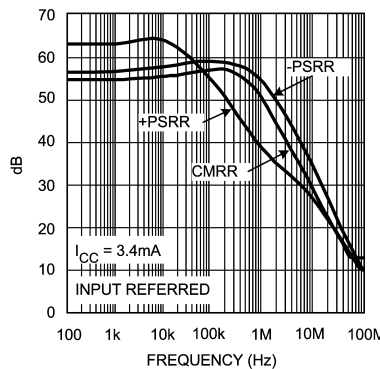
20060231

CMRR and PSRR  
I<sub>CC</sub> = 9mA



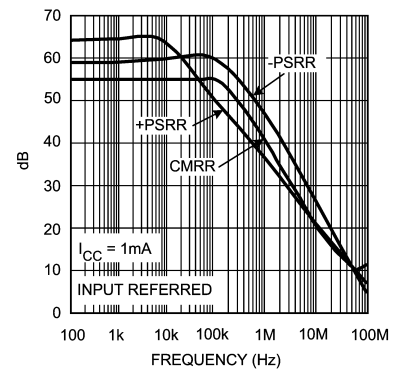
20060205

CMRR and PSRR  
I<sub>CC</sub> = 3.4mA



20060204

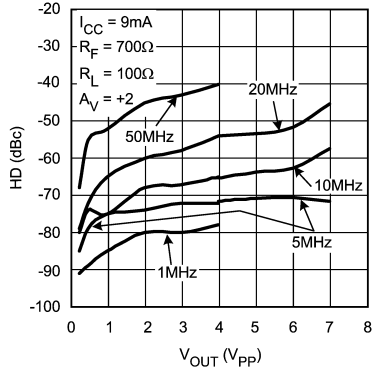
CMRR and PSRR  
I<sub>CC</sub> = 1mA



20060203

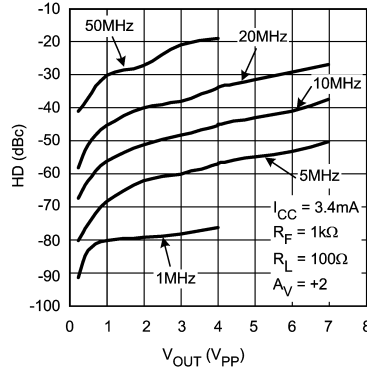
# Typical Performance Characteristics (Continued)

**2nd Distortion vs. Output Amplitude**  
 $I_{CC} = 9\text{mA}$



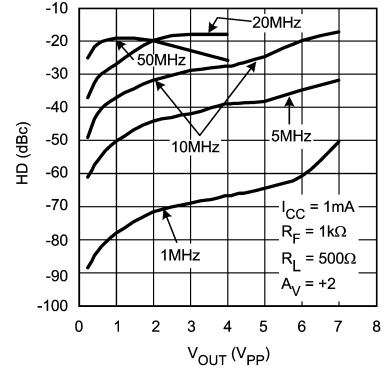
20060223

**2nd Distortion vs. Output Amplitude**  
 $I_{CC} = 3.4\text{mA}$



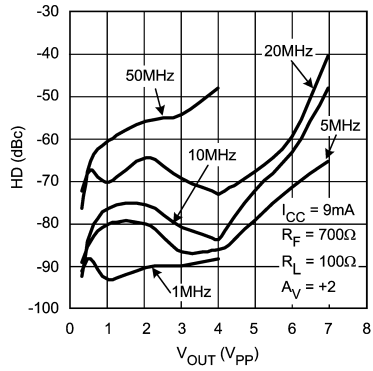
20060225

**2nd Distortion vs. Output Amplitude**  
 $I_{CC} = 1\text{mA}$



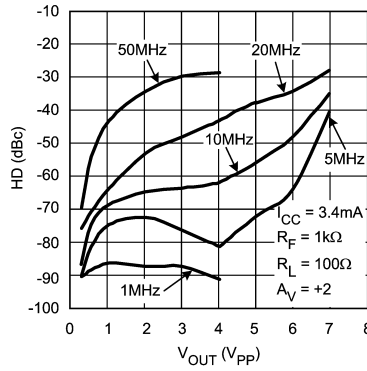
20060227

**3rd Distortion vs. Output Amplitude**  
 $I_{CC} = 9\text{mA}$



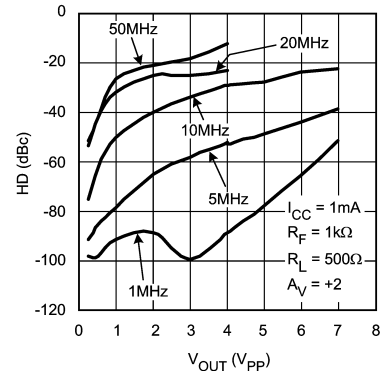
20060224

**3rd Distortion vs. Output Amplitude**  
 $I_{CC} = 3.4\text{mA}$



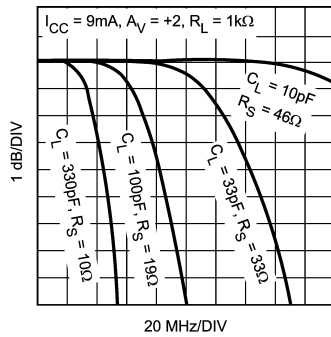
20060226

**3rd Distortion vs. Output Amplitude**  
 $I_{CC} = 1\text{mA}$



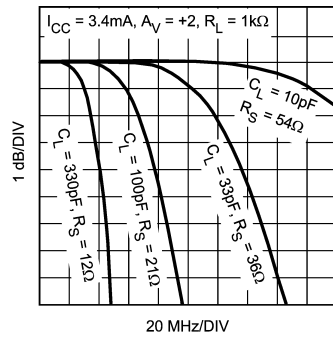
20060222

**Frequency Response for Various  $C_L$**   
 $I_{CC} = 9\text{mA}$



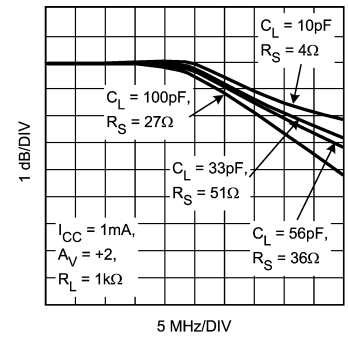
20060255

**Frequency Response for Various  $C_L$**   
 $I_{CC} = 3.4\text{mA}$



20060256

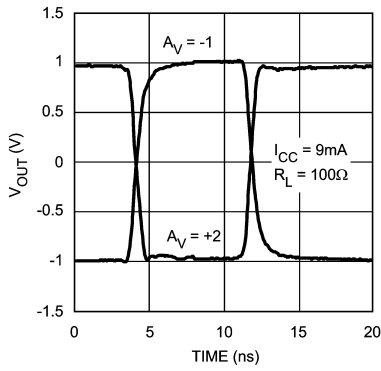
**Frequency Response for Various  $C_L$**   
 $I_{CC} = 1\text{mA}$



20060257

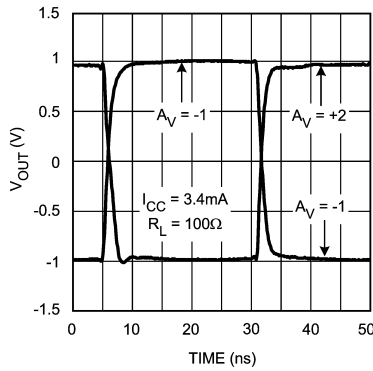
# Typical Performance Characteristics (Continued)

**Small Signal Step Response**  
 $I_{CC} = 9\text{mA}$



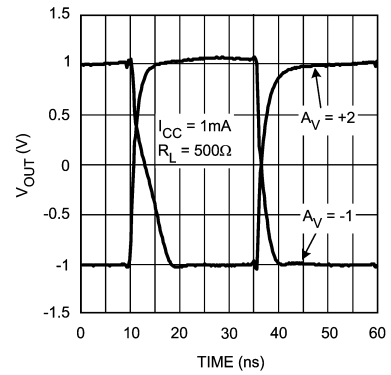
20060221

**Small Signal Step Response**  
 $I_{CC} = 3.4\text{mA}$



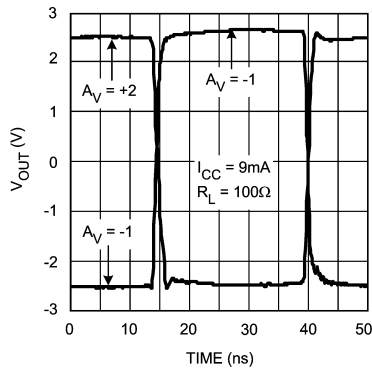
20060243

**Small Signal Step Response**  
 $I_{CC} = 1\text{mA}$



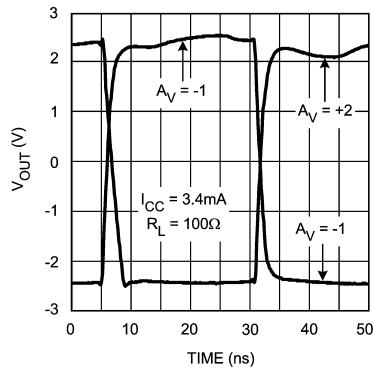
20060241

**Large Signal Step Response**  
 $I_{CC} = 9\text{mA}$



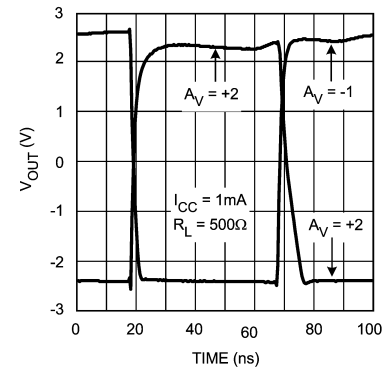
20060245

**Large Signal Step Response**  
 $I_{CC} = 3.4\text{mA}$



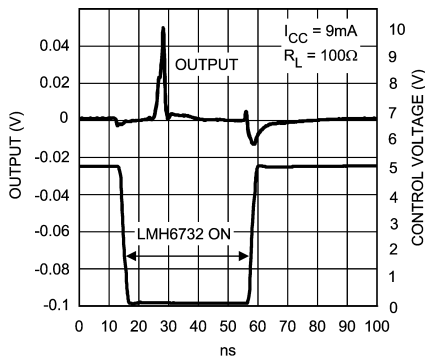
20060244

**Large Signal Step Response**  
 $I_{CC} = 1\text{mA}$



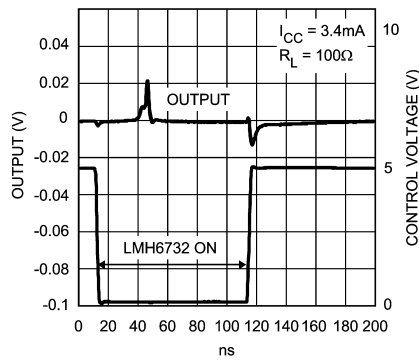
20060242

**Output Glitch**  
 $I_{CC} = 9\text{mA}$



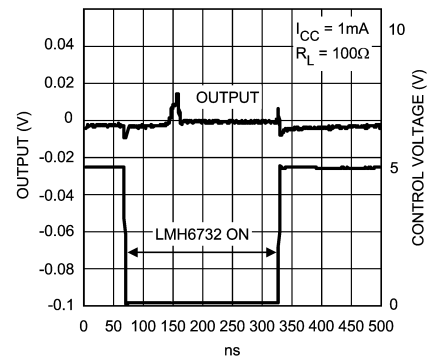
20060247

**Output Glitch**  
 $I_{CC} = 3.4\text{mA}$



20060248

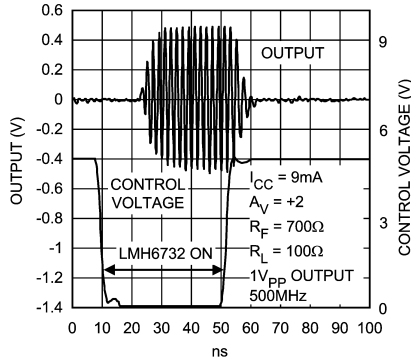
**Output Glitch**  
 $I_{CC} = 1\text{mA}$



20060249

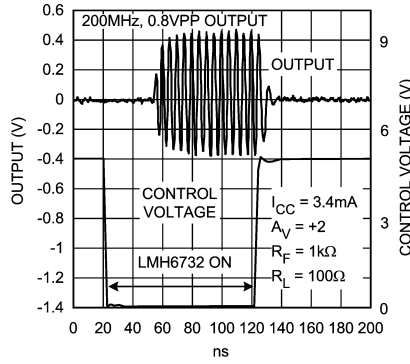
# Typical Performance Characteristics (Continued)

**Turn-On/Off Characteristics**  
 $I_{CC} = 9\text{mA}$



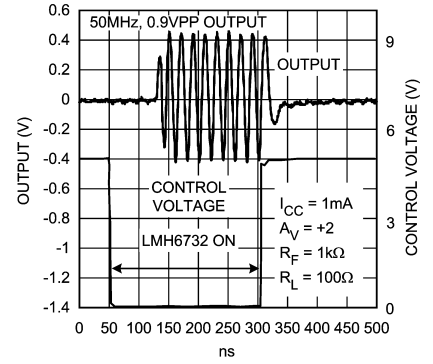
20060250

**Turn-On/Off Characteristics**  
 $I_{CC} = 3.4\text{mA}$



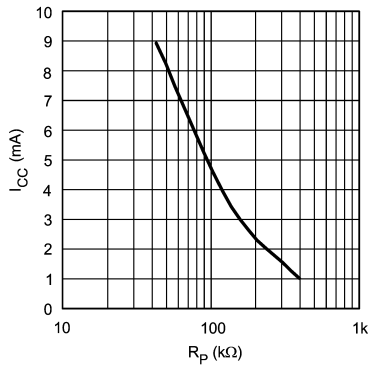
20060251

**Turn-On/Off Characteristics**  
 $I_{CC} = 1\text{mA}$



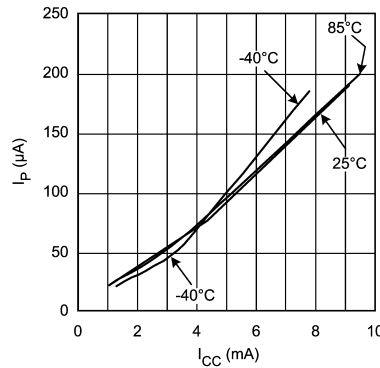
20060252

**$I_{CC}$  vs.  $R_P$**



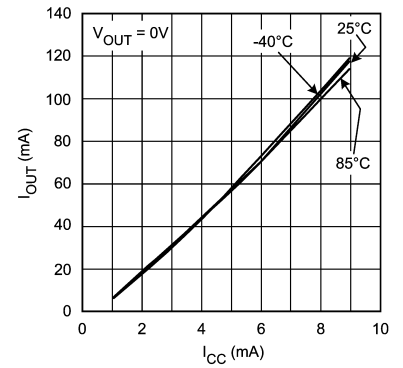
20060235

**$I_P$  vs.  $I_{CC}$**



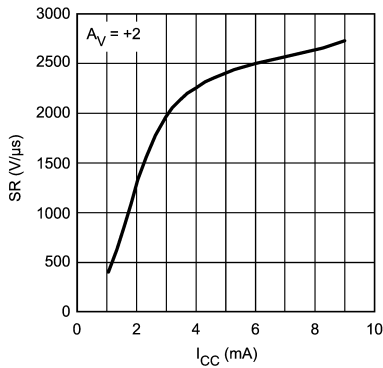
20060240

**Max Output Current vs.  $I_{CC}$**



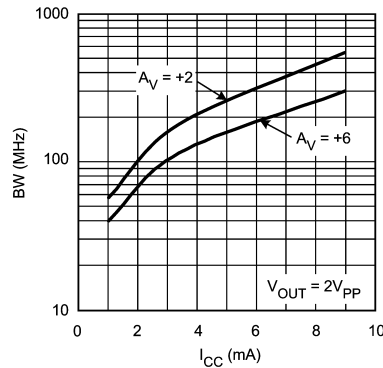
20060236

**Slew Rate vs.  $I_{CC}$**



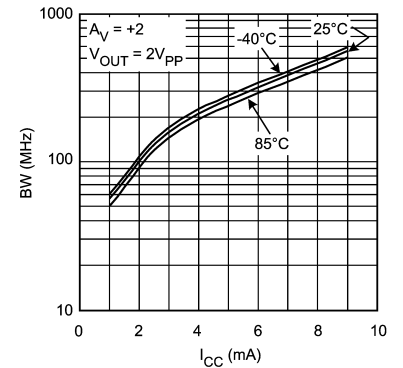
20060237

**BW vs.  $I_{CC}$**



20060238

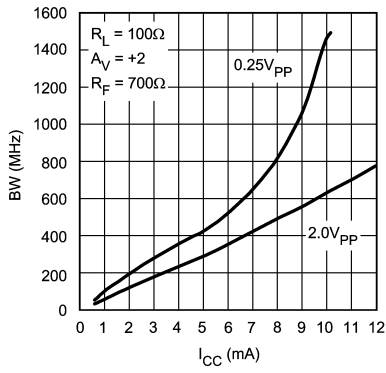
**BW vs.  $I_{CC}$  for Various Temperature**



20060239

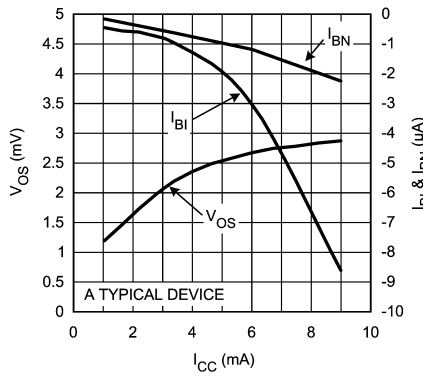
# Typical Performance Characteristics (Continued)

**-3dB BW vs.  $I_{CC}$**



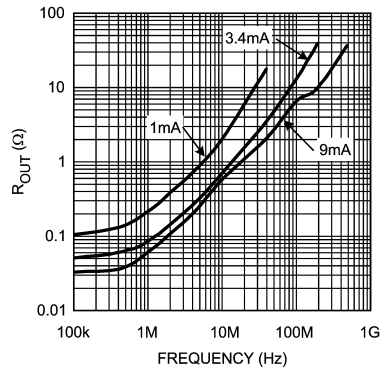
20060262

**$V_{OS}$ ,  $I_{BI}$  &  $I_{BN}$  VS.  $I_{CC}$**



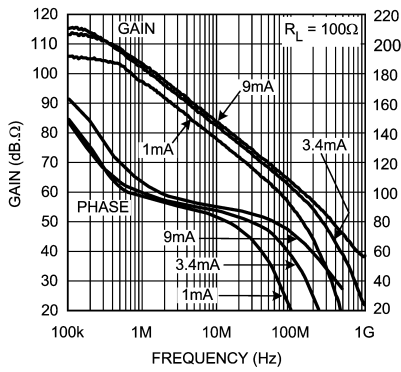
20060234

**Output Impedance vs. Frequency**



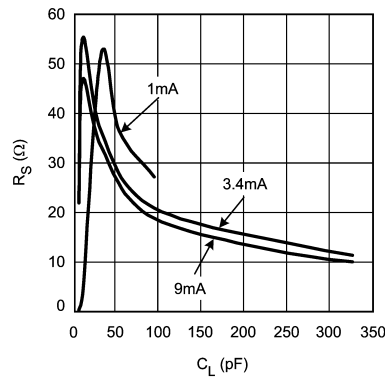
20060233

**Transimpedance**



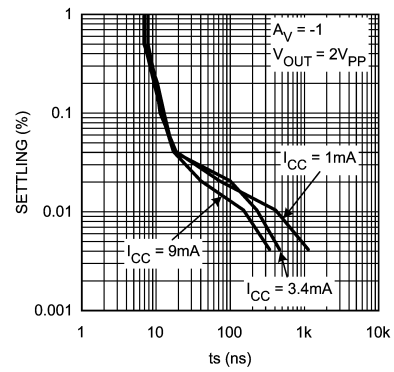
20060232

**Recommended  $R_S$  vs.  $C_L$**



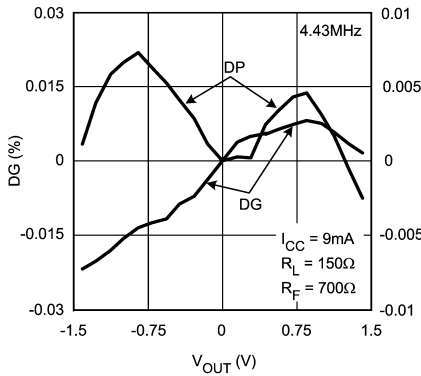
20060254

**Settling Time**



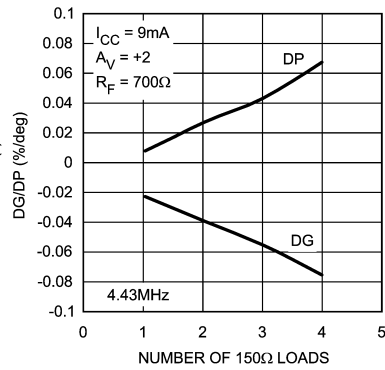
20060228

**DG/DP  
 $I_{CC} = 9mA$**



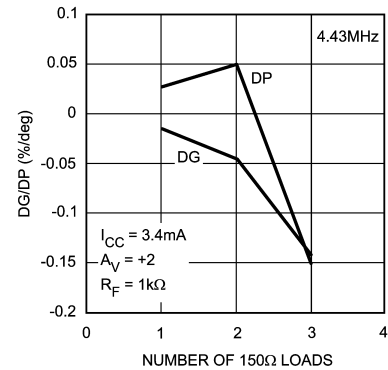
20060206

**DG/DP for Various  $R_L$   
 $I_{CC} = 9mA$**



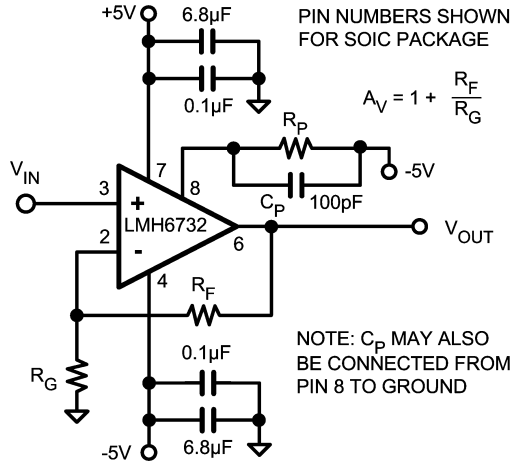
20060207

**DG/DP for Various  $R_L$   
 $I_{CC} = 3.4mA$**



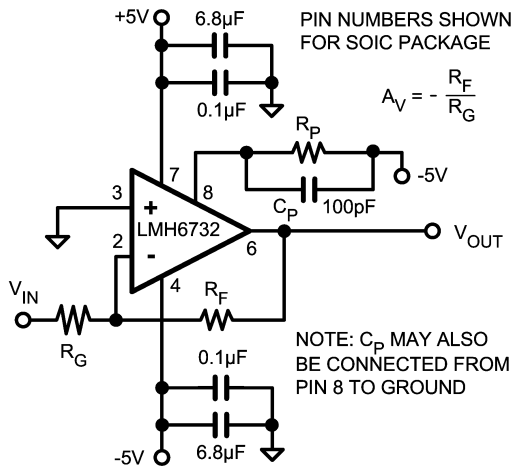
20060208

## Application Information:



20060258

FIGURE 1. Recommended Non-Inverting Gain Circuit



20060259

FIGURE 2. Recommended Inverting Gain Circuit

### DESCRIPTION

The LMH6732 is an adjustable supply current, current-feedback operational amplifier. Supply current and consequently dynamic performance can be easily adjusted by selecting the value of a single external resistor ( $R_P$ ).

**Note:** Note: The following discussion uses the SOIC package pin numbers. For the corresponding SOT23-6 package pin numbers, please refer to the Connection Diagram section.

### SELECTING AN OPERATING POINT

The operating point is determined by the supply current which in turn is determined by current ( $I_P$ ) flowing out of pin 8. As the supply current is increased, the following effects will be observed:

TABLE 1. Device Parameters Related to Supply Current

Specification	Effect as $I_{CC}$ Increases
Bandwidth	Increases
Rise Time	Decreases
Enable/ Disable Speed	Increases
Output Drive	Increases
Input Bias Current	Increases
Input Impedance	Decreases (see Source impedance Discussion)

Both the Electrical Characteristics pages and the Typical Performance Characteristics section illustrate these effects to help make the supply current vs. performance trade-off. The supply current is adjustable over a continuous range of more than 10 to 1 with a single resistor,  $R_P$ , allowing for easy trade-off between power consumption and speed. Performance is specified and tested at  $I_{CC} = 1\text{mA}$ ,  $3.4\text{mA}$ , and  $9\text{mA}$ . (Note: Some test conditions and especially the load resistances are different for the three supply current settings.) The performance plots show typical performance for all three supply currents levels.

When making the supply current vs. performance trade-off, it is first a good idea to see if one of the standard operating points ( $I_{CC} = 1\text{mA}$ ,  $3.4\text{mA}$ , or  $9\text{mA}$ ) fits the application. If it does, performance guaranteed on the specification pages will apply directly to your application. In addition, the value of  $R_P$  may be obtained directly from the Electrical Characteristics pages.

### BEYOND 1GHz BANDWIDTH

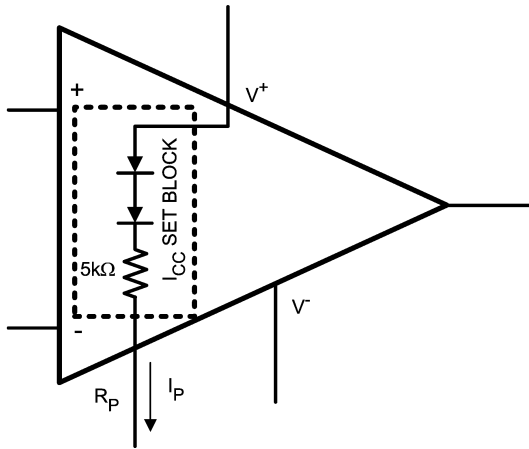
As stated above, the LMH6732 speed can be increased by increasing the supply current. The  $-3\text{dB}$  Bandwidth can even reach the unprecedented value of  $1.5\text{GHz}$  ( $A_V = +2$ ,  $V_{OUT} = 0.25V_{PP}$ ). Of course, this comes at the expense of power consumption (i.e. supply current). The relationship between  $-3\text{dB}$  BW and supply current is shown in the Typical Performance Characteristics section. The supply current would nominally have to be set to around  $10\text{mA}$  to achieve this speed. The absolute maximum supply current setting for the LMH6732 is  $14\text{mA}$ . Beyond this value, the operation may become unpredictable.

**The following discussion will assist in selecting  $I_{CC}$  for applications that cannot operate at one of the specified supply current settings.**

Use the typical performance plots for critical specifications to select the best  $I_{CC}$ . For parameters containing Min/Max ratings in the data sheet tables, interpolate between the values of  $I_{CC}$  in the plots & specification tables to estimate the max/min values in the application.

The simplified schematic for the supply current setting path ( $I_P$ ) is shown below in Figure 3.

## Application Information: (Continued)



20060246

**FIGURE 3. Supply Current Control's Simplified Schematic**

The terminal marked "R<sub>P</sub>" is tied to a potential through a resistor R<sub>P</sub>. The current flowing through R<sub>P</sub> (I<sub>P</sub>) sets the LMH6732's supply current. Throughout the data sheet, the voltages applied to R<sub>P</sub> and V<sup>-</sup> are both considered to be -5V. However, the two potentials do not necessarily have to be the same. This is beneficial in applications where non-standard supply voltages are used or when there is a need to power down the op amp via digital logic control.

The relationship between I<sub>CC</sub> and I<sub>P</sub> is given by:

$I_P = I_{CC}/57$  (approximate ratio at I<sub>CC</sub> = 3.4mA; consult "I<sub>CC</sub> vs. I<sub>P</sub>" plot for relationship at any I<sub>CC</sub>).

Knowing I<sub>P</sub> leads to a direct calculation of R<sub>P</sub>.

$$R_P + 5k\Omega = [(V^+ - 1.6)V^-] / I_P$$

$$R_P + 5k\Omega = 8.4 / I_P \text{ (for } V^+ = 5V \text{ and } V^- = -5V).$$

First, an operating point needs to be determined from the plots & specifications as discussed above. From this, I<sub>P</sub> is obtained. Knowing I<sub>P</sub> and the potential R<sub>P</sub> is tied to, R<sub>P</sub> can be calculated.

### EXAMPLE

An application requires that V<sub>S</sub> = ±3V and performance in the 1mA operating point range. The required I<sub>P</sub> can therefore be determined as follows:

$$I_P = 21\mu A$$

R<sub>P</sub> is connected from pin 8 to V<sup>-</sup>. Calculate R<sub>P</sub> under these conditions:

$$R_P + 5k\Omega = [(V^+ - 1.6)V^-] / I_P$$

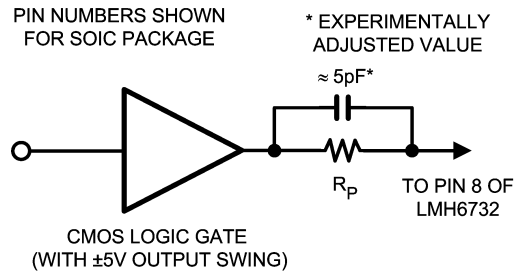
$$R_P + 5k\Omega = [(3V - 1.6V) - (-3V)] / 21\mu A$$

$$R_P = 205k\Omega$$

The LMH6732 will have performance similar to R<sub>P</sub> = 412kΩ shown on the datasheet, but with 40% less power dissipation due to the reduced supply voltages. The op amp will also have a more restricted common-mode range and output swing.

## DYNAMIC SHUTDOWN CAPABILITY

The LMH6732 may be powered on and off very quickly by controlling the voltage applied to R<sub>P</sub>. If R<sub>P</sub> is connected between pin 8 and the output of a CMOS gate powered from ±5V supplies, the gate can be used to turn the amplifier on and off. This is shown in Figure 4 below:



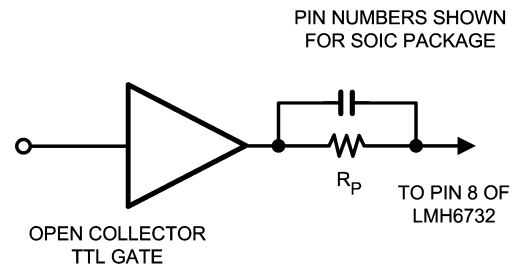
20060260

**FIGURE 4. Dynamic Control of Power Consumption Using CMOS Logic**

When the gate output is switched from high to low, the LMH6732 will turn on. In the off state, the supply current typically reduces to 1μA or less. The LMH6732's "off state" supply current is reduced significantly compared to the CLC505. This extremely low supply current in the "off state" is quite advantageous since it allows for significant power saving and minimizes feed-through. To improve switching time, a speed up capacitor from the gate output to pin 8 is recommended. The value of this capacitor will depend on the R<sub>P</sub> value used and is best established experimentally. Turn-on and turn-off times of <20ns (I<sub>CC</sub> = 9mA) are achievable with ordinary CMOS gates.

### EXAMPLE

An open collector logic device is used to dynamically control the power dissipation of the circuit. Here, the desired connection for R<sub>P</sub> is from pin 8 to the open collector logic device.



20060261

**FIGURE 5. Controlling Power On State with TTL Logic (Open Collector Output)**

When the logic gate goes low, the LMH6732 is turned on. The LMH6732 V<sup>+</sup> connection would be to +5V supply.

Performance desired is that given for I<sub>CC</sub> = 3.4mA under standard conditions. From the I<sub>CC</sub> vs. I<sub>P</sub> plot, I<sub>P</sub> = 61μA. Then calculating R<sub>P</sub>:

$$R_P + 5k\Omega = [(5V - 1.6V) - 0] / 61\mu A$$

$$R_P = 51k\Omega$$



## Application Information: (Continued)

### "POPLESS OUTPUT" & OFF CONDITION OUTPUT STATE

The LMH6732 has been especially designed to have minimum glitches during turn-on and turn-off. This is advantageous in situations where the LMH6732 output is fed to another stage which could experience false auto-ranging, or even worse reset operation, due to these transient glitches. Example of this application would be an AGC circuit or an ADC with multiple ranges set to accommodate the largest input amplitude. For the LMH6732, these sorts of transients are typically less than 50mV in amplitude (see Electrical Characteristics Tables for Typical values). Applications designed to utilize the CLC505's low output glitch would benefit from using the LMH6732 instead since the LMH6732's output glitch is improved to be even lower than the CLC505's. In the "Off State", the output stage is turned off and is in effect put into a high-Z state. In this state, output can be forced by other active devices. No significant current will flow through the device output pin in this mode of operation.

### MUX APPLICATION

Since The LMH6732's output is essentially open in the "off" state, it is a good candidate for a fast 2:1 MUX. *Figure 6* shows one such application along with the output waveform in *Figure 7* displaying the switching between a continuous triangle wave and a single cycle sine wave (signals trigger locked to each other for stable scope photo). Switching speed of the MUX will be less than 50 ns and is governed by the "Ton" and "Toff" times for U1 and U2 at the supply current set by  $R_{P1}$  and  $R_{P2}$ . Note that the "Control" input is a 5V CMOS logic level.

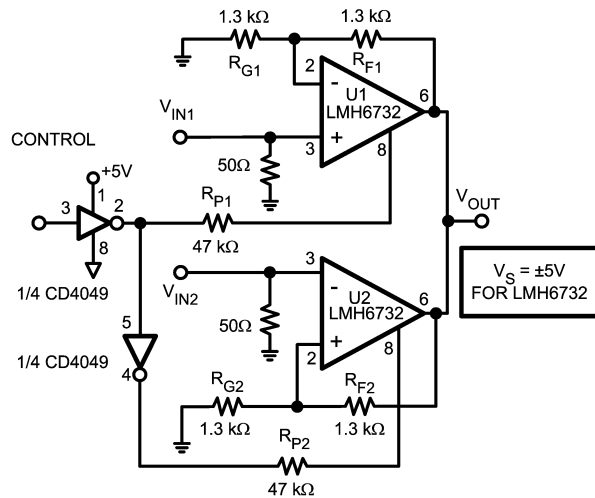
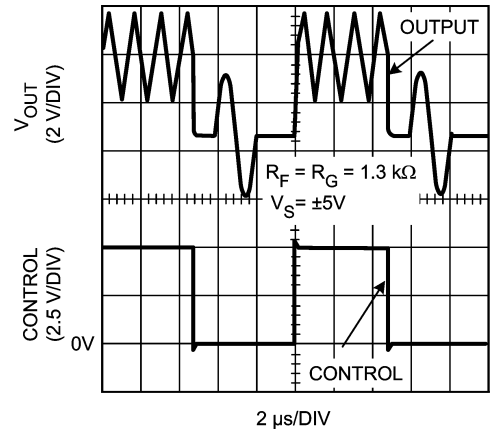


FIGURE 6. 50 ns 2:1 MUX Schematic



20060264

FIGURE 7. MUX "V<sub>OUT</sub>" and "Control" Waveform

### DIFFERENTIAL GAIN AND PHASE

Differential gain and phase are measurements useful primarily in composite video channels. They are measured by monitoring the gain and phase changes of a high frequency carrier (3.58MHz for NTSC and 4.43MHz for PAL systems) as the output of the amplifier is swept over a range of DC voltages. Specifications for the LMH6732 include differential gain and phase. Test signals used are based on a  $1V_{PP}$  video level. Test conditions used are the following:

DC sweep range: 0 to 100 IRE units (black to white)

Carrier: 4.43MHz at 40 IRE units peak to peak

$A_V = +2$ ,  $R_L = 75\Omega + 75\Omega$

### SOURCE IMPEDANCE

For best results, source impedance in the non-inverting circuit configuration (see *Figure 1*) should be kept below  $5k\Omega$ . Above  $5k\Omega$  it is possible for oscillation to occur, depending on other circuit board parasitics. For high signal source impedances, a resistor with a value of less than  $5k\Omega$  may be used to terminate the non-inverting input to ground.

### FEEDBACK RESISTOR

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value. The LMH6732 provides optimum performance with feedback resistors as shown in Table 2 below. Selection of an incorrect value can lead to severe rolloff in frequency response, (if the resistor value is too large) or , peaking or oscillation (if the value is too low).

20060263

**Application Information:** (Continued)**TABLE 2. Feedback Resistor Selection for Various Gain Settings and  $I_{CC}$ 's**

Gain (V/V)	$I_{CC}$ (mA)			Unit
	9	3.4	1	
$A_V = +1$	700	1k	1k	$\Omega$
$A_V = +2$	700	1k	1k	$\Omega$
$A_V = -1$	500	750	1k	$\Omega$
$A_V = -2$	400	450	1k	$\Omega$
$A_V = +6$	500	500	1k	$\Omega$
$A_V = -6$	200	200	1k	$\Omega$
$A_V = +21$	1k	1k	1k	$\Omega$
$A_V = -20$	500	500	1k	$\Omega$

For  $I_{CC} > 9\text{mA}$  at any closed loop gain setting, a good starting point for  $R_F$  would be the 9mA value stated in Table 2 above. This value could then be readjusted, if necessary, to achieve the desired response.

**PRINTED CIRCUIT LAYOUT & EVALUATION BOARDS**

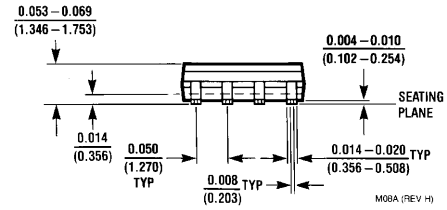
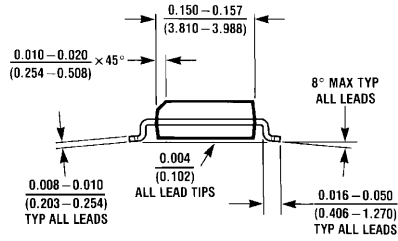
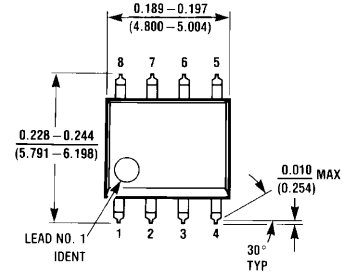
Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to

ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

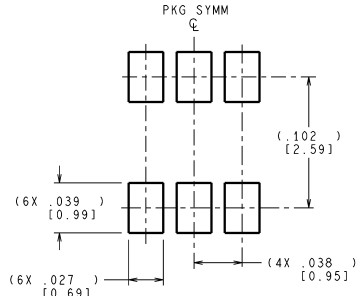
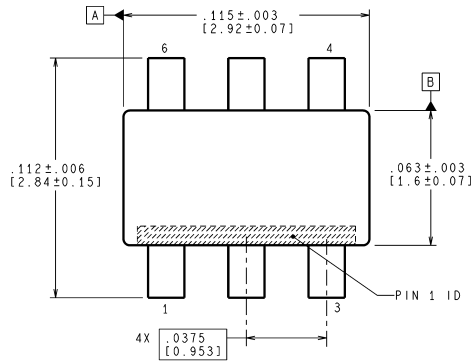
Device	Package	Evaluation Board Part Number
LMH6732MF	SOT23-6	CLC730216
LMH6732MA	SOIC	CLC730227

These evaluation boards are shipped when a device sample request is placed with National Semiconductor. The supply current adjustment resistor,  $R_P$ , in both evaluation boards should be tied to the appropriate potential to get the desired supply current. To do so, leave R2 (CLC730216) [ R5 (CLC730227) ] uninstalled. Jumper "Dis" connector to  $V^-$ . Install R1 (CLC730216) [ R4 (CLC730227) ] to set the supply current.

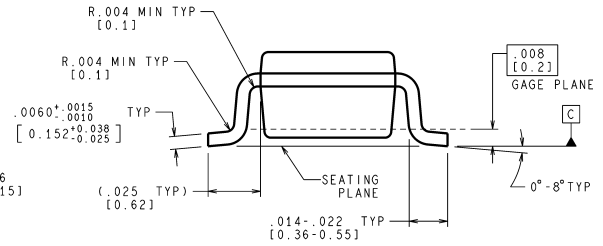
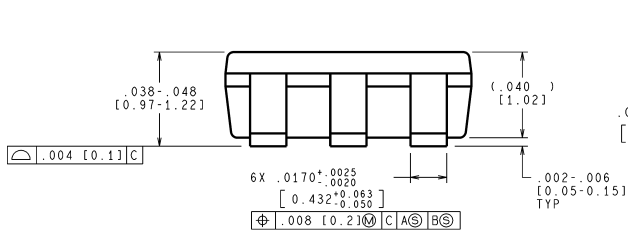
**Physical Dimensions** inches (millimeters)  
unless otherwise noted



**8-Pin SOIC**  
**NS Package Number M08A**



**RECOMMENDED LAND PATTERN**



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

**6-Pin SOT23**  
**NS Package Number MF06A**

MF06A (Rev B)

## Notes

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- |                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.</p> | <p>2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.</p> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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