F95231

HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION — The F95231 contains two master/slave D type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

PIN NAMES

D	Data Input to Master
CP	Clock Input
CP_C	Common Clock Input
Q	Output
$\overline{Q}$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

SYNCHRONOUS OPERATION

D TABLE

D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

(t+1) = Time after positive going clock transition

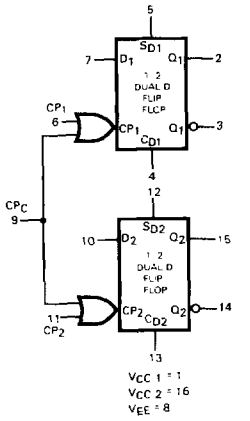
TRUTH TABLES

ASYNCHRONOUS OPERATION

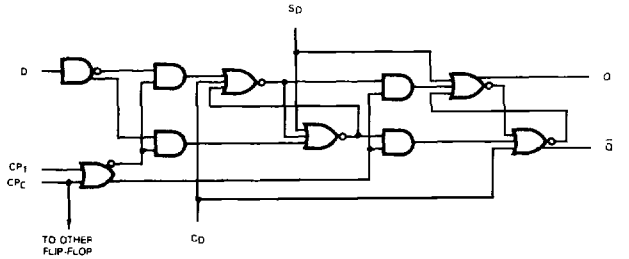
S_D C_D TABLE

C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC SYMBOL



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH C_{D1} and C_{D2} S_{D1} and S_{D2} CP_1 and CP_2 D_1 and D_2 CP_C			 330 330 220 245 265	µA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-56	-45		mA	Inputs & Outputs Open	

DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to +75°C

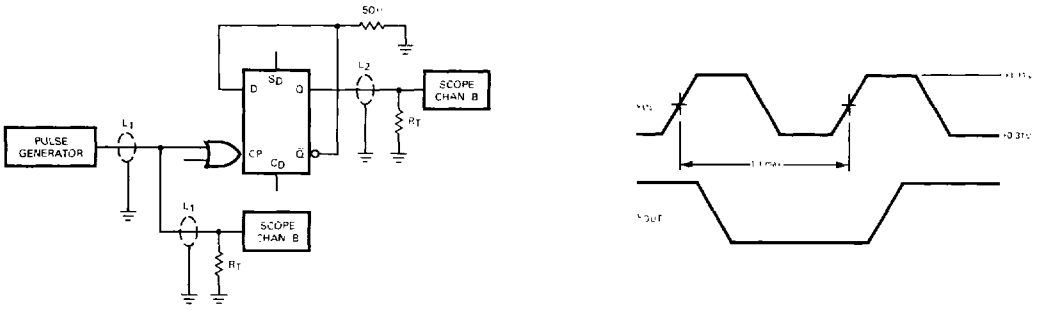
V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} *per Truth Table*	Loading is 50Ω *to -2.0 V*
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current		-47		mA	Inputs & Outputs Open V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 75°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Toggle Frequency	200			MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output	1.5	2.8	3.5	ns	See Figures 2 and 3
t_{PLH}, t_{PHL}	Propagation Delay Set to Q, Clear to Q	1.5	2.8	3.7	ns	
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.0	1.8	3.1	ns	
t_s	Set-up Time Data to Clock	1.5	0.5		ns	
t_h	Hold Time Data to Clock	0.75	-0.5		ns	

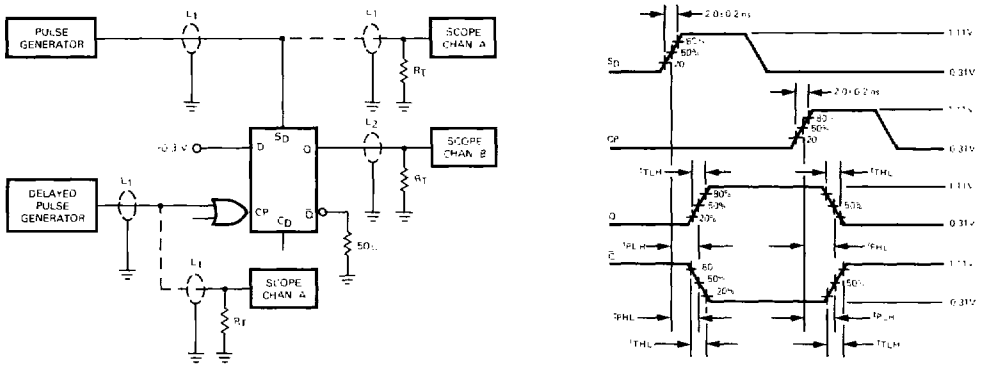
8

SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Toggle Rate Test Circuit and Waveforms



L_1 and L_2 = equal length 50 Ω impedance lines
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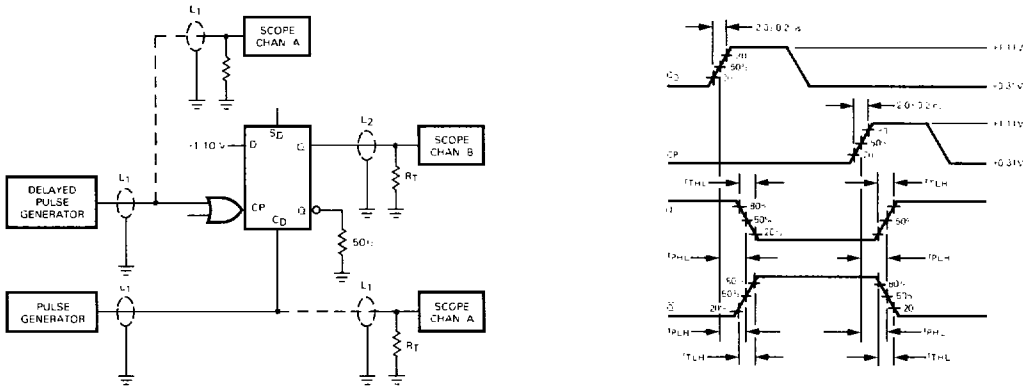
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Propagation Delay and S_D Test Circuit

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)

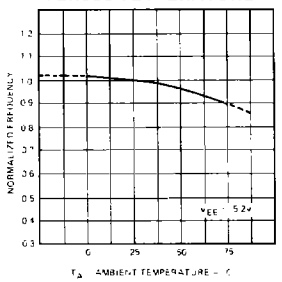


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

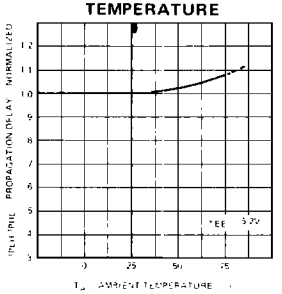
Fig. 3. Propagation Delay and C_D Test Circuit

TYPICAL ELECTRICAL CHARACTERISTICS

TOGGLE RATE VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS V_{EE}