BVA303

DIGITAL VARIABLE GAIN AMPLIFIER

30-4000 MHz

Device Features

- Integrate DSA to Amp Functionality
- Wide Power supply range of +2.7 to +5.5V (DSA)
- Single Fixed +3V supply (Amp)
- 30-4000MHz Broadband Performance
- 20.3dB Gain @ 2.14GHz
- 3.0dB Noise Figure @ 2.14GHz with max gain setting
- 15.7dBm P1dB @ 2.14GHz
- 28.5dBm OIP3 @ 2.14GHz
- No matching circuit needed
- Attenuation: 0.5 dB steps up to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy (DSA to Amp)
  ±(0.15 + 5% x Atten) @ 2.14GHz
- 1.8V control logic compatible
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

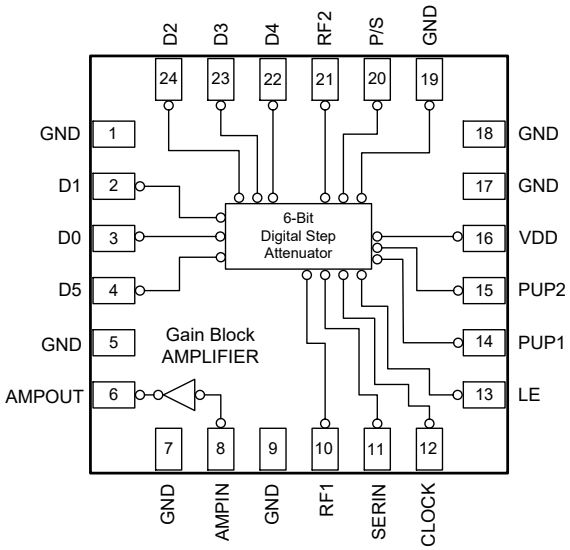


Figure 2. Functional Block Diagram

Product Description

The BVA303 is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 3V supply with a broadband frequency range of 30 to 4000 MHz.

The BVA303 integrates a high performance digital step attenuator and a high linearity, broadband gain block.
using the small package (4x4mm QFN package) and operating V_{DD} 3V voltage.
and designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

Both stages are internally matched to 50 Ohms and It is easy to use with no external matching components required.

A serial output port enables cascading with other serial controlled devices.

An integrated digital control interface supports both serial and parallel programming of the attenuation,
including the capability to program an initial attenuation state at power-up.
Covering a 31.5 dB attenuation range in 0.5 dB steps.

The BVA303 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Application

- 3G/4G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			30		4000	MHz
Gain[2]		Attenuation = 0dB, at 1900MHz	20.1	21.1	22.1	dB
Attenuation Control range		0.5dB step		31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	30MHz — 1GHz	Any bit or bit combination			±(0.15 + 3% of atten setting)	dB
	>1GHz — 2.2GHz				±(0.15 + 5% of atten setting)	
	>2.2GHz — 3GHz				±(0.15 + 8% of atten setting)	
	>3GHz — 4GHz				±(0.15 + 11% of atten setting)	
Return loss (input or output port)	1GHz — 2.2GHz	Attenuation = 0dB	13	18		dB
	>2.2GHz — 4GHz		10	16		
Output Power for 1dB Compression		Attenuation = 0dB , at 1900MHz		16		dBm
Output Third Order Intercept Point[3]		Attenuation = 0dB, at 1900MHz two tones at an output of 0 dBm per tone separated by 1 MHz.		29		dBm
Noise Figure		Attenuation = 0dB, at 1900MHz		2.9		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		3		V
Supply Current			40	54	60	mA
Control Interface		Serial / parallel mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Maximum Spurious level[4]		Measured at DSA RF1, RF2 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3V, measure on Evaluation Board (DSA to AMP)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 measured with two tones at an output of 0 dBm per tone separated by 1 MHz.
4. The unwanted spurious due to built-in negative voltage generator.

Table 2. Typical RF Performance[1]

Parameter	Frequency					Unit
	70[2]	900	1900	2140	2650	MHz
Gain[3]	27.2	24.7	21.1	20.3	18.2	dB
S11	-14.7	-13.7	-18.4	-18.2	-19.2	dB
S22	-13.4	-10.7	-17	-16.4	-13.3	dB
OIP3[4]	31.5	31	29	28.5	27.2	dBm
P1dB	16.3	17	16	15.7	15	dBm
Noise Figure	2.4	2.8	2.9	3.0	3.2	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3V,50 Ω system. measure on Evaluation Board. (DSA to AMP)
2. 70MHz measured with application circuit refer to table 11.
3. Gain data has PCB & Connectors insertion loss de-embedded.
4. OIP3 measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(VDD)	Amp/DSA			3.6/5.5	V
Supply Current	Amp		110		mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+12/+30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Amp + DSA	30		4000	MHz
Supply Voltage	Amp		3		V
	DSA	2.7		5.5	V
Operating Temperature	Amp + DSA	-40		85	℃

Specifications are not guaranteed over all recommended operating conditions.

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the BVA303. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of six CMOS compatible control lines that select the desired attenuation state, as shown in *Table 5*.

The parallel interface timing requirements are defined by *Figure 4* (Parallel Interface Timing Diagram), *Table 8* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 3*) to latch the new attenuation state into the device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 3* (Serial Interface Timing Diagram) and *Table 6* (Serial Interface AC Characteristics).

Power-up Control Settings

The BVA303 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 6.*
(Power-Up Truth Table, Parallel Mode).

Table 5. Truth Table

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation state
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in table

Table 6. Parallel PUP Truth Table

P/S	LE	PUP2	PUP1	Attenuation state
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5-C16

Note: Power up with LE = 1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active

Figure 3. Serial Interface Timing Diagram

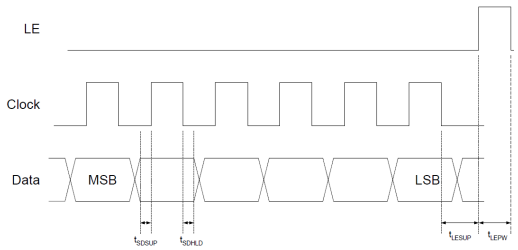


Figure 4. Parallel Interface Timing Diagram

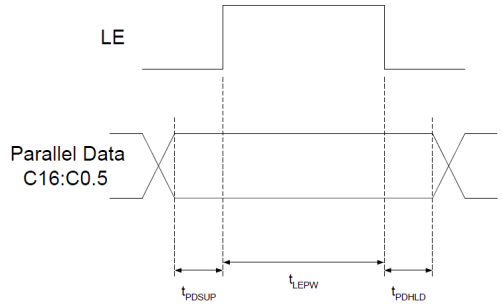


Table 7. Serial Interface AC Characteristics

VDD = 3.3V with DSA only, -40°C < TA < 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification

Table 8. Parallel Interface AC Characteristics

VDD = 3.3V with DSA only, -40°C < TA < 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before rising edge of LE	10		ns
t_{PDHLD}	Data hold time after falling edge of LE	10		ns

Table 9. 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B3	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) ↑ ... ↑ LSB (Last in)

Figure 5. Pin Configuration(Top View)

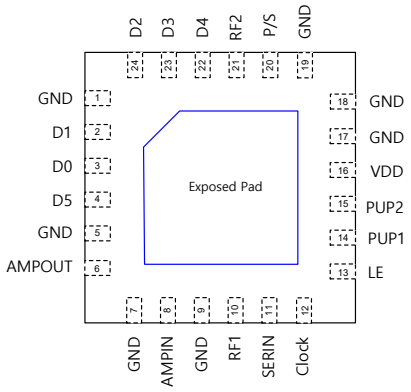


Table 10. Pin Description

Pin	Pin name	Description
1,5,7,9, 17,18,19	GND	Ground
2	C1	Attenuation control bit, 1dB
3	C0.5[4]	Attenuation control bit, 0.5dB
4	C16[2,4]	Attenuation control bit, 16dB
6	AMPOUT	RF Amp out Port
8	AMPIN	RF Amp in port
10	RF1[1]	RF port (DSA output)
11	DATA[2]	Serial interface data input
12	Clock	Serial interface clock input
13	LE[3]	Latch Enable input
14	PUP1[4]	Power-up selection bit 1
15	PUP2	Power-up selection bit 2
16	VDD	Supply voltage (nominal 3V)
20	P/S	Parallel/Serial mode select
21	RF2[1]	RF port (DSA input)
22	C8	Attenuation control bit, 8dB
23	C4	Attenuation control bit, 4dB
24	C2	Attenuation control bit, 2dB

Note: 1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met
2. Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance
3. This pin has an internal 2 MΩ resistor to internal positive digital supply
4. This pin has an internal 200 kΩ resistor to GND

Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 6. Gain[1] vs Frequency @ Temperature (Max Gain State)

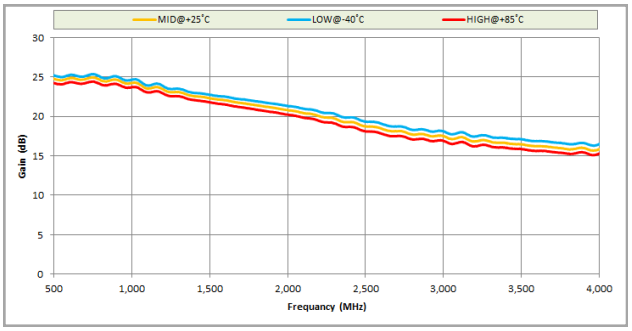
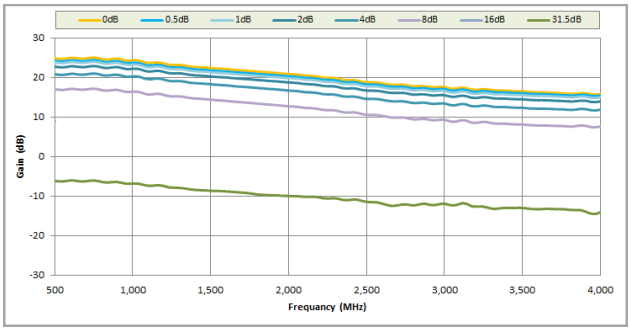


Figure 7. Gain vs Frequency @ Major Attenuation Steps



Note: **1.** Gain data has PCB & Connectors insertion loss de-embedded

Figure 8. Input Return Loss vs Frequency @ Temperature (Max Gain State)

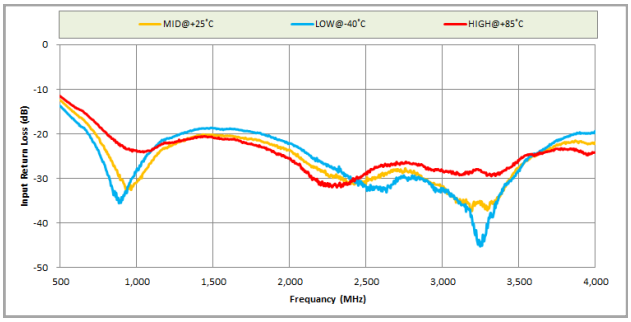
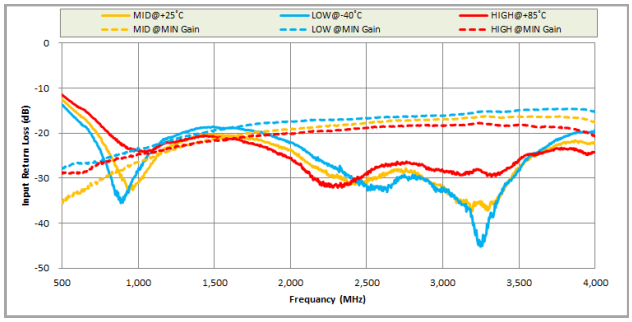


Figure 9. Input Return Loss vs Frequency @ Max Gain & Min Gain[1] State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 10. output Return Loss vs. Frequency @ Temperature (Max Gain State)

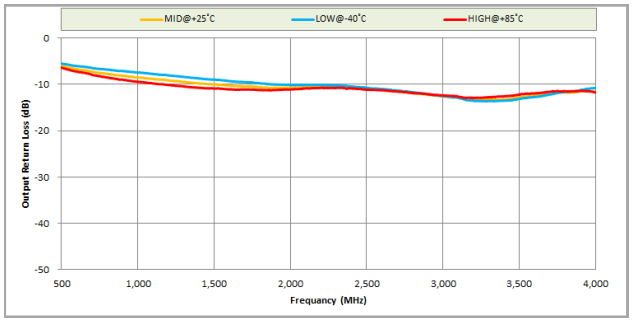
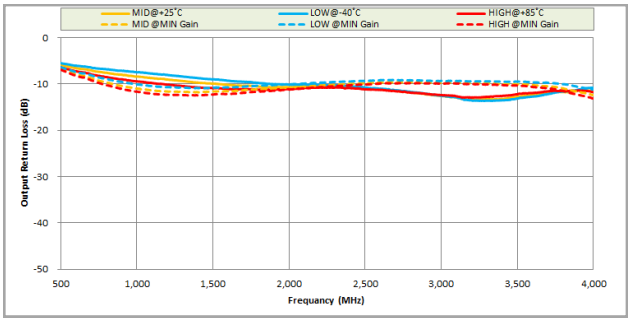


Figure 11. output Return Loss vs. Frequency @ Max Gain & Min Gain[1] State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 12. OIP3 vs Frequency @ Temperature (Max Gain State)

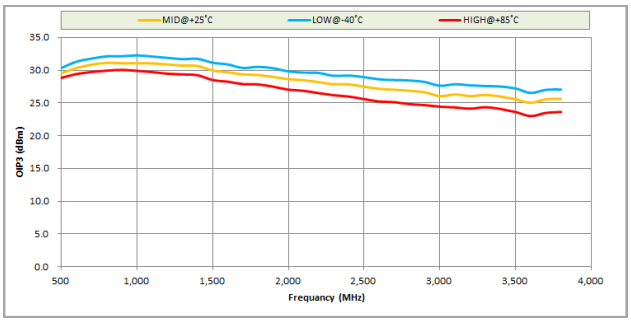


Figure 13. P1dB vs Frequency @ Temperature (Max Gain State)

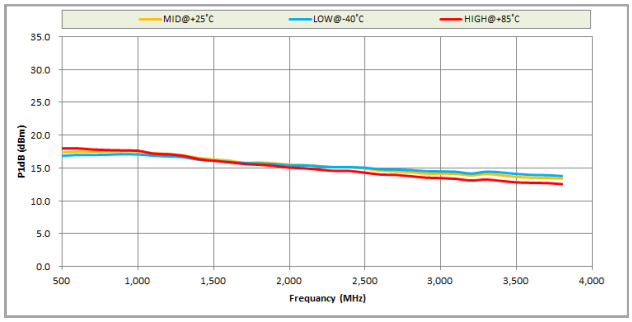


Figure 14. Noise Figure vs Frequency @ Temperature (Max Gain State)

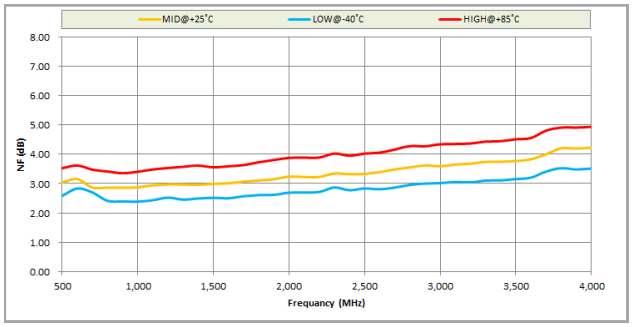


Figure 15. Attenuation Error vs Frequency @ Major Attenuation Steps

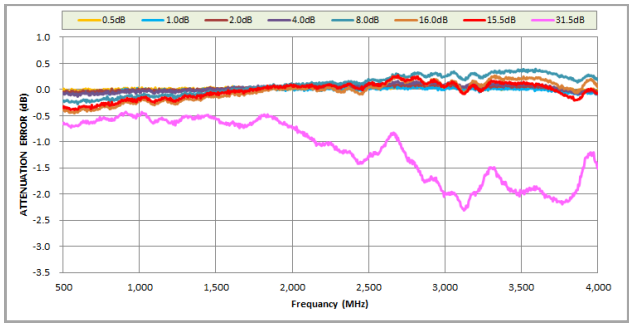


Figure 16. Attenuation Error vs Attenuation Setting @Major Frequency (Max Gain State)

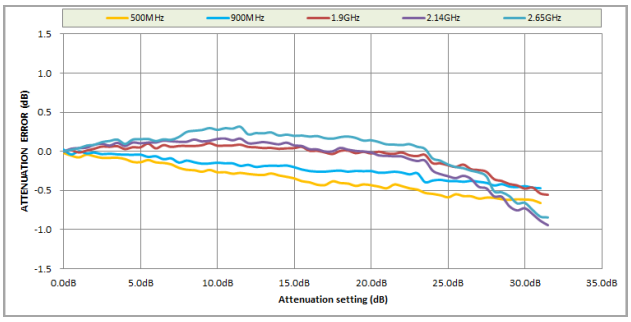
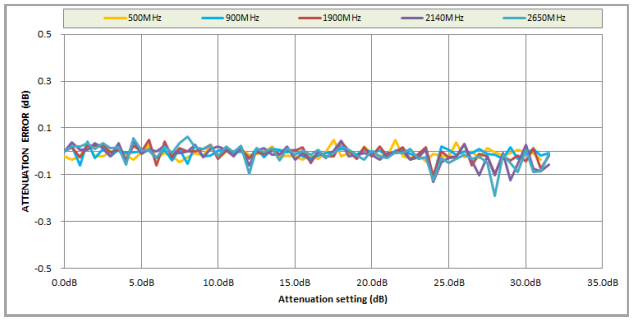


Figure 17. 0.5dB Step Attenuation vs Attenuation Setting @Major Frequency (Max Gain State)



Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 18. Attenuation Error @ 900MHz vs Temperature

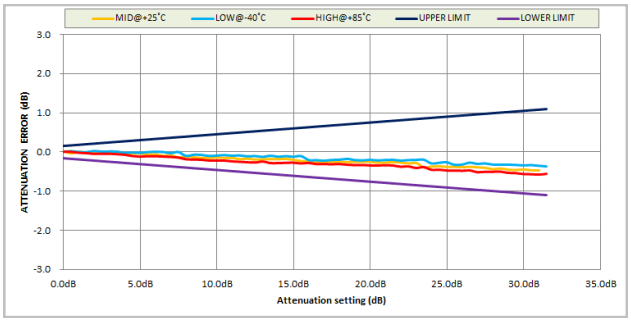


Figure 19. Attenuation Error @ 1.9GHz vs Temperature

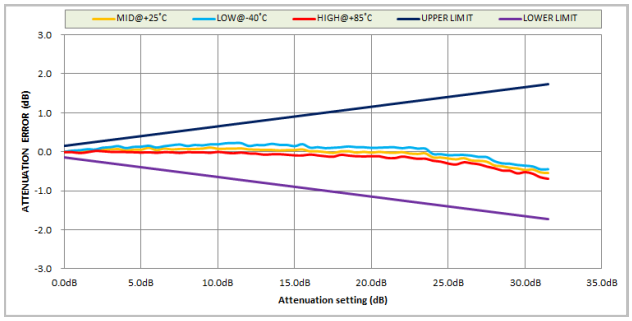


Figure 20. Attenuation Error @ 2.14GHz vs Temperature

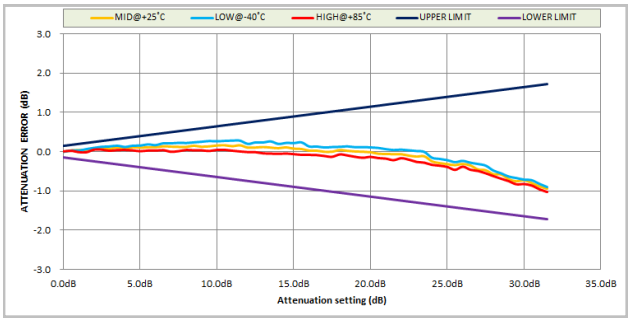


Figure 21. Attenuation Error @ 2.65GHz vs Temperature

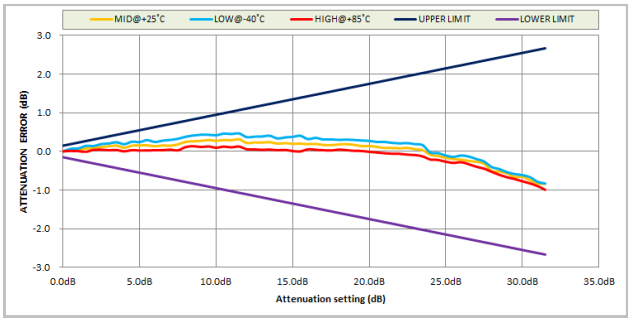
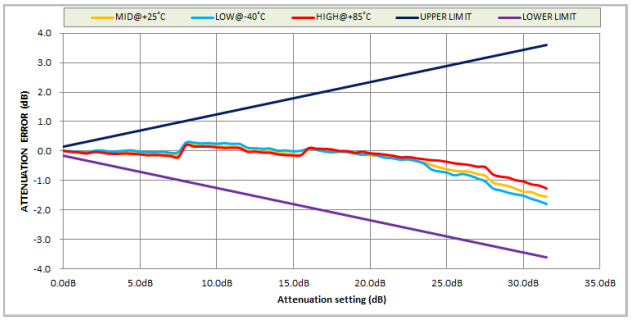


Figure 22. Attenuation Error @ 3.9GHz vs Temperature



Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 30~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 23. Gain[1] vs Frequency @ Temperature (Max Gain State)

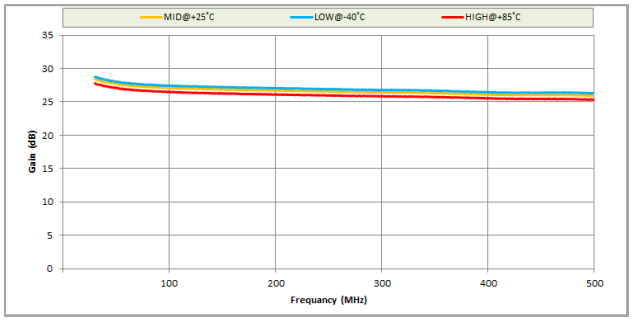
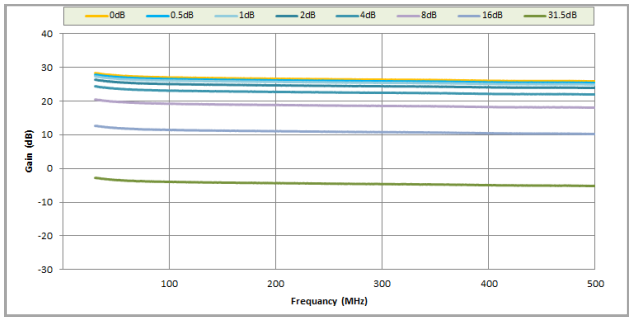


Figure 24. Gain vs Frequency @ Major Attenuation Steps



Note: **1.** Gain data has PCB & Connectors insertion loss de-embedded

Figure 25. Input Return Loss vs Frequency @ Temperature (Max Gain State)

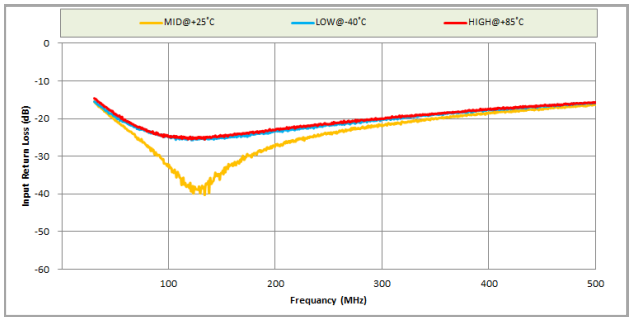
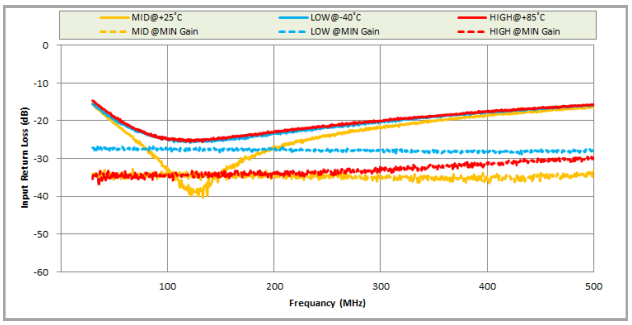


Figure 26. Input Return Loss vs Frequency @ Max Gain & Min Gain[1] State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 27. output Return Loss vs. Frequency @ Temperature (Max Gain State)

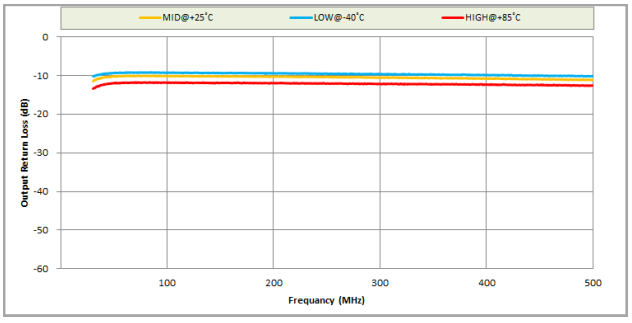
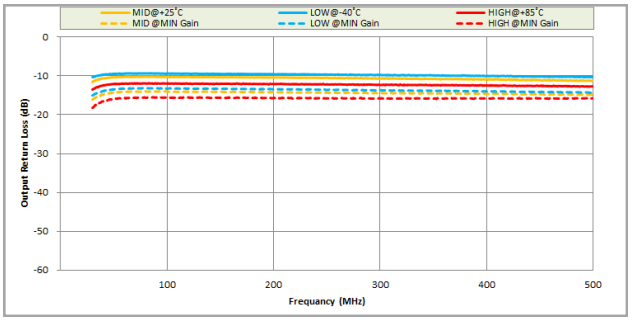


Figure 28. output Return Loss vs. Frequency @ Max Gain & Min Gain[1] State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 30~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 29. OIP3 vs Frequency @ Temperature (Max Gain State)

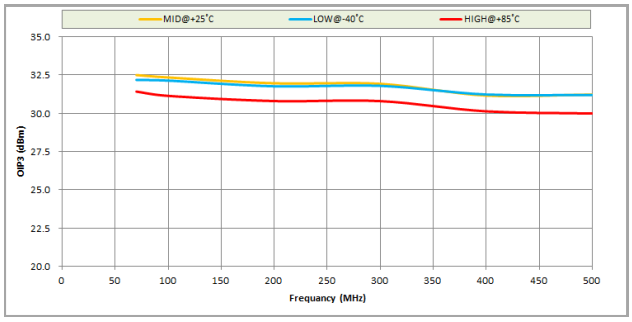


Figure 30. P1dB vs Frequency @ Temperature (Max Gain State)

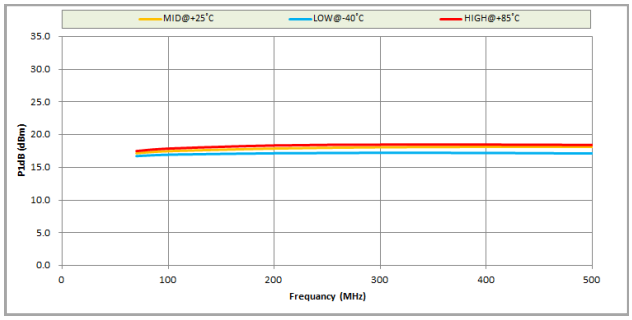


Figure 31. Noise Figure vs Frequency @ Temperature (Max Gain State)

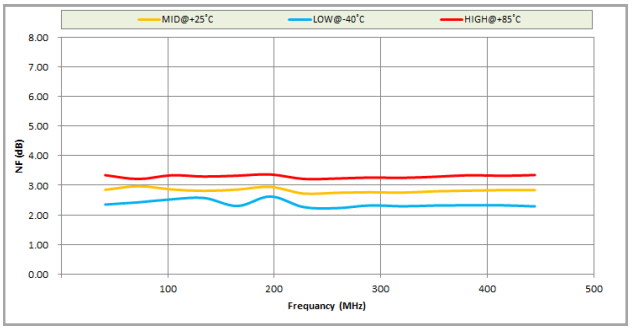


Figure 32. Attenuation Error vs Frequency @ Major Attenuation Steps

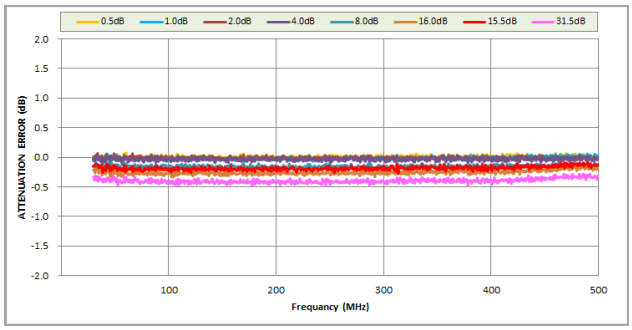


Figure 33. Attenuation Error vs Attenuation Setting @Major Frequency (Max Gain State)

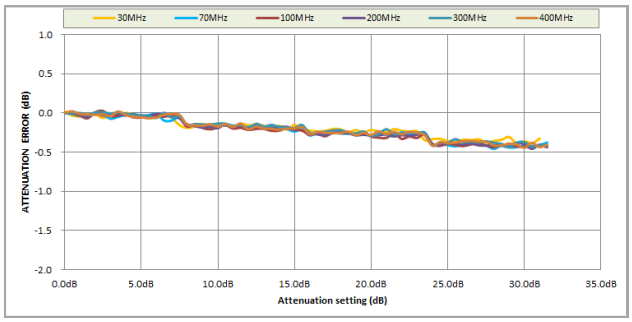
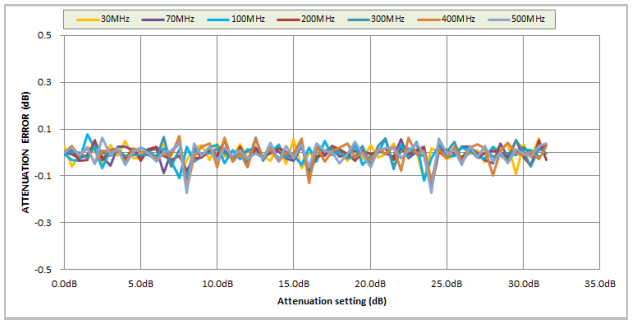


Figure 34. 0.5dB Step Attenuation vs Attenuation Setting @Major Frequency (Max Gain State)



Typical Performance Plot - BVA303 EVK - PCB (Application Circuit : 30~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted and Application Circuit refer to Table 11

Figure 35. Attenuation Error @ 30MHz vs Temperature

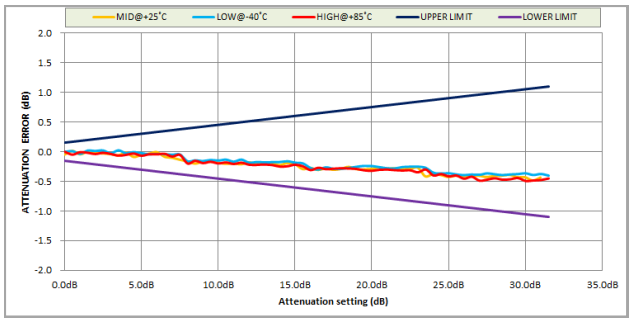


Figure 36. Attenuation Error @ 70MHz vs Temperature

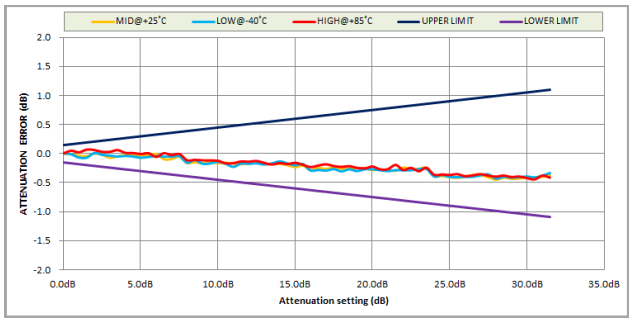


Figure 37. Attenuation Error @ 100MHz vs Temperature

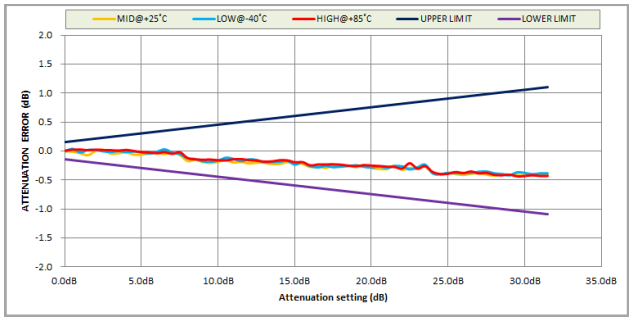


Figure 38. Attenuation Error @ 200MHz vs Temperature

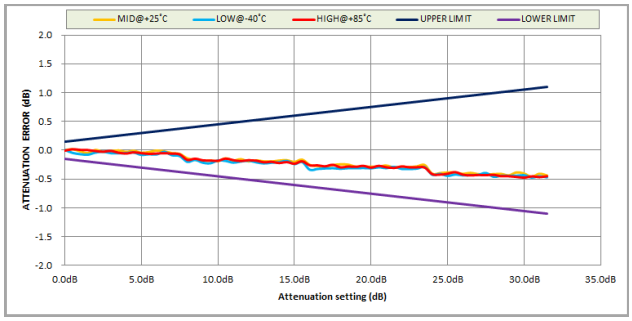


Figure 39. Attenuation Error @ 300MHz vs Temperature

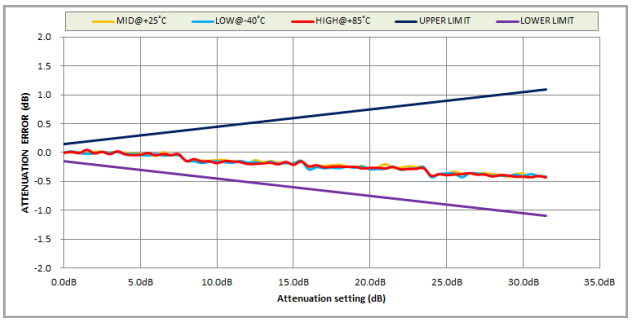
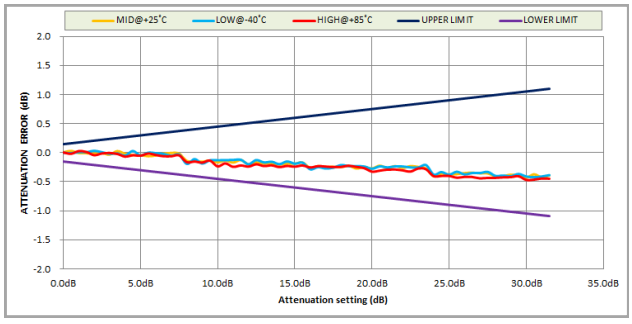


Figure 40. Attenuation Error @ 400MHz vs Temperature



Evaluation Board PCB Information

Figure 41. Evaluation Board PCB Layer Information

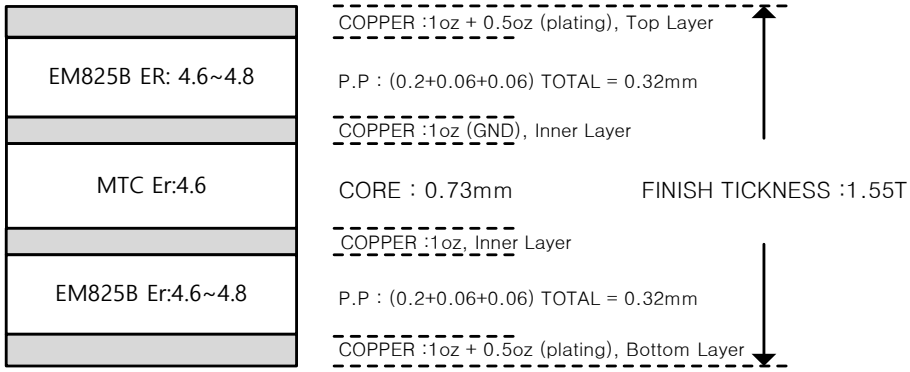


Figure 42. Evaluation Board PCB

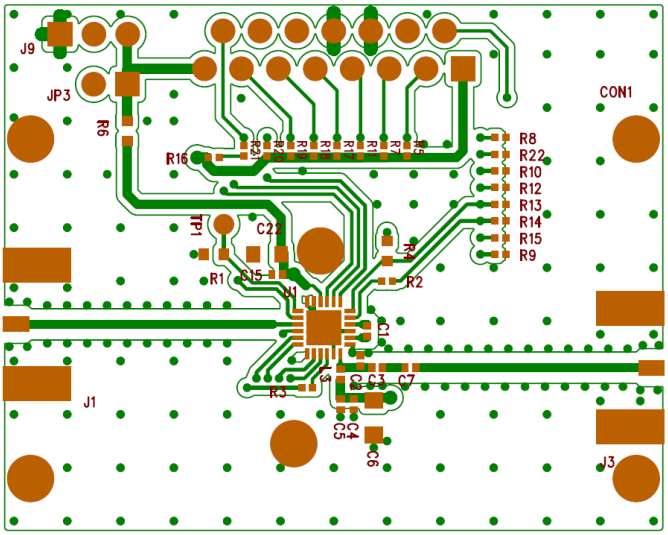


Figure 43. Evaluation Board Schematic

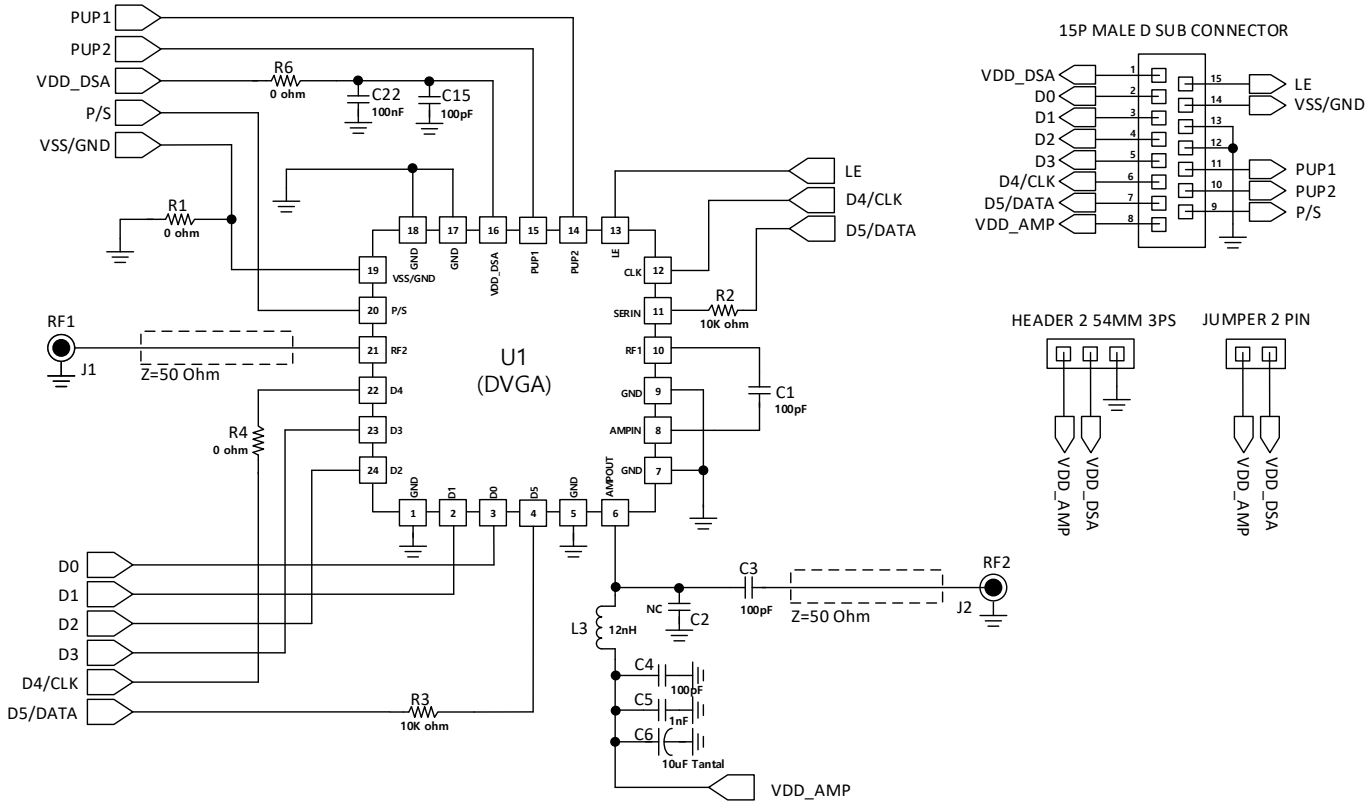


Table 11. Application Circuit

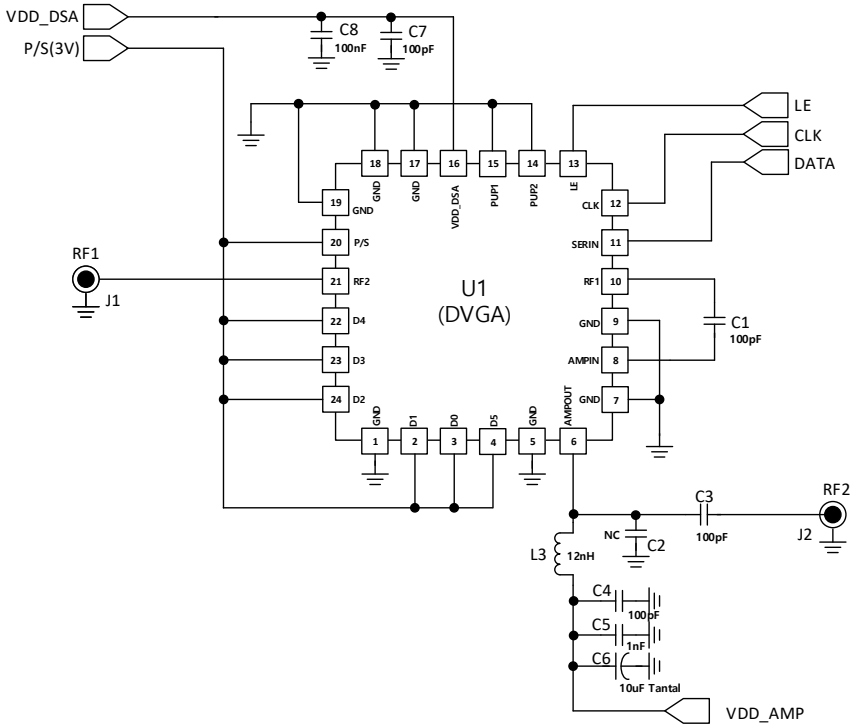
Application Circuit Values Example		
Freq.	IF Circuit 50~500MHz	RF Circuit 500MHz ~ 4GHz
C1/C3	2nF	100pF
L3(1005 Chip Ind)	820nH	12nH

Table 12. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C1,C3	2	CAP 0402 100pF J 50V	IF circuit refer to table 11
2	C4,C15	2	CAP 0402 100pF J 50V	
3	C5	1	CAP 0402 1000pF J 50V	
4	C6	1	TANTAL 3216 10UF 16V	
5	C22	1	TANTAL 3216 0.1uF 35V	
6	L3	1	IND 1608 12nH	IF circuit refer to table 11
7	R2,R3	2	RES 1005 J 10K	
8	R1,R4,R6	3	RES 1608 J 0ohm	
9	CON1	1	15P-MALE-D-sub con-nector	
10	U1	1	QFN4X4_24L_BVA303	
11	J1,J3	2	SMA_END_LAUNCH	

Notice: Evaluation Board for Marketing Release was set to 500MHz to 4GHz application circuit (Refer to Table 11)

Figure 44. Recommended Serial mode Application Circuit schematic* (with maximum attenuation)



*. The serial mode PUP state of this Figure 44. is setting in **Maximum Attenuation** (31.5dB) and each combinations of C0.5-C16 are shown in the Table 4. Truth Table.

Figure 45. Suggested PCB Land Pattern and PAD Layout

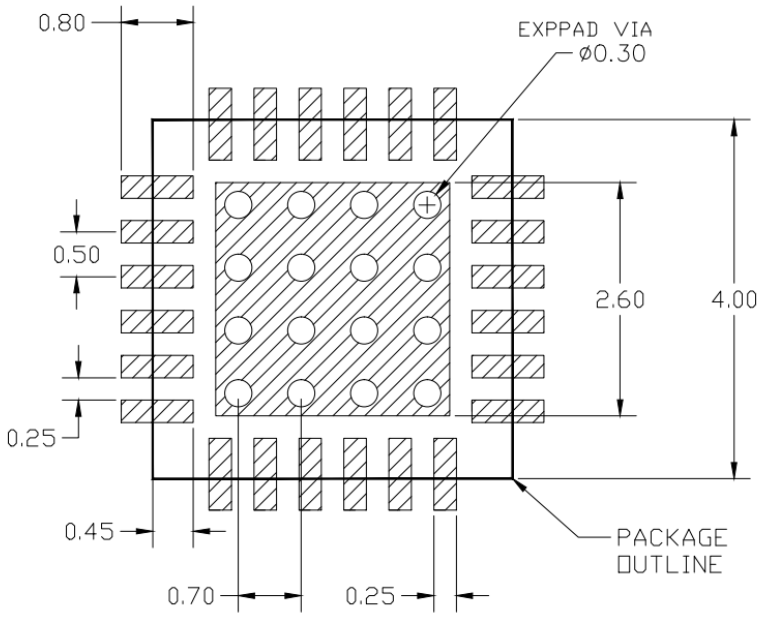
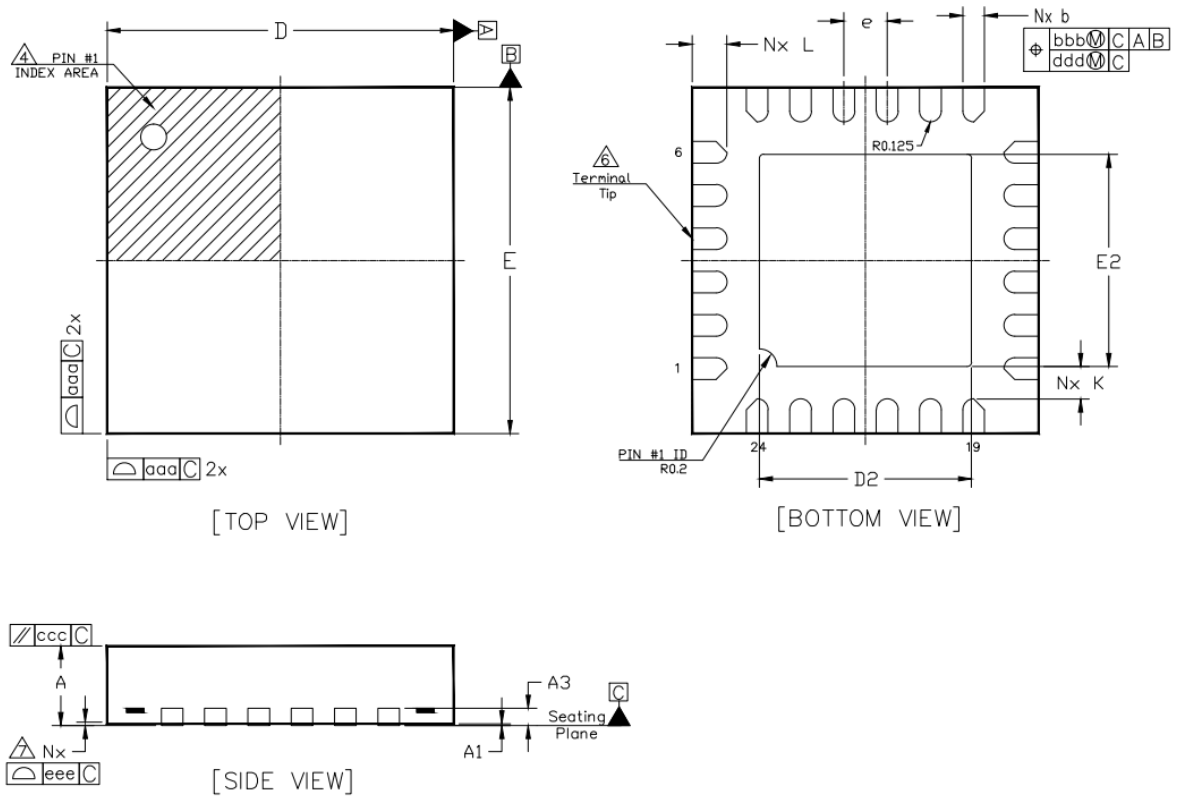


Figure 46. Package Outline Dimension

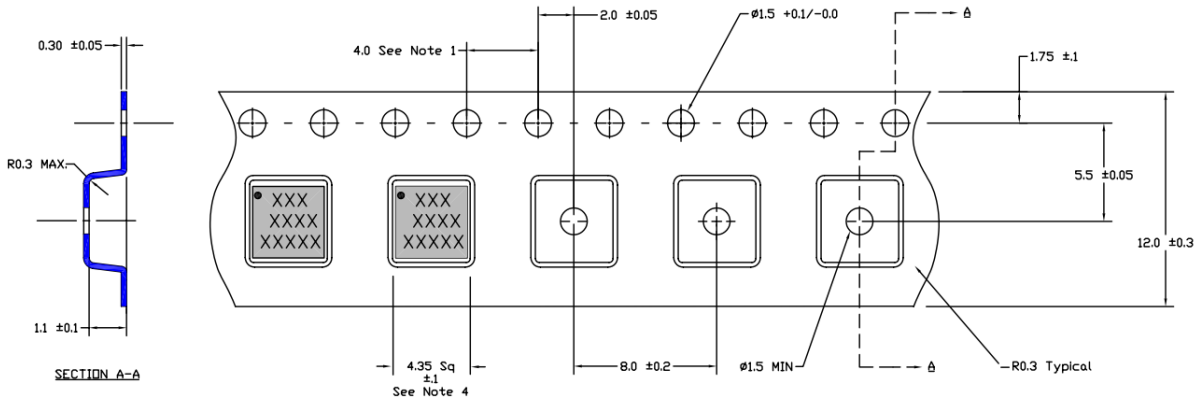


NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)				
Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.18	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.30	2.45	2.55	
E2	2.30	2.45	2.55	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
ND		6		5
NE		6		5

Figure 47. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 48. Package Marking

Marking information:	
BVA303	Device Name
YY	Year
WW	Work Week
XX	LOT Number

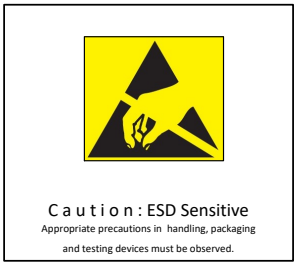
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1B
Value:	500V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2014
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**