MOTOROLA

MC54/74F646
MC54/74F648

Product Preview

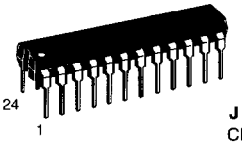
OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS

OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS

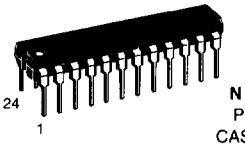
FAST™ SCHOTTKY TTL

These devices consist of bus transceiver circuits with 3-state D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable $\overline{OE}$ is Active LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

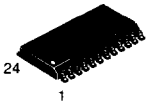
- Independent Registers for A and B
- Multiplexed Real-Time and Stored Data
- Choice of True (F646) and Inverting (F648) Data Paths
- 3-State Outputs



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03

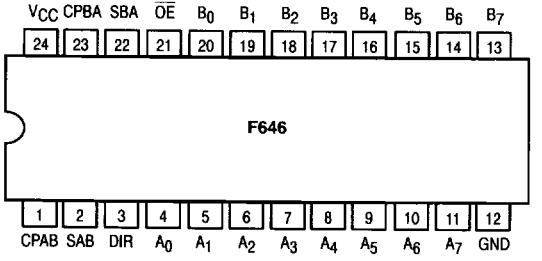


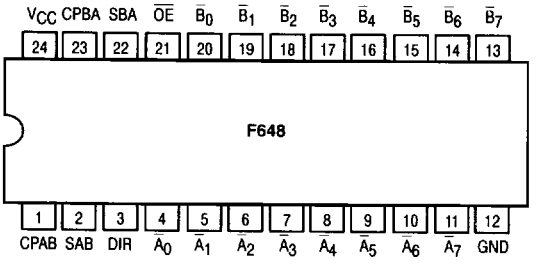
DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

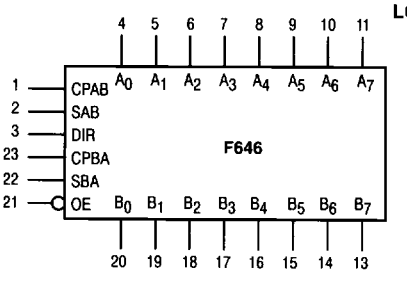
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

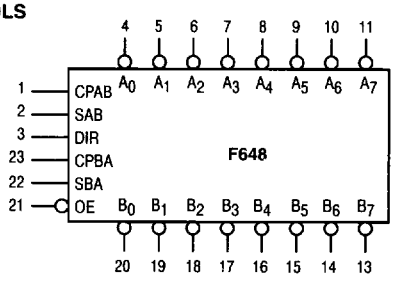
PIN ASSIGNMENTS





LOGIC SYMBOLS





FUNCTION TABLE

Inputs						Data I/O*		Operation/Function
OE bar	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X	Input	Input	Store A_n Data in A Register
H	X	X	↑	X	X	Input	Input	Store B_n Data in B Register
H	X	↑	↑	X	X	Input	Input	Store A_n/B_n Data in A/B Register
L	H	X	X	L	X	Input	Output	A_n to B_n — Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Store A_n Data in A Register
L	H	H or L	X	H	X	Input	Output	A Register to B_n (Stored Mode)
L	H	↑	X	H	X	Input	Output	Clock A_n Data to B_n and into A Register
L	L	X	X	X	L	Output	Input	B_n to A_n — Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Store B_n Data in B Register
L	L	X	H or L	X	H	Output	Input	B Register to A_n (Stored Mode)
L	L	X	↑	X	H	Output	Input	Clock A_n Data to B_n and into B Register

*The data output function may be enabled or disabled by various signals at the OE bar and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the appropriate clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = Don't Care

↑ = Low-to-High transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	DC Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74	— —	— —	−12 −15	mA
I_{OL}	Output Current — Low	54 74	— —	— —	48 64	mA

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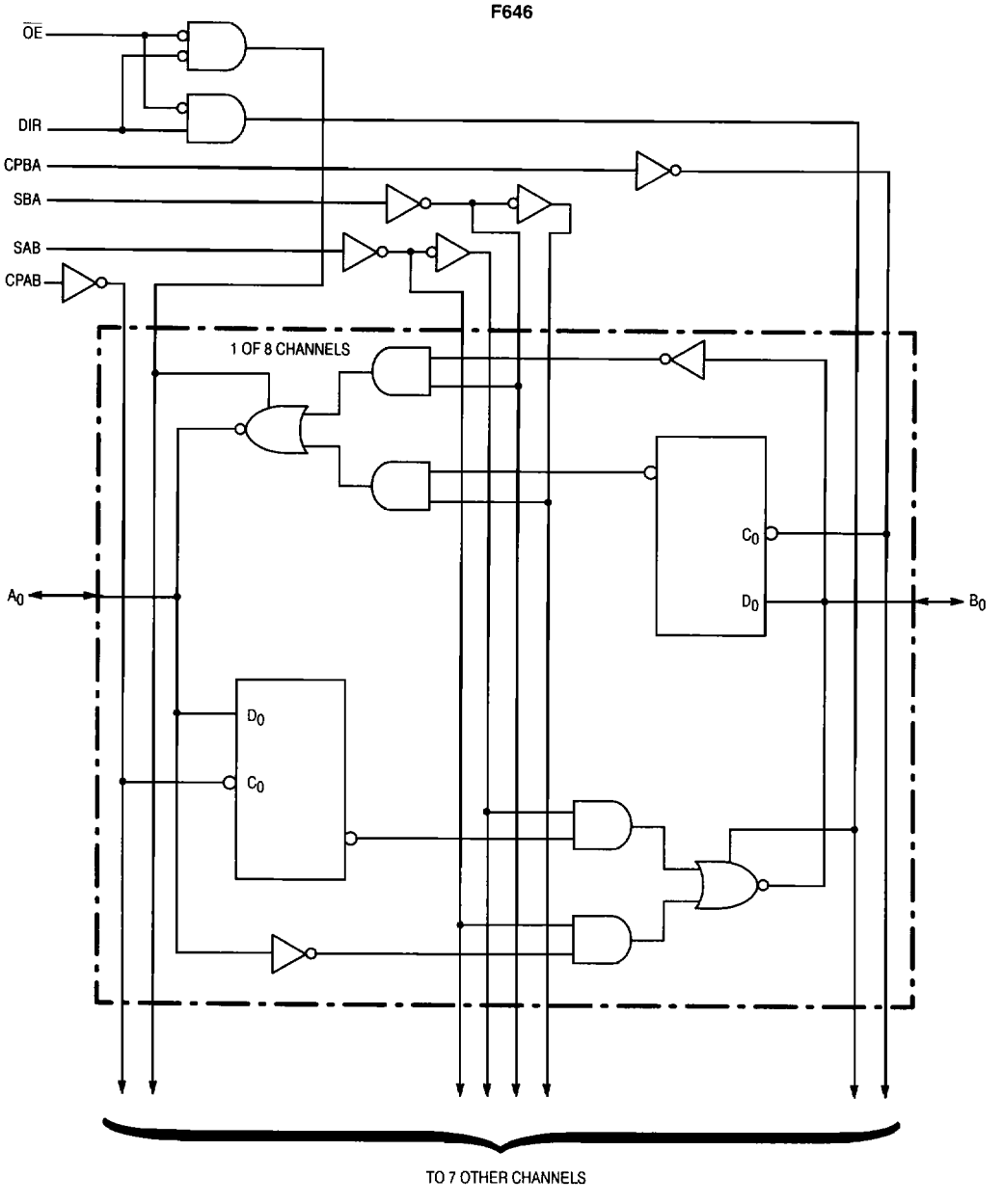
LOGIC DIAGRAM
F646



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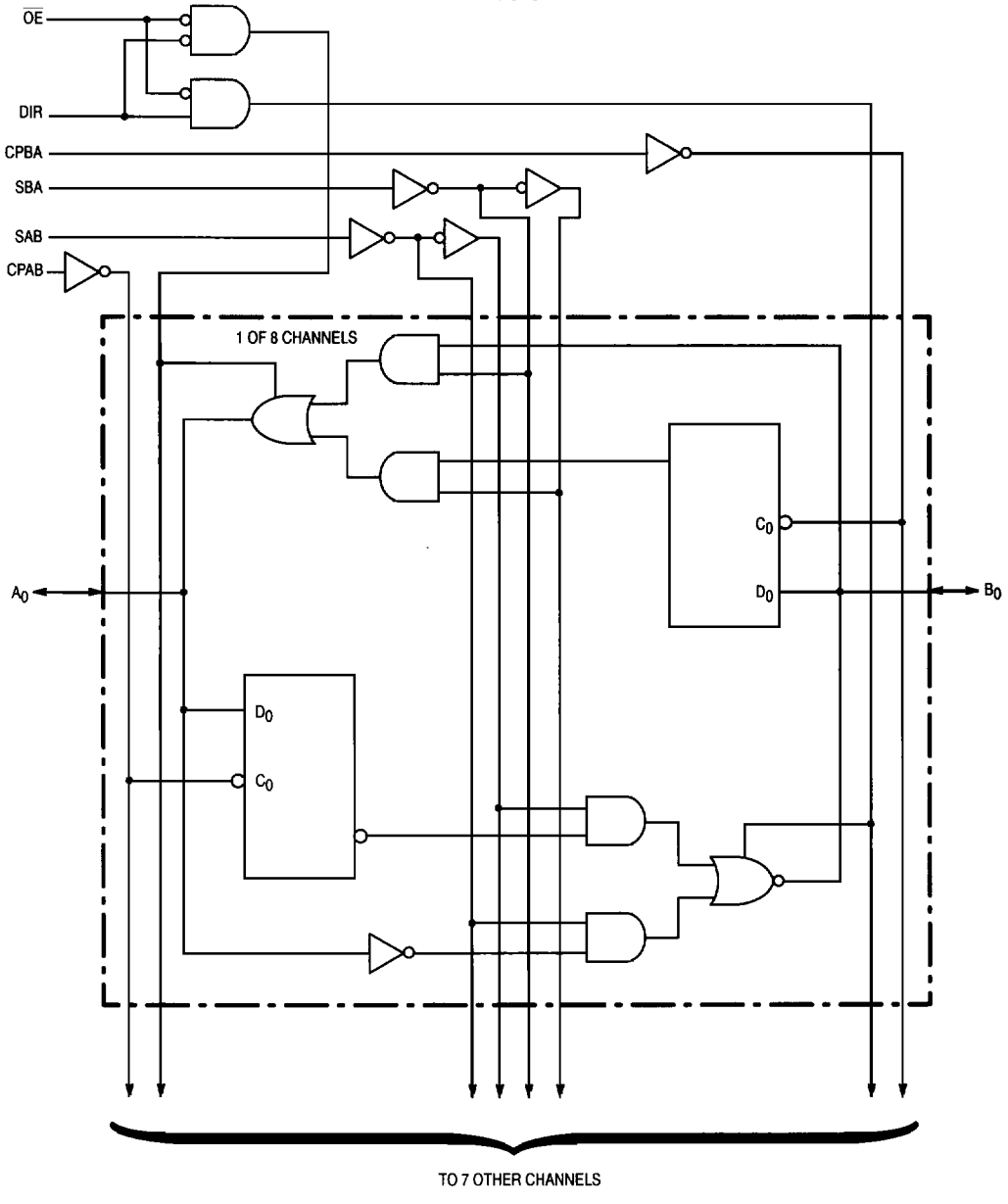
LOGIC DIAGRAM
F648



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter			Limits Min	Limits Typ	Limits Max	Unit	Test Conditions (Note 1)	
V_{IH}	Input HIGH Voltage			2.0	—	—	V	Guaranteed as a HIGH Signal	
V_{IL}	Input LOW Voltage			—	—	0.8	V	Guaranteed as a LOW Signal	
V_{IK}	Input Clamp Diode Voltage			—	—	−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	A_n, B_n	54/74	2.4	—	—	V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
			74	2.7	—	—	V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
			54	2.0	—	—	V	I_{OH} = −12.0 mA	V_{CC} = 4.5 V
			74	2.0	—	—	V	I_{OH} = −15.0 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	A_n, B_n	54	—	—	0.55	V	I_{OL} = 48 mA	V_{CC} = MIN
			74	—	—	0.55	V	I_{OL} = 64 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current		Non I/O Pins	—	—	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
			Non I/O Pins	—	—	100	µA	V_{CC} = MAX, V_{IN} = 7.0 V	
			I/O (Aa, Bn)	—	—	1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current		Non I/O Pins	—	—	−600	µA	V_{CC} = MAX, V_{IN} = 0.5 V	
$I_{IH} + I_{OZH}$	Output Leakage Current		I/O (A_n, B_n)	—	—	70	µA	V_{CC} = MAX	V_{OUT} = 2.7 V
$I_{IL} + I_{OZL}$	Output Leakage Current		I/O (A_n, B_n)	—	—	−650	µA	V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)			−100	—	−225	mA	V_{CC} = MAX, V_{OUT} = GND	
I_{CC}	Power Supply Current		I_{CCH}	—	—	135	mA	V_{out} = HIGH	V_{CC} = MAX
			I_{CCL}	—	—	150		V_{out} = LOW	
			I_{CCZ}	—	—	150		V_{out} = HIGH Z	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF R_L = 500 Ω		54F T_A = –55°C to +125°C V_{CC} = +5.0 V ±10% C_L = 50 pF R_L = 500 Ω		74F T_A = 0°C to +70°C V_{CC} = +5.0 V ±10% C_L = 50 pF R_L = 500 Ω		Unit
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100	—	75	—	90	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0 2.0	7.0 8.0	2.0 2.0	8.5 9.5	2.0 2.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (F646)	1.0 1.0	7.0 6.5	1.0 1.0	8.0 8.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (F648)	1.0 1.0	7.0 6.5	1.0 1.0	10.0 9.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n	2.0 2.0	7.5 7.5	2.0 2.0	10.0 10.0	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A_n or B_n	2.0 2.0	7.0 7.0	2.0 2.0	9.5 9.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A_n or B_n	1.0 2.0	7.0 7.0	1.0 2.0	9.5 9.5	1.0 2.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A_n or B_n	2.0 2.0	7.0 7.0	2.0 2.0	9.5 9.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A_n or B_n	1.0 2.0	7.0 7.0	1.0 2.0	9.5 9.5	1.0 2.0	8.5 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF R_L = 500 Ω		54F T_A = –55°C to +125°C V_{CC} = +5.0 V ±10% C_L = 50 pF R_L = 500 Ω		74F T_A = 0°C to +70°C V_{CC} = +5.0 V ±10% C_L = 50 pF R_L = 500 Ω		Unit
		Min	Max	Min	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW Bus to Clock	4.0 4.0	— —	5.0 5.0	— —	5.0 5.0	— —	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW Bus to Clock	0.0 0.0	— —	0.0 0.0	— —	0.0 0.0	— —	ns
$t_{w(H)}$ $t_{w(L)}$	Clock Pulse Width HIGH or LOW	4.0 5.0	— —	4.0 5.0	— —	4.0 5.0	— —	ns

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