National Semiconductor

PRELIMINARY

T-45-23-05

MM54HC160/MM74HC160 Synchronous Decade Counter with Asynchronous Clear
MM54HC161/MM74HC161 Synchronous Binary Counter with Asynchronous Clear
MM54HC162/MM74HC162 Synchronous Decade Counter with Synchronous Clear
MM54HC163/MM74HC163 Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize advanced silicon-gate CMOS technology and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

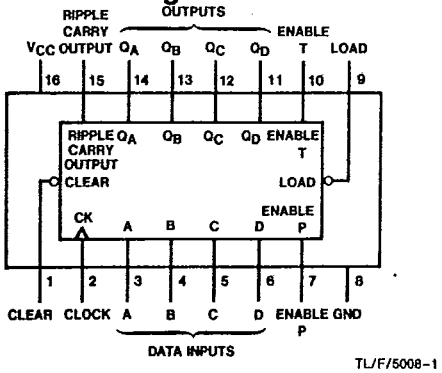
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

Connection Diagram



TL/F/5008–1

Order Number MM54HC160/161/162/163* or MM74HC160/161/162/163*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

T-45-23-05

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

3

T-45-23-05

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		27	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	40	27	21	18	MHz
			6.0V	45	32	25	21	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		2.0V	100	215	271	320	ns
			4.5V	32	43	54	64	ns
			6.0V	28	37	46	54	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		2.0V	88	175	220	260	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		2.0V	95	205	258	305	ns
			4.5V	30	41	52	61	ns
			6.0V	26	35	44	52	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	85	170	214	253	ns
			4.5V	17	34	43	51	ns
			6.0V	14	29	36	43	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		2.0V	90	195	246	291	ns
			4.5V	28	39	49	58	ns
			6.0V	24	33	42	49	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		2.0V	80	160	202	238	ns
			4.5V	16	32	40	48	ns
			6.0V	14	27	34	41	ns
t_{PHL}	Maximum Propagation Delay, Clear to RC		2.0V	100	220	275	325	ns
			4.5V	32	44	55	66	ns
			6.0V	28	37	47	55	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		2.0V	100	210	260	315	ns
			4.5V	32	42	52	63	ns
			6.0V	28	36	45	54	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		125	158	186	ns
			4.5V		25	32	37	ns
			6.0V		21	27	32	ns
t_S	Minimum Setup Time Clear or Data to Clock		2.0V		150	190	225	ns
			4.5V		30	38	45	ns
			6.0V		26	32	38	ns
t_S	Minimum Setup Time Load to Clock		2.0V		135	170	200	ns
			4.5V		27	34	41	ns
			6.0V		23	29	35	ns
t_H	Minimum Hold Time Data from Clock		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time Enable, Load or Clear to Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns

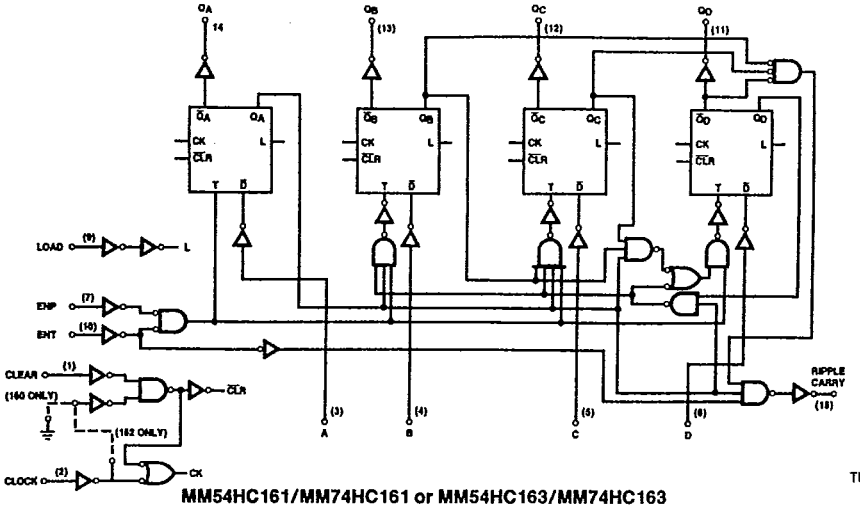
AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_W	Minimum Pulse Width Clock, Clear, or Load		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	40	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

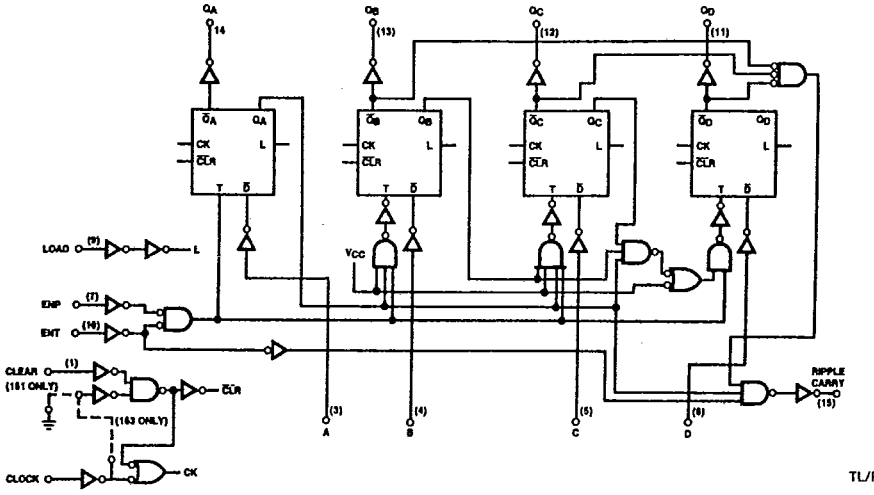
Logic Diagrams

MM54HC160/MM74HC160 or MM54HC162/MM74HC162



TL/F/5008–2

MM54HC161/MM74HC161 or MM54HC163/MM74HC163

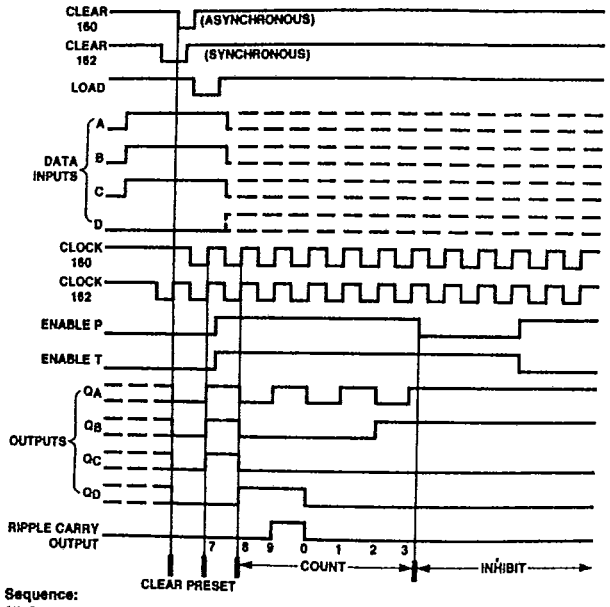


TL/F/5008–3

T-45-23-05

Logic Waveforms

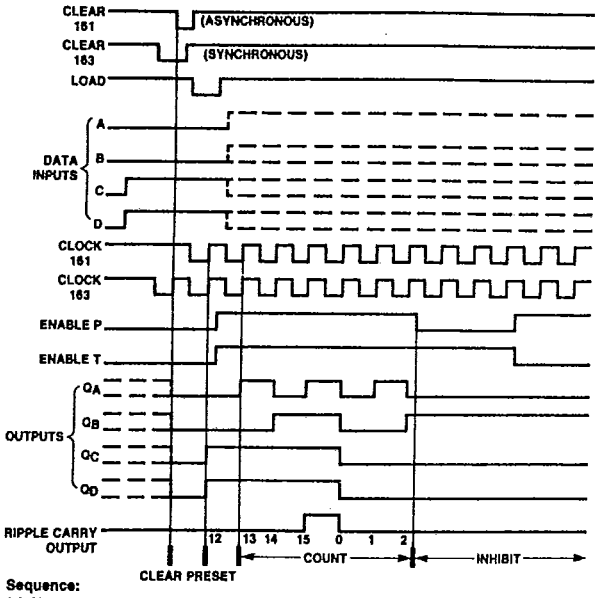
160, 162 Synchronous Decade Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–4

Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, 163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–5

Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit